Integrated Operation of Image Capturing and Processing in FPGA

Chi-Jeng Chang†, *Pei-Yung Hsiao*††, *Zen-Yi Huang*†

†*Dept. of Computer and Information Engineering, Jin Wen Institute of Technology, Hsin-Tien, Taipei, Taiwan, R.O.C.*
††*Dept. of Electronics Engineering, Chang Gung University, Tao-Yuan, Taiwan, R.O.C.*

Summary

This paper presents a Field Programmable Gate Array (FPGA) integrated architecture to perform a pipelined operations of image capturing, convolution and sorting, which were usually operated in series. FPGA receives pixels from image sensor in series, when they are able to be filled in a first n×n window. A convolution with selected coefficients of n×n matrix can be started to obtain a target image pixel. After the target image pixels are filled in another n×n window again. Maheshwari sorting is performed and three values (max, mid, min) are obtained simultaneously, ready for next processing.

Convolution and sorting help further filter image noises, such as dark current noise and Fixed Pattern Noise (FPN) in CMOS image sensor. This is one of the main reasons that make this integrated image processing device in FPGA demonstrate a high image qualities. A faster capturing speed is also gained due to using hardware-oriented FPGA instead of ordinary software programmed 8051 series microprocessors. This integrated processing device might relieve the microcontrollers of extensive software image computing if applied in a embedded system.

Key words:
CMOS image sensor, Digital image processing, FPGA, image capturing.

1. Introduction

The FPGA integrated processing architecture shown in Figure 1, consists of four units, namely, initialization unit (INU), data transfer unit (DTU), image processing unit (IPU) and memory management unit (MMU). MMU manages the object (processed) image to be stored in external memory while the related settings information about sensor exposure time, frame size, filter selection etc. are stored in the internal memory. Initialization unit (INU) accesses the necessary settings stored in the MMU for the system initialization when system is started. Image processing unit (IPU) does the pipelined operations of the image capturing, convolution and sorting.

Section 2 makes literature reviews about image convolution and 2-D sorting. Section 3 describes how initialization does the necessary settings. Section 4 describes more detail in IPU. Section 5 describes some detail of MMU and DTU for the data transfer in the system. Section 6 shows some experiment results from the system. A concluding remark is described in Section 7.

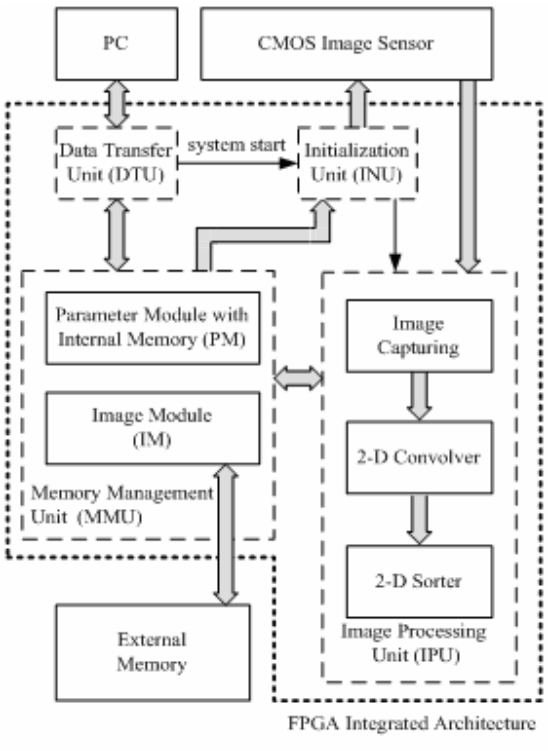


Fig. 1. Block diagram of FPGA integrated processing Architecture

2. Theoretical Consideration

2.1 Convolution as a Filter

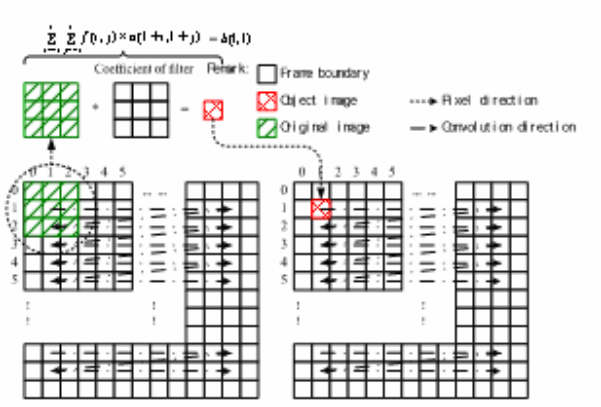
The original image(o) obtained from any source (camera, picture…) can be processed by a function to obtain a result

Manuscript revised August 22, 2005.

called object image(b) as shown in the following equation, and the related graph in Figure 2.

$$b(m,n) = \sum_{i=-1}^{1}\sum_{j=-1}^{1} f(i,j) \times o(m+i, n+j)$$

Function f (i,j) is one element of filter coefficient, in a position at i-th row and j-th column.



(A) original image(o) (B) object image(b)

Figure 2. Object image (b) is a result from an original image (o) convolved by a filter function

Many functions can be used for convolution of which image filtering is one of its applications. There are coefficients for three filter functions listed in Figure 3, the result images after convolutions and the original image will be shown in Section 6 for comparison.

1/9	1/9	1/9
1/9	1/9	1/9
1/9	1/9	1/9

(a) Averaging filter

(b) Gaussian filter

-1/9	-1/9	-1/9
-1/9	8/9	-1/9
-1/9	-1/9	-1/9

(c) High pass filter

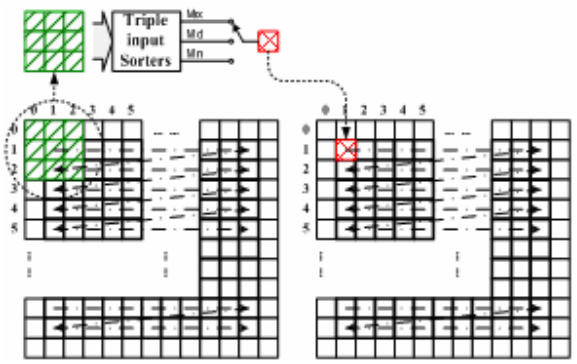
Figure 3. The coefficient of three filter functions

Image filtering is an important application in image processing [1]-[4]. It was first done through the software package of matrix operation. To increase the processing speed Crookes presented a hardware FPGA implementation around the year 2000 [5]-[8]. The details and our modification of Crookes' implementation will be shown in section 4.

2.2 Filtering by 2-D sorting

2-D sorting was presented by Maheshwari in 1997 [9]. It can sort a 3×3 matrix and find its maximum (Max), middle (Mid) and minimum (Min) elements simultaneously in one operation through 5 triple input sorters as shown in Figure 4.

The detailed FPGA implementation will be described in Section Ⅴ. The maximum value, the middle value, and the minimum value can be used for maximum filter, median filter, and minimum filter, respectively. The actual image outputs from these three filters will also be shown later in Section 6.



(A) original image(o) (B) object image(b)

Figure 4. Original image(o) going though the process of triple sorters to obtain a object image(b)

3. Initialization Unit

When system "start" signal is received by initialization unit, addresses are generated to MMU as shown in Figure 5, commands or parameters in MMU are sent to Initialization unit. The commands are decoded to generate different signals to the related units for necessary initial settings.

For example, exposure setting sent to CMOS Image Sensor by I^2C bus [10] [11]. Frame settings sent to Image Process Unit (IPU). These commands can be input to MMU from PC before or after system being started, which means the system operations can be changed or parameters be selected (such as image brightness, frame size, convolution coefficients, filtering parameters, etc.) at any time in system operation.

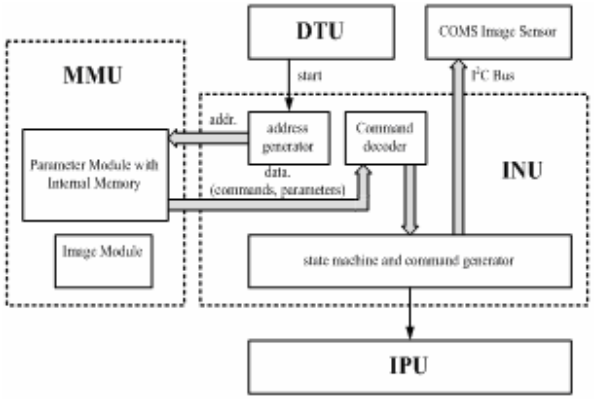


Figure 5. Block diagram of Initialization Unit (INU) & data connections with related units

4. Image Processing Unit

Figure 6, shows the control and data connections of IPU to other units as well as to the internal parts. IPU contains three parts, namely, image capturing, 2-D convolver, and 2-D sorters. They will be described in more detail in the followings;

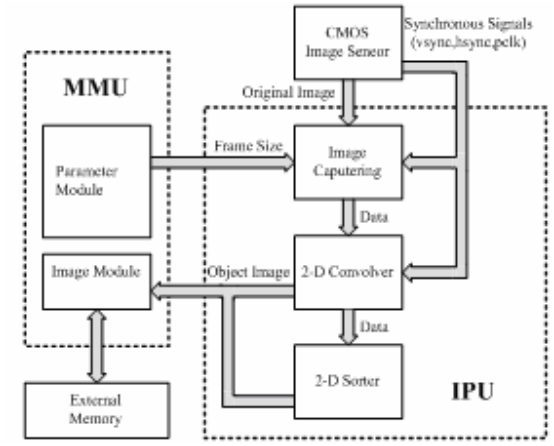


Figure 6. The control and data connections of IPU to other units and devices

4.1. Image Capturing

After INU finished its operations of initialization, "ic-go" control is enable from MMU, to start the image capturing operations. As shown in Figure 7, signal "valid" is enable from comparing xpos and ypos with the stored frame size, then "enable" signal is activated for sending the input image data to 2-D convolver if the image data are within the frame size, and image capturing is in busy state indicating IPU is busy in working condition.

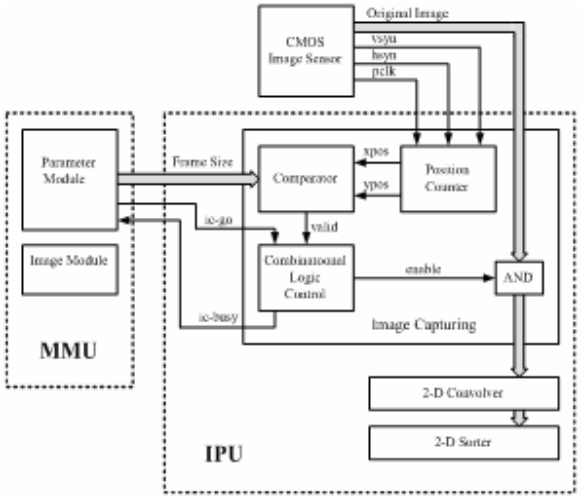


Figure 7. Internal and external connection of image capturing(ic) area

4.2 2-D convolver and modifications

Figure 8, shows Crookes' FPGA 2-D convolver, where Z^{-1} means after one clock delay and Z^{-ow} means after "ow" number of clock delay. Figure 9 shows an example 10x10(ow=10) image frame in which a 3×3 window is undergoing a convolution.

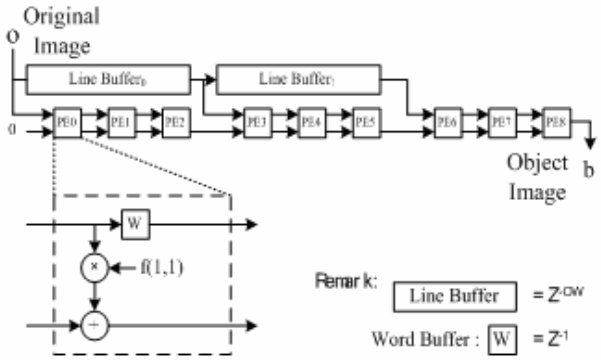


Figure 8. Crookes' FPGA 2-D convolver architecture

Figure 10a, shows the diagram when 10x10 frame is fit to the Crookes' convolver architecture. It needs 9 multipliers (represented by"↓") and 9 adders (represented by "•") as shown in Figure 10a. Figure 10a can also be modified like Figure 10b for simplicity.

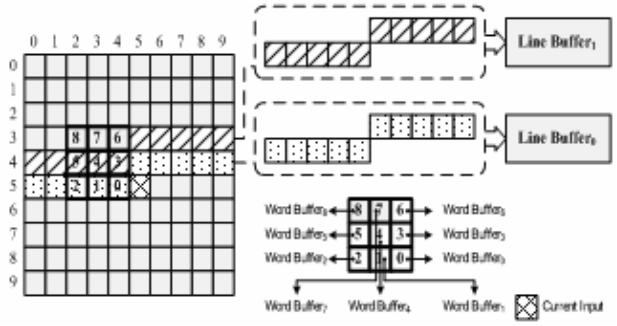


Figure 9. 10×10 image frame with 3×3 window for convolution

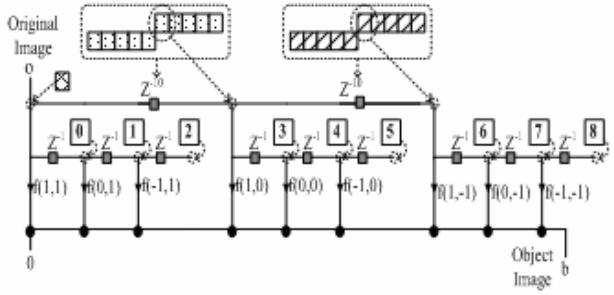


Figure 10a. hitting 10×10 frame in Crookes' convolver

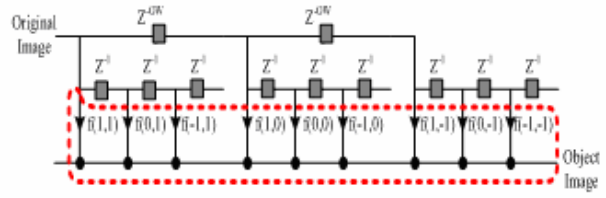


Figure 10b. Simplified representation of figure 10a

A modification of Crookes' convolver is shown in Figure 11, which just continually multiplies and adds (accumulates) the incoming pixels with a specific element (by means of multiplexing) of the nine coefficients. It then shifts to right. Only one multiplier and one addition are needed. It is quite a save (up to 90% saving) in circuit design without significant time delay.

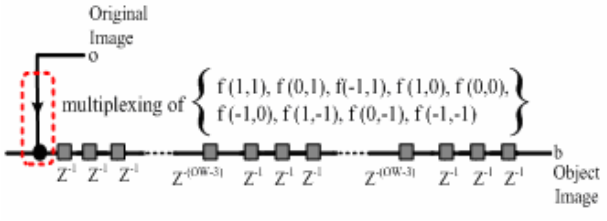


Figure 11. Modified Crookes' implementation with one multiply and one addition delay

4.3 Sorter implementation

Maheswari applied three 2-input bubble sorting algorithm to obtain a triple input sorter and implemented it in FPGA. The function of triple input sorter is shown in Figure 12.

By using triple input sorter , a 3×3 matrix can be sorted serially by vertical, horizontal and main diagonal and obtained the maximum, middle, and minimum values in the second diagonal (3 gray boxes) as shown in Figure 13.

Figure 12.Triple input sorting

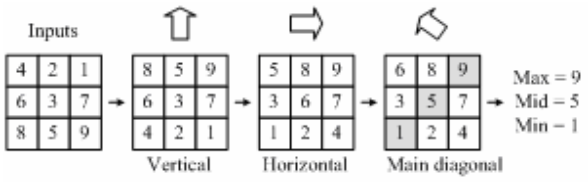


Figure 13. Three values (max, mid, min) obtained by triple input sorters

The triple input algorithm presented by Maheshwari, can be used to realize the 2-D sorting by combining 5 triple input sorters as shown in Figure 14, where the input "sort bus" at the upper left corner in Figure 14, is obtained form the right-hand side column of 3×3 window currently performing the convolution operation as shown in Figure 15.

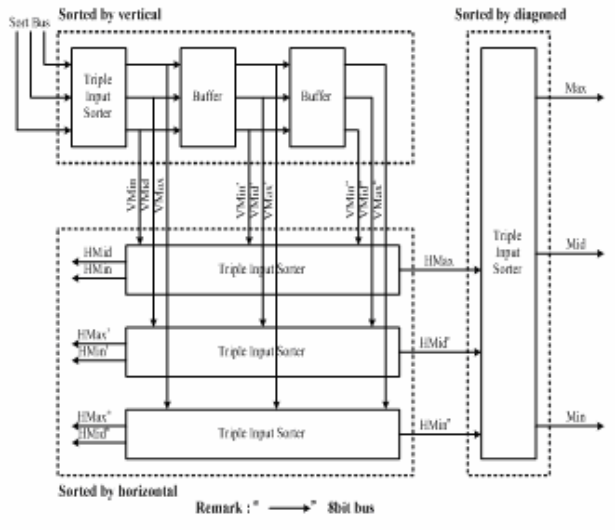


Figure 14. FPGA realization of 3×3 Maheshwari algorithm.

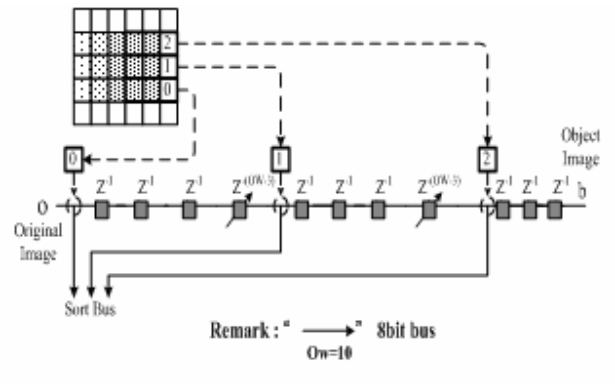


Figure 15. Sort bus is from 3×3 convolution window

From the above description of convolver and sorter the connections to both parts are shown in Figure 16.

The internal as well as external connections of IPU are shown in Figure 17. The overall operation in IPU can also be considered as 3-stage pipelined image process, namely, capturing, convolution and sorting.

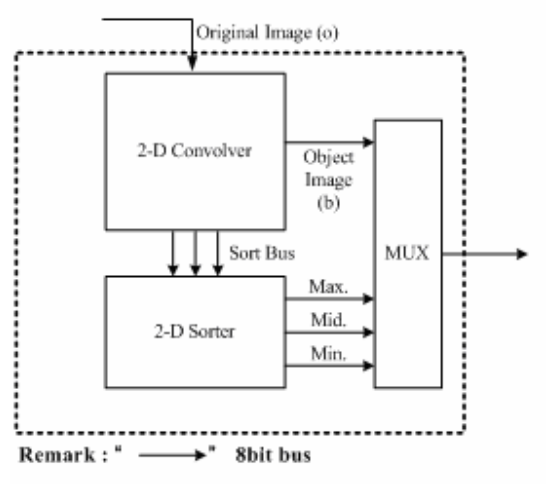


Figure 16. The external and internal connections of 2-D convolver

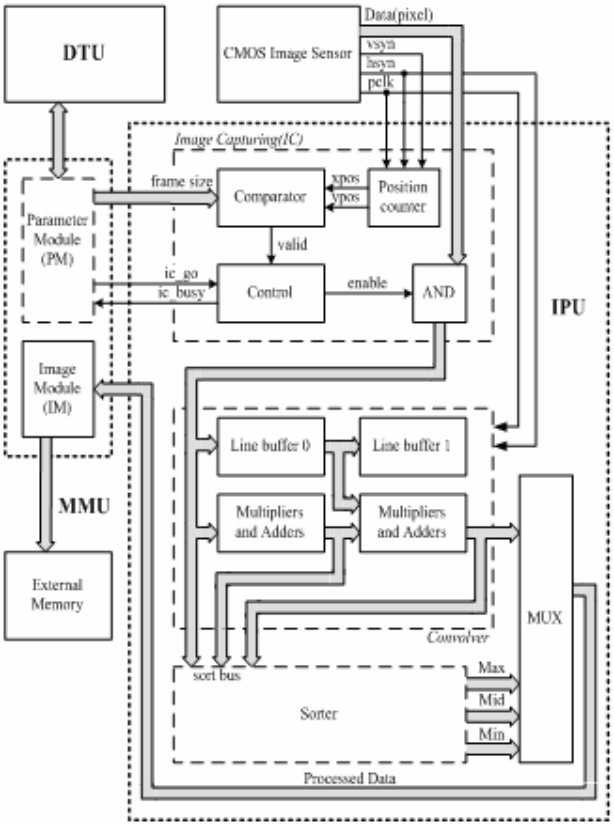


Figure 17. IPU external and internal connections

5. Memory Management Unit and Data Transfer Unit

The remaining two units, Memory Management Unit (MMU) and Data transfer Unit (DTU) are described in this section. MMU consists of two modules, namely, parameter module and image module. Parameter module includes an internal memory for storing the parameter initialization settings. Image module takes care of the object image storing from IPU or the readout form external memory to PC through DTU using IEEE 1284 standard [12]-[14]. Figure 18, shows the connections between MMU, DTU, PC, INU, IPU and external memory.

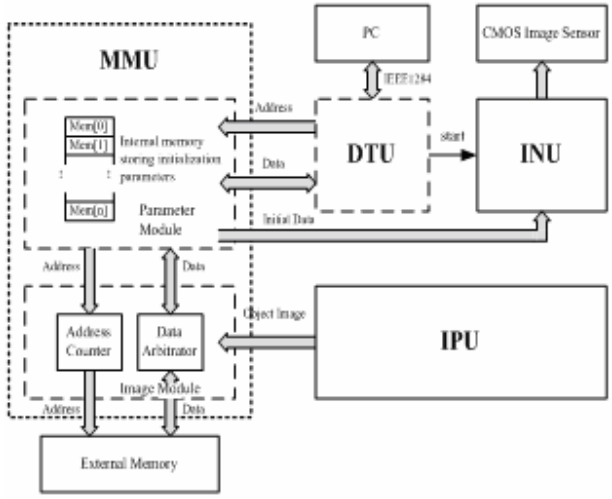


Figure 18. Connection between MMU, DTU, INU and IPU

6. Experiment and Results

The Configuration of CMOS image sensor for this integrated architecture experiment is shown in Figure 19. Its practical circuits and devices connection is shown in Figure 20.

Figure 21, Shows Lena's filtered images through 2-D convolution form the experiment. The result image through high pass filter is hard to be seen or be printed as shown in (d) of Figure 21, so (d) is enhanced for easier to be seen as shown in (e) of Figure 21. Figure 22, applies median filters. Figure 23, applies maximum and minimum filters. Currently the qualities of all the processed images form these experiments are above the average according to the human eye's inspection.

57.8MHz is the maximum clock rate to run this FPGA board, it is estimated about 20 frames(320×240) per second can be achieved under this clock rate.

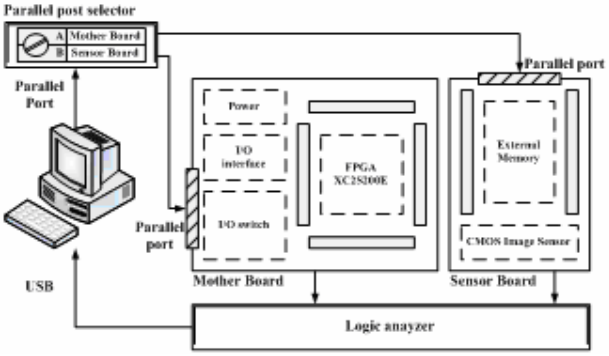


Figure 19. Configuration of FPGA integrated architecture experiment

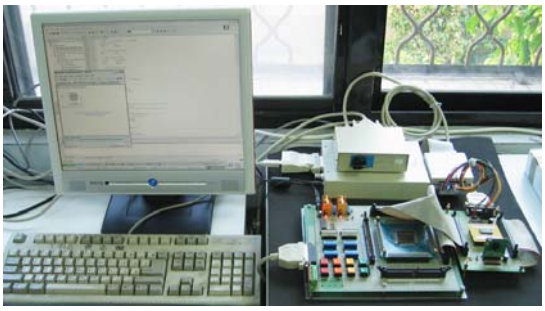
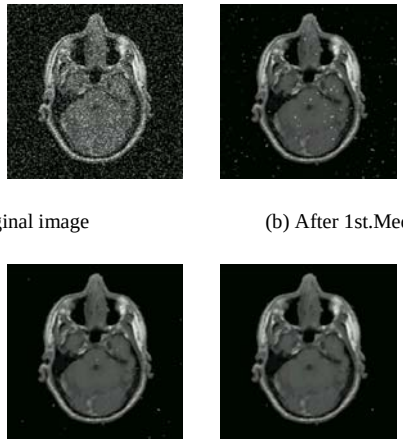


Figure 20. Practical connection of FPGA integrated architecture experiment

(a) Original Image (b) Averaging filter (c) Gaussian filter

(d) High pass filter (e) Enhance from d (f) a plus d

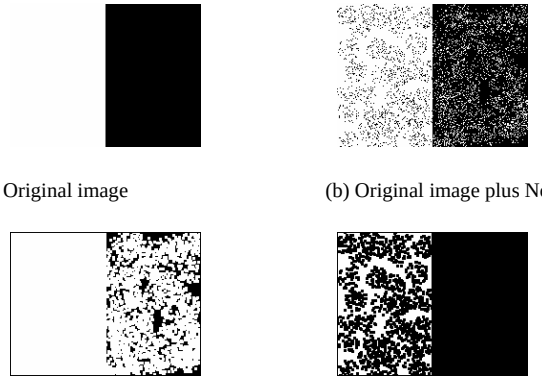
Figure 21.Lena's filtered images though 2-D convolution from this experiment



(a) Original image (b) After 1st.Median Filter

(c) After 2nd Median Filter (d) After 3rd Median Filter

Figure 22. Results from median filter in this experiment



(a) Original image (b) Original image plus Noise

(c) After 1st Maximum Filter (d) After 1st Minimum Filter

Figure.23 Results from maximum filter and median filter in this experiment

7. Concluding Remark

Image capturing, convolution and 2-D sorting were usually done in series. They are now integrated in a FPGA chip, using 60k gate-count out of the total 200k gate-count available in that chip (Spartan-IIE XC2S200E) and operate in 3-stage pipelined. It demonstrates the speed of 20 frames (320×240) per second with high quality images.

After this initial experiment, it is found that further improvements are possible for increasing the operation speed and operating flexibility. The following lists are some examples;

- In this experiment, 2-D sorting is done after all 9 elements in 3×3 window are filled. Sorting can also be done immediately after each element is generated by using bubble sorting. The sorted listing can be stored in a buffer for next processing. In this modified design, convolution and sorting are in parallel operation. It will greatly increase the processing speed.
- Dynamically changing the size of convolution window instead of 3×3 is possible by dynamically presetting a counter that controls the number of shifting in the shift registers used as line buffers.

This integrated image capturing device in FPGA can be independently operated with LCD display or applied in an embedded system as an image accelerator to relieve processor core's burden of extensive software image computing, in addition to the high speed as well as a better image quality.

References

[1] Bosi B., Bois G., and Savaria Y., "Reconfigurable pipelined 2-D convolvers for fast digital signal processing," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 7, Issue: 3, Sept, 1999, pp. 299 -308.

[2] Hyun Man Chang, Sunwoo, and M.H., "An efficient programmable 2-D convolver chip," *ISCAS '98. Proceedings of the 1998 IEEE International Symposium on Circuits and Systems*, vol. 2, June, 1998, pp. 429-432 ,.

[3] Kwan H.-K and Okullo-Oballa T.S., "2-D systolic arrays for realization of 2-D convolution," *IEEE Transactions on Circuits and Systems*, vol. 37, Issue: 2 , Feb, 1990, pp. 267 -233.

[4] Lakshminarayanan G., Venkataramani B., Senthilkumar K.P., and Kottapalli M.S.V.A., "Design and implementation of FPGA based wavepipelined fast convolver," *TENCON 2000. Proceedings* , vol. 3 , Sept, 2000, 212 -217.

[5] Crookes D., Benkrid K., Bouridane A., Alotaibi K., and Benkrid A., "Design and implementation of a high level programming environment for FPGA-based image processing," *Vision, Image and Signal Processing, IEE Proceedings*, vol. 147, Issue: 4 , Aug, 2000, pp. 377 -384.

[6] Benkrid K., Crookes D., and Benkrid A., "Towards a general framework for FPGA based image processing using hardware skeleton," *Parallel Computing* vol. 28, Issue: 7-8, Aug, 2002, pp. 1141-1154.

[7] Bouridane A., Crookes D., Donachy P., Alotaibi K., and Benkrid K., "A high level FPGA-based abstract machine for image processing," *Journal of Systems Architecture* vol. 45, Issue: 10, April, 1999, pp. 809-824.

[8] Bouridane A., Crookes D., Donachy P., Alotaibi K., and Benkrid K., "A high level FPGA-based abstract machine for image processing," *Journal of Systems Architecture* vol. 45, Issue: 10, April, 1999, pp. 809-824.

[9] Maheshwari R., Rao S.S.S.P., and Poonacha P.G., "FPGA implementation of median filter," *Tenth International Conference on VLSI Design*, June, 1997, pp. 523 -524.

[10] Philips Semiconductors: The I2C-bus Specification, Philips Semiconductor, 2000.

[11] Philips Semiconductors: The I2C-bus and how to use it (including specifications), Philips Semiconductors, 1995.

[12] Craig Peacock, Interfacing the Standard Parallel Port, Craig Peacock, 1998.

[13] Craig Peacock, Interfacing the Enhanced Parallel Port (EPP), Craig Peacock, 2002.
[14] Craig Peacock, Interfacing the Extended Capabilities Parallel Port (ECP), Craig Peacock, 2002.

Chi-Jeng Chang received the B.S degree from National Taiwan Normal University, Taipei, Taiwan, R.O.C, and the M.S. degree from the University of Wisconsin-Stout, Wisconsin, U.S.A., in 1996 and 1971, respectively, both in industrial education, with a concentration in electronics and computer hardware.
He was with the Department of Information Engineering, Tamkang University, Taipei, Taiwan, R.O.C, from 1974 to 1980. From 1980 to 2005, he was a professor in the Department of Industrial Education, National Taiwan Normal University, Taipei, Taiwan, R.O.C., Since 2005 he has joined the faculty members in the Department of Computer Science and Information Engineering, Jin Wen Institute of Technology, Taipei, Taiwan, R.O.C. His research interests include electronics, computer architecture, microprocessor applications and VLSI design.

Pei-Yung Hsiao was born in Taiwan, R.O.C., in 1957. He received the B.S. degree in chemical engineering from Tung Hai University, Taichung, Taiwan, R.O.C., and the M.S. and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, R.O.C., in 1980, 1987, and 1990, respectively.
He is currently the President of Aetex Biometric Corporation, Taipei, Taiwan, R.O.C., as well as an Associate Processor in the Department of Electronics Engineering Chang Gung University, Taipei, Taiwan, R.O.C. From August 1990 to February 1998, he was an Associate Processor in the Department of Computer and Information Science, National Chiao Tung University, Hsinchu, Taiwan, R.O.C. His main research interests are VLSI-CAD, piping engineering design automation, fingerprint identification, artificial intelligence, neural network, and expert system application. He has published more than 70 articles in conference record and technical journals.

Zen-Yi Huang received B.S. and M.S. degree in industrial Education with a concentration in electronics and computer hardware, from National Taiwan Normal University, Taipei, Taiwan, R.O.C., in 2002 and 2005, respectively.
He was a teacher at National Tainan Vocational High School for one year in 2005. He is now in military service. His research interests include image processing and VLSI design.