Design of Q-IDEN D Flip-Flop Using RS-latch

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Summary
In this study we design quaternary acting Q-IDEN D flip-flop circuit. First of all, we design thermometer code output circuit, EXOR gate, bias inverter, transmission gate, and binary D flip-flop circuit. Using thermometer code output circuit, EXOR gate, and bias inverter we design multi-valued identity logic circuit, and with multi-valued identity logic circuit and binary D flip-flop we design Q-IDEN and D flip-flop.
Key words:
Quaternary, D-FF, Bias inverters, Transmission gates

Introduction

From Although developing multi-valued device using voltage mode sometimes causes unpredictable output due to transmission time delay, it has the advantage of easy applicability to particular system and less power consumption. When using voltage mode producing the element, which has multiple threshold voltage and is essential for actualizing multi-valued device, was a really difficult problem. But the appearance of Neuron-MOSFETs enabled actualizing multi-valued systems using general voltage mode CMOS technique.

The advantage of multi-valued circuits using Neuron-MOS NMIN, NMAX circuit is that it can be applied in every multi-valued logic value without changing the structure. But the disadvantage of it was long transmission time and large power consumption.

Neuron-MOS which had the similar characteristic with the neuron of human nerve system was suggested by T. Shibata [1] on the early 1990s, and was typically used in the circuit for forming the intelligent network. These Neuron-MOS can be made by adding several input gates and floating gates to the existing MOSFET structure.

K. W. Current [2] suggested voltage mode quaternary CMOS latch circuit using binary CMOS RS latch circuit acting on single threshold voltage.

T. Uemura et al. suggested tertiary D flip-flop circuit using multi-junction surface tunnel transistor and MOSFET, designed tertiary logic gate using voltage mode CMOS technique, and suggested tertiary flip-flop[3].

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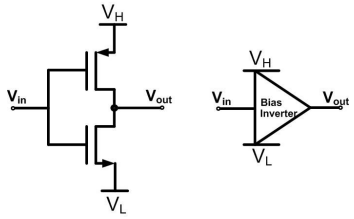
M. Inaba [4] et al. suggested quantizer flip-flop and multi-valued flip-flop, in other words, analog flip-flop using Neuron-MOS CMOS NMIN circuit. Every element used Neuron-MOS and T-gate circuit was designed using CMOS.

In this study we suggested and designed Q-IDEN D flip-flop. Suggested Q-IDEN D flip-flop was designed using Neuron-MOS and occasionally general MOSFET when necessary.

2. Component circuits

2.1 Bias inverter circuit

Bias inverter has the same structure with typical binary inverter but uses the bias power supply V_H and V_L of a specific value instead of V_{DD} and GND. Figure 1 shows the circuit diagram and circuit symbol of bias inverter.



(a) (b)
Fig. 1 Bias inverter: (a) Circuit. (b) Symbol.

The threshold voltage of bias inverter is determined by the bias voltage V_H and V_L as Formula (1) and. V_{out} is determined as Formula (2).

$$V_{TH} = \frac{V_H + V_L}{2} \tag{1}$$

$$V_{out} = \begin{cases} V_L & V_{in} > V_{TH} \\ V_H & V_{in} < V_{TH} \end{cases} \quad (2)$$

Bias inverter works in a same mechanism with typical binary inverter. Bias inverter yields low bias voltage V_L as the output when input voltage V_{in} is higher than the threshold voltage V_{TH}, and yields high bias voltage V_H when V_{in} is lower than V_{TH}. Bias voltage V_H and V_L has quaternary value, and when the difference of the two values becomes an even number threshold voltage V_{TH} can't have the middle value (0.5, 1.5, 2.5) of the quaternary level. Table 1 shows the quaternary truth table of bias inverter and Figure 2 shows the result waveform of the simulation experiment of bias inverter. It is verified that the result waveform of the simulation experiment of bias inverter is exactly identical to the quaternary truth table of bias inverter.

Table 1: Quaternary truth table of bias inverter

V_H	V_L	V_{TH}	BIAS_INV_IN				BIAS_INV_OUT			
3	2	2.5	3	2	1	0	2	3	3	3
3	0	1.5	3	2	1	0	0	0	3	3
2	1	1.5	3	2	1	0	1	1	2	2
1	0	0.5	3	2	1	0	0	0	0	1

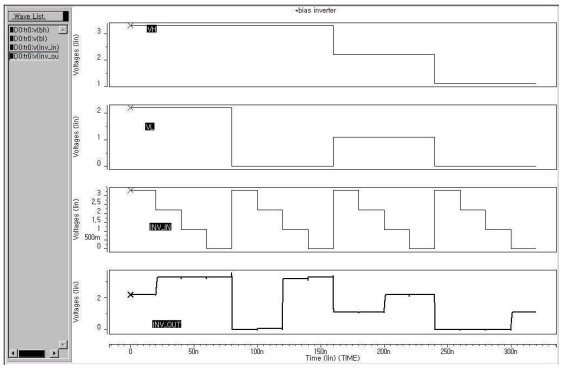
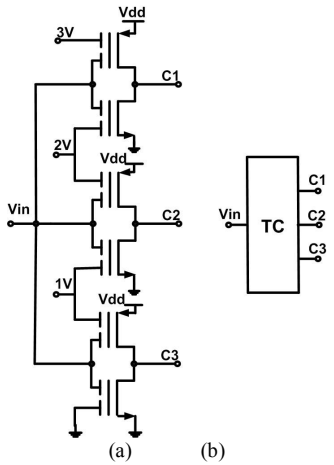


Fig. 2 Quaternary input and output waves of bias-inverter.

2.2 Thermometer code output circuit

Figure 3 is the thermometer code output circuit made up of 3 DLCs. Threshold voltage V_{TH} is 2.5, 1.5, and 0.5, respectively from the top DLC in Figure 3. It outputs binary thermometer code according to the input value of V_{in}. Table 2 simplifies the relationship between the input and the output of thermometer code circuit, and Figure 4 shows the result waveform of the simulation experiment of thermometer code circuit.



(a) (b)

Fig. 3 Thermometer code output circuit.
(a) Circuit.(b) Symbol.

Table 2: Input and output of thermometer code output circuit

	C_1	C_2	C_3
V_0(GND)	3	3	3
V_1	0	3	3
V_2	0	0	3
V_3(VDD)	0	0	0

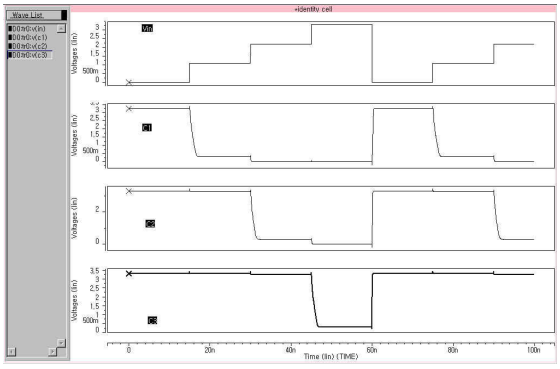


Fig. 4 Input and output waves of thermometer code circuit.

2.3 Quaternary identity logic circuit

Quaternary identity logic circuit works as a buffer and is used in designing quaternary D flip-flop. As shown in Figure 5. Quaternary identity logic circuit is composed of thermometer code circuit, EXOR gate, 2 bias inverters, N-type transmission gate, and P-type transmission gate. When quaternary logic data is entered to input x of

quaternary identity logic circuit, thermometer code value is yielded as the thermometer code circuit, C_1, C_2, C_3, like table 3. C_1 and C_3 go through EXOR and yields PS and C_2 directly transmits to VS. Bias inverter with bias $V_H = 3$, $V_L = 0$, yields 0 for the output when the input is $V_{in} > 1.5$, and yields 3 when $V_{in} < 1.5$.

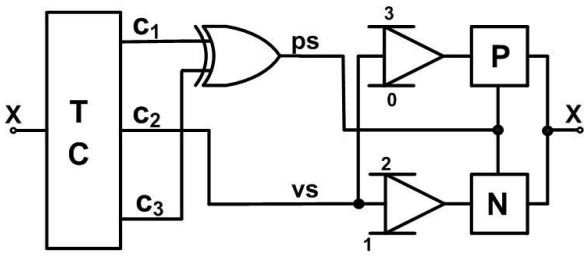


Fig. 5 Quaternary identity logic circuit.

Bias inverter with bias $V_H = 2$, $V_L = 1$, yields 1 for output when input is $V_{in} > 1.5$, and yields 2 when $V_{in} < 1.5$. In the transmission gate, when PS value is 3 the input of N-type transmission gate is transmitted to the output, and when 0 the input of P-type transmission gate is transmitted. The logic value of thermometer code output, PS, VS and output V_{out} according to the quaternary input x, is like it is shown in table 3. Figure 6 shows the result waveform of the simulation experiment of quaternary identity logic circuit.

Table 3: Operation characteristics of quaternary identity logic circuit

x	C_1	C_2	C_3	VS	PS	V_{out}
0	3	3	3	3	0	0
1	0	3	3	3	3	1
2	0	0	3	0	3	2
3	0	0	0	0	0	3

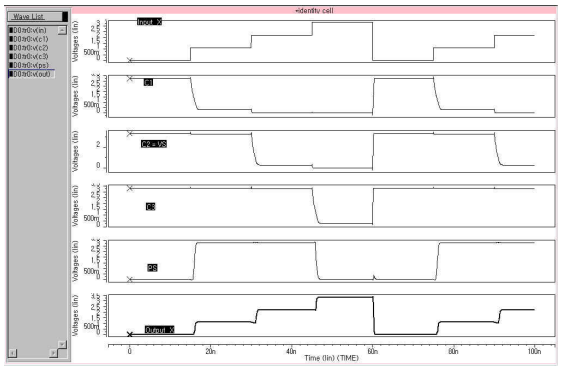


Fig. 6 Quaternary input and output waves of identity logic circuit.

2.4 Binary RS latch circuit

When quaternary Q-IDEN D flip-flop is designed, binary acting RS latch circuit is used to give additional function of flip-flop to quaternary identity logic circuit. The circuit shown in figure 7 is a binary latch circuit using general MOSFETs. The binary latch circuit of figure 7 is a circuit that when CLK input is 3V, output V_{out} is determined by R, S input. Table 4 shows the truth table of RS latch circuit and Fig. 8 shows the result waveform of the simulation experiment of RS latch circuit.

Fig. 7 Binary RS latch circuit.

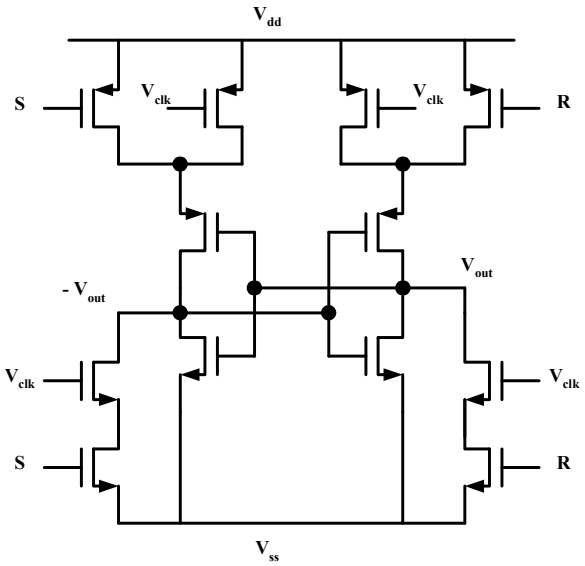


Table 4: Truth table of RS latch circuit

S	R	Q	Q_bar
0	0	status unchanged	status unchanged
0	3	0	3
3	0	3	0
3	3	unusable	unusable

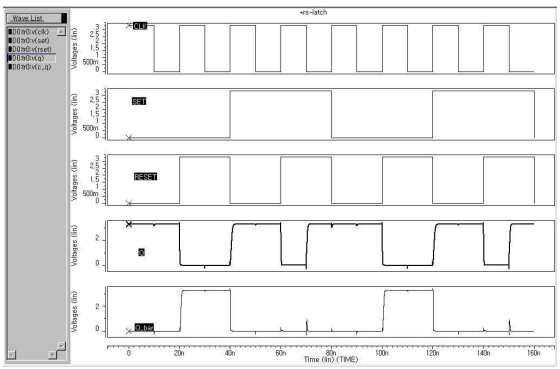


Fig. 8 Input and output waves of RS latch circuit.

3. Designing Q-IDEN D flip-flop

As shown in figure 9. Q-IDEN D flip-flop is composed of binary D flip-flop and multi-valued Identity logic circuit. According to quaternary D input, thermometer code output circuit yields C1, C2 and C3 after converting them to thermometer code, like it is shown in figure 9.

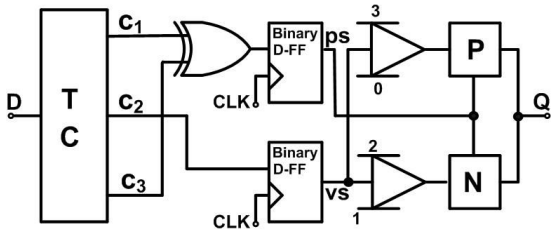


Fig. 9 Q-IDEN D flip-flop.

Table 5: Operation characteristics of Q-IDEN D flip-flop

D	C_1	C_2	C_3	BD1	BD2	VS	PS	Q
0	3	3	3	0	3	3	0	0
1	0	3	3	3	3	3	3	1
2	0	0	3	3	0	0	3	2
3	0	0	0	0	0	0	0	3

The result of C_1 and C_3 gone through EXOR becomes the input of upper binary D flip-flop and get stored as PS. C_2 becomes the input of lower binary D flip-flop and get stored as VS. By using binary flip-flop, total circuit obtains the function of the flip-flop. Bias inverter with $V_H = 3$, $V_L = 0$, yields 0 for output when input is $V_{in} > 1.5$, and yields 3 when $V_{in} < 1.5$. Bias inverter with $V_H = 2$, $V_L = 1$, yields 1 for output when input is $V_{in} > 1.5$, and yields 2 when $V_{in} < 1.5$. When PS value is 3 the input of N-type transmission gate is transmitted to the output, and when 0 the input of P-type transmission gate is transmitted. Eventually, the logic value of output Q and input D become identical. Table 3.12 shows the logic value of thermometer code, PS, VS, and output Q according to input D. Figure 10 shows the result waveform of the simulation experiment of Q-IDEN D flip-flop.

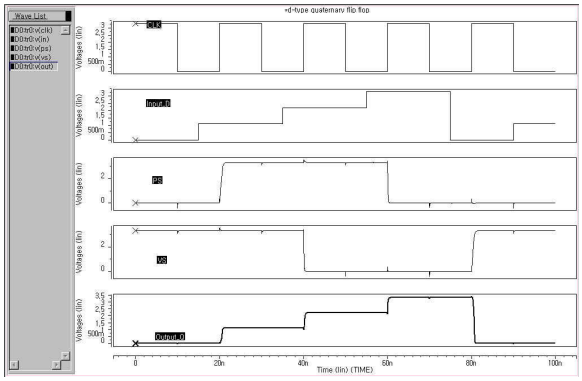


Fig. 10 Quaternary input and output waves of Q-IDEN D flip-flop.

4. Comparision and Discussion

In this chapter, we verified the action condition of quaternary Q-IDEN D flip-flop through HSPICE simulation experiment on 0.35 ㎛ 1-poly 6-metal CMOS process. The Q-IDEN D flip-flop suggested in this report was compared with previously reported multi-valued Flip-flop in the aspect of propagation delay characteristics and power consumption, and it is summarized in table 6. Supply voltage was 3.3V and the logic level 0, 1, 2, and 3 of input and output was 0.0V, 1.1V, 2.2V, and 3.3V, respectively.

Table 6: Comparison of the propagation delay characteristics

Flip-Flop	Author	F (㎛)	S.V. (V)	Propagation Delay(㎱)/P_D
Binary Flip-Flop	Elgamel[5]	0.18	3.3	0.224/19.8 ㎼
	Do[6]	0.18	1.8	0.138/4.7 ㎽
	Sung[7]	0.18	1.5	0.402/47.8 ㎼
	Shin[8]	0.35	3.3	0.427/540 ㎼
Multi-valued Flip-Flop	Current[3]	2	5	2.8/354.8 ㎼
	Inaba(I)[4]	0.6	3.5	420/80 ㎼
	Inaba(II)[4]	0.6	3.5	130/155 ㎼
	Q-IDEN D_FF	0.35	3.3	0.43/138 ㎼

Among the characteristics of binary flip-flop, the power consumption of Do was 4.7 ㎽. This is very much for the power consumption of binary flip-flop. In case of Elgamel, Sung, and Shin it was detected in ㎼ s.

Current suggested quaternary latch circuit using binary CMOS RS latch and proved that propagation delay characteristics was 2.8 ㎱ when power consumption was 354.8 ㎼.

Inaba designed multi-valued using Neuron-MOS, suggested D flip-flop, and proved that in analog D flip-flop propagation delay characteristics was 420 ns when power consumption was 80 ㎼ and in quantize D flip-flop 130 ns when 155 ㎼.
Propagation delay characteristics of the Q-IDEN D flip-flop, suggested in this report, was 0.43 ns when power consumption was 138 ㎼, and it is similar to the propagation delay characteristics of the binary flip-flop.

5. Conclusion

In this study, we suggested and designed Q-IDEN D flip-flop. Suggested Q-IDEN D flip-flop was designed using bias inverter, transmission gate, thermometer code output circuit, and binary RS latch circuit.
Q-IDEN D flip-flop showed 138 ㎼ of power consumption, 0.43 ns of propagation delay, and 59.3fJ of PDP, the better characteristics than previous flip-flops.
The problems occurred during the study, excessive power consumption of Neuron-MOS device circuit and raising the max-sampling frequency, are still remained to be investigated in the future.

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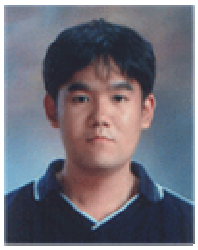

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