Design of Advanced Multiple-Valued D-FF Using Neuron-MOS

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Summary

The proposed two types of multi-valued D flip-flops are NMAX-TG D flip-flop and NMIN-TG D flip-flop A NMAX-TG D flip-flop and a NMIN D flip-flop are composed of the components such as NMAX D flip-flops, NMIN D flip-flops and T-gate circuits. In the simulations, sampling frequencies of NMAX-TG D flip-flop and NMIN-TG D flip-flop are measured around 500 ㎑ and 1 ㎒, respectively. The PDP parameters of NMAX-TG D flip-flop and NMIN-TG D flip-flop are measured to be 28.49nJ and 25.5nJ respectively.
Key words:
NMAX, NMIN, T-gate, D-FF

Introduction

The materialization method of multiple-valued logic element can be categorized by current mode and voltage mode. With the voltage mode, unexpected output can be occurred due to the electric wave delay time but the voltage mode has advantages such as easy to apply for substantial system and low power consumption. In case to use the voltage mode, the production of the element, which has multiple threshold voltage that is the essential for materialization of multiple-valued logic element, was the greatly difficult problem. However, the materialization of multiple-valued logic system by general voltage mode CMOS technology has become possible due to the appearance of neuron-MOS element.

The neuron-MOS, which has similar performance characteristics to human's nervous system, was introduced by T. Shibata [1] in 90's and mainly used as the circuit for intelligence network construction. Such neuron-MOS can be produced by addition of number of input gates and floating gates into the exist MOSFET structure. This element can control the threshold voltage by transmission of many input gate signal voltage to floating gate.

K. Kondo [2]etc. proposed the circuits of MIN, MAX, NMIN and NMAX based on neuron-MOS which can compare the multiple-valued variable value using down-literal circuit, analogue inverter, multiple-valued voltage comparison device, transmission gate.

K. W. Current [3] proposed the voltage mode 4-valued CMOS latch circuit using binary CMOS RS latch circuit which performs by single threshold voltage.

M. Inaba [4]etc. proposed the multiple-valued flip-flop, that is analogue flip-flop and quantizer flip-flop using neuron-MOS-CMOS NMIN circuit. Every element used neuron-MOS and T-gate circuit was designed by using CMOS.

In this research, two types of multiple-valued D flip-flop was proposed and designed. The proposed NMAX-TG D flip-flop and NMIN-TG D flip-flop was designed by addition of T-gate circuit in order to improve the performance characteristics of NMAX D flip-flop and NMIN D flip-flop. Every circuit was designed using neuron-MOS and general MOSFET was used as a subsidiary as occasion demands. NMAX-TG D flip-flop and NMIN-TG D flip-flop have a advantage which can be used in every multiple-valued logic without structural change.

2. Multiple-valued logical function and neuron-MOS

2.1 Neuron-MOS[2],[4]

Neuron-MOS element is a modified element of existed MOSFET element and it has many threshold voltage, that is, it can materialize the multi threshold voltage. Figure 1 presents N channel neuron-MOS transistor structure.

In the figure 1, the different part from the general MOSFET is the gate structure. It has multiple gate instead of single gate and it includes floating gate. Therefore, neuron-MOS element permissive with many input voltage.

According to the permissive voltage of multiple input gate, the strength of voltage which transmit to floating gate can be varied, so the threshold voltage of the element also can be changed by input voltage.

The equivalence circuit of 2-input P channel neuron-MOS and N channel neuron-MOS can be presented as figure 2. To achieve two gate input structure in one element, two

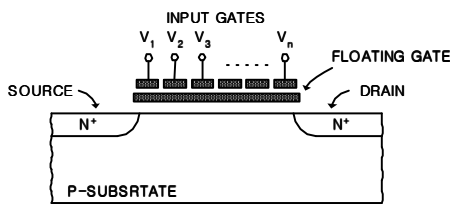capacitor connect with parallel connection between floating gate and two input gate.

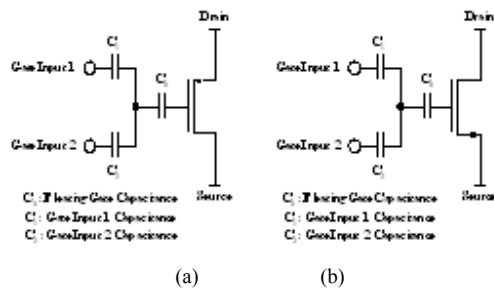
Fig. 1 Basic structure of N-channel Neuron MOS.

(a)   (b)

Fig. 2 The equivalence circuits of 2-input Neuron MOS.

(a) P channel Neuron MOS. (b) N channel Neuron MOS.

2.2 Analogue inverter[4]

Analogue inverter for the performance of NOT function of analogue value is very valuable not only to analogue circuit but also to multiple-valued logic circuit.

Analogue inverter is composed by P channel which has two input gate and neuron-MOS of N channel as shown in the figure 3.

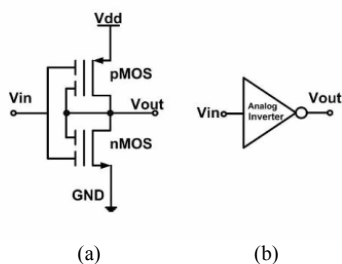
(a)   (b)

Fig. 3 Analog inverter. (a) Circuit. (b) Symbol.

V_{in} and V_{out} represents voltage of input terminal and output terminal.

Analogue inverter has capacitor return system from output terminal to floating gate via bias terminal.

3. Advanced multiple-valued D flip-flop

In case of multiple-valued NMAX D flip-flop circuit, when the input condition matched to CLK = 0, the present output condition of flip-flop should be keep the same constantly, and in case of multiple-valued NMIN D flip-flop circuit, when the input condition is matched to CLK = 3, the present output condition should be keep the same constantly. However, in reality, it is occurred that the present output logic voltage may not keep constantly and malfunction would be happened.

3.1 Transmission gate circuit

Transmission gate is a circuit for performing of transmission operation. As figure 9, transmission gate can be composed using N channel MOSFET and P channel MOSFET. The transmission gate in figure 4(a) is N type which input signal C_i transmit to output when transmission control variable B is V_{DD}. The transmission gate in figure 4(b) is P type which input signal C_i transmit to output when transmission control variable B is 0V.
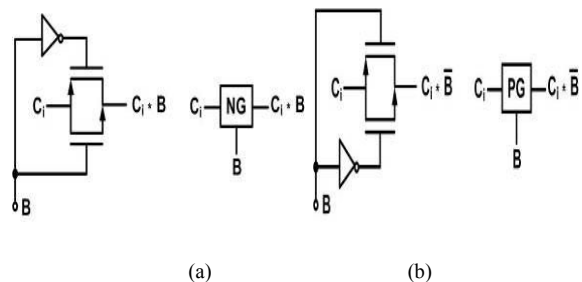

(a)   (b)

Fig. 4 Transmission gate. (a) N-type. (b) P-type.

Figure 5 presents the combination form of N type transmission gate and P type transmission gate. Transmission factor C_1 is input transmission factor for P type transmission gate and transmission factor C_2 is input transmission factor for N type transmission gate. The transmission control variable B is permitted to N channel MOS gate of N type transmission gate and simultaneously, permitted to P channel MOS gate of P type transmission gate.
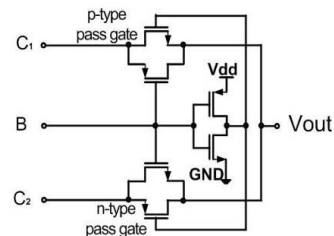

Fig. 5 Transmission gate circuit combined with N-type and P-type.

As well as, the inverter output which reverse the value of control variable B is permitted to P channel MOS gate of N type transmission gate and permitted to N channel gate of P type transmission gate respectively.

In figure 5, if the value of transmission control variable *B* is 0V, P type transmission gate circuit would operate and C_1 will be output at V_{out}. If the value of *B* is 3V, N type transmission gate circuit would operate and C_2 will be output at V_{out}. Table 1 presents the output value of transmission gate circuit according to the value of control variable B.

Table 1: Input and output voltage of transmission gate circuit

P type transmission gate input	N type transmission gate input	*B*	
C_1	C_2	0V	C_1
		3V	C_2

In figure 5, the voltage of 0V, 1.1V, 2.2V, 3.3V were input to C_1 with changes by periods and constant voltage, 1V, was input to C_2. The figure 6 presents the simulation result wave by control variable B.
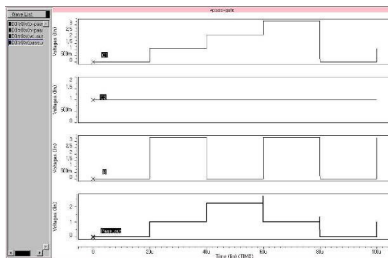

Fig. 6 Quaternary input and output waves of transmission gate circuit.

When the value of control variable *B* is 0, P type transmission gate would operate and the output of value of C_1 can be confirmed and when the value of control variable B is 3, N type transmission gate would operate and the output of value of C_2 can be confirmed.

3.2 Neuron MOS 4-valued T-gate circuit

T-gate function is one of the important functions for multiple-valued logic signal treatment. 4-Valued T-gate function is defined as formula (1).

$$T(P_0, P_1, P_2, P_3; x) = \begin{cases} P_0 & if \quad x = 0 \\ P_1 & if \quad x = 1 \\ P_2 & if \quad x = 2 \\ P_3 & if \quad x = 3 \end{cases}$$

Where, $P_0, P_1, P_2, P_3, x \in \{0,1,2,3\}$ (1)

T-gate function is that the one of the 4 inputs, P_0, P_1, P_2, P_3, would transmit to output according to the value of critical input x=0, 1, 2, 3. T-gate circuit is the circuit for actualizing of T-gate function.

T-gate circuit can be composed with CMOS transmission gate and DLC. Figure 7 represents the neuron MOS 4-valued T-gate circuit. In the T-gate circuit, transmission gate is N type transmission gate. The critical voltages of DLC circuit D_0, D_1, D_2 in 4-valued T-gate circuit are formula (2), (3), (4) respectively.
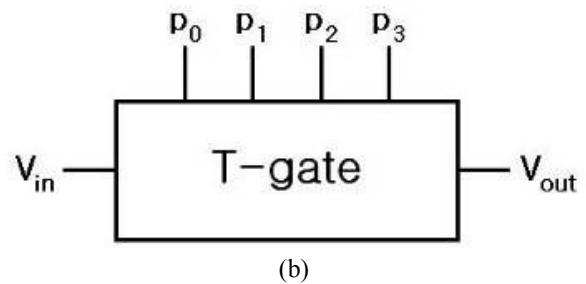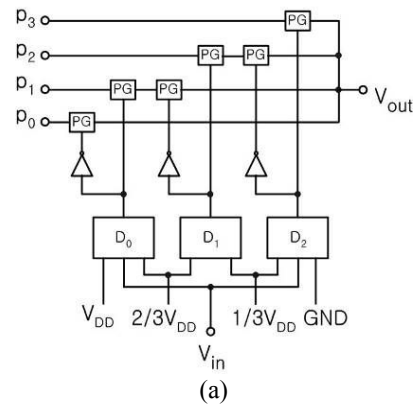

(a)

(b)

Fig. 7 Quaternary T-gate. (a)Block diagram. (b)Symbol.

$$V_{TD0} = V_{DD} - \frac{V_{DD} + (2V_{DD}/3)}{2}   (2)$$

$$V_{TD1} = V_{DD} - \frac{(2V_{DD}/3) + (V_{DD}/3)}{2}   (3)$$

$$V_{TD2} = V_{DD} - \frac{(V_{DD}/3)}{2}   (4)$$

According to the relationship between input voltage V_{in} and critical voltage V_{TDn} (n=0, 1, 2), one of the P_0, P_1, P_2, P_3 input would transmit to output V_{out}. The relationship between input and output in T-gate can be arranged as formula (5).

$$V_{out} = \begin{cases} P_0 & if & V_{in} \leq V_{TD0} \\ P_1 & if & V_{TD0} \leq V_{in} \leq V_{TD1} \\ P_2 & if & V_{TD!} \leq V_{in} \leq V_{TD2} \\ P_3 & if & V_{TD@} \leq V_{in} \end{cases} \quad (5)$$
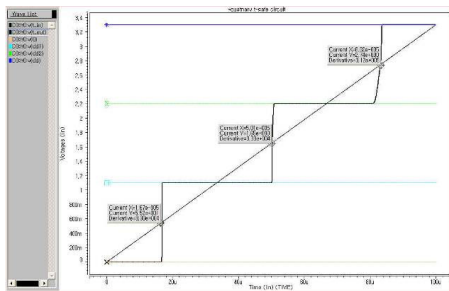

Fig. 8 Input and output waves of T-gate circuit.

It is confirmed that the operation of 4-valued T-gate circuit in figure 7, and figure 8 presents the verification result of T-gate circuit.

As a result of T-gate circuit simulations of figure 8, in the waves, it can be confirmed that when input voltage V_{in} is smaller than critical voltage V_{TD0} = 0.5V, output V_{out} would be P_0 =0V, when input voltage V_{in} is bigger than critical voltage V_{TD0} = 0.5V and smaller than critical voltage V_{TD1} = 1.5V , output V_{out} would be P_0 = 1V, when input voltage V_{in} is bigger than critical voltage V_{TD1} = 1.5V and smaller than critical voltage V_{TD2} = 2.5V, output V_{out} would be P_2 = 2V, and when input voltage V_{in} is bigger than critical voltage V_{TD2} = 2.5V, output V_{out} would P_0 = 3V.

3.3 NMAX-TG D FF and NMIN-TG D FF

Figure 9 shows advanced flip-flop circuit which is created to add T-gate in multiple-valued NMAX D flip-flop. Figure 10 presents advanced flip-flop circuit which is created to add T-gate in multiple-valued NMIN D flip-flop.
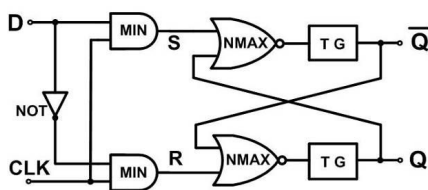

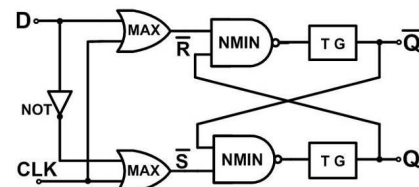Fig. 9 NMAX-TG D flip flop block diagram.

Fig. 10 NMIN-TG D flip flop block diagram.

As figure 7, multiple-valued NMAX D flip-flop and R-S latch circuit output of multiple-valued NMIN D flip-flop are connected to T-gate circuit input voltage terminal V_{in}. T-gate transmission signal input terminal P_0, P_1, P_2, P_3 are connected to each logic level voltage 0V, 1V, 2V, 3V directly. In the composition diagram of multiple-valued NMAX-TG D flip-flop in figure 9 and multiple-valued NMIN-TG D flip-flop in figure 10, the condition of terminal connection for P_0, P_1, P_2, P_3 were omitted.

In the multiple-valued NMAX-TG D flip-flop and NMIN-TG D flip-flop, because the T-gate circuit correct to accurate logic signal voltage size over again and output the change of voltage size which generated when the signal passing the analogue inverter and transmission gate in return loop process, the output signal voltage correspond accurately to the value of the fact table of multiple-valued D flip-flop.

The performance of Multiple-valued NMAX-TG D flip-flop circuit in figure 9 is confirmed and the confirmed results are presented in figure 11. The performance of Multiple-valued NMAX-TG D flip-flop circuit in figure 10 is confirmed and the confirmed results are presented in figure 12.
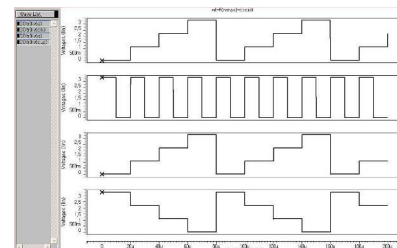

Fig. 11 Input and output waves of NMAX-TG D flip flop.

In the input and output wave of confirmed result, it can be confirmed that the performance of multiple-valued NMAX-TG D flip-flop circuit and the performance of multiple-valued NMIN-TG D flip-flop circuit are correspond accurately to value of the fact table of multiple-valued D flip-flop.
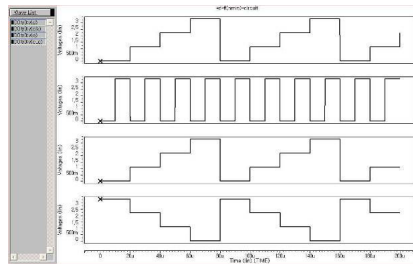
Fig. 12 Input and output waves of NMIN-TG D flip flop.

4. Comparison and Investigation

Table 2 represents the comparison of proposed multiple-valued NMAX-TG D flip-flop and multiple-valued NMIN-TG D flip-flop in the point of existed multiple-valued flip-flop, characteristics of electric wave delay and power dissipation. 3.3V of voltage is used and logic level 0, 1, 2, 3 of input and output use voltage 0.0V, 1.1V, 2.2V, 3.3V.

Table 2: Comparison of the propagation delay characteristics

Flip-Flop classification	Author	FF	Propagation Delay(ns)/P_D
Binary Flip-Flop	Elgamel[5]	D	0.224/19.84 μW
	Do[6]	D	0.138/4.7 mW
	Sung[7]	D	0.402/47.8 μW
	Shin[8]	D	0.427/540 μW
Multi-valued Flip-Flop	Current[3]	D	2.8/354.8 μW
	Inaba(I)[4]	D	420/80 μW
	Inaba(II)[4]	D	130/155 μW
	NMAX-TG D_FF	D	32.2/890 μW
	NMIN-TG D_FF	D	29.0/880 μW

Current proposes value 4 latch circuit using binary CMOS RS latch and shows 2.8 ns of electric wave delay time when the power dissipation is 354.8 μW. Inaba designed multiple-valued gate using neuron MOS, and proposed D flip-flop. In case of analogue D flip-flop, when the power dissipation is 80 μW, the electric wave delay time shows 420 ns and in case of quantizer D flip-flop, when the power dissipation is 155 μW, the electric wave delay time shows 130 ns.

The proposed electric wave delay time of NMAX-TG D flip-flop and NMAX-TG D flip-flop in this research are 32.2 ns and 29 ns respectively when the power dissipation is approximately 880 μW. Especially, electric wave delay time of Q-IDEN D flip-flop is 0.43 ns when the power

dissipation is 138 μW. It shows similar characteristic with electric wave delay of binary flip-flop.

5. Result

In this research, two types of NMAX-TG D flip-flop and NMIN-TG D flip-flop were proposed and designed.

The result for the simulation of proposed circuit showed that NMAX-TG D flip-flop and NMIN-TG D flip-flop present sampling frequencies up to 1 MHz. So it represented the more than 10 times faster sampling speed than analogue flip-flop and quantizer flip-flop in Inaba's recent research.

The power dissipation of NMAX-TG D flip-flop and NMIN-TG D flip-flop was measured as 880 μW and the electric wave delay time was measured as 29 ns, therefore, the value of PDP, Power dissipation-Delay time Product, presented as 25.5pJ.

From the result of that dissipation power of NMAX-TG D flip-flop and NMIN-TG D flip-flop was too big and the maximum sampling frequency was too low, a problem is deduced.

The excessive power dissipation problem of neuron-MOS element circuit and to increase maximum sampling frequency, which are the problems produced during this research, would be the our future research task.

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