A New Temperature Compensation Method for a 2.5 GHz Integrated VCO

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Summary:
A 2.5 GHz fully integrated voltage controlled oscillator (VCO) for wireless application has been designed in a 0.35µm CMOS technology. A method for compensating the effect of temperature on the carrier oscillation frequency has been presented in this work. We compare also different VCOs topologies in order to select one with low phase noise, low supply sensitivity and large tuning frequency. Good results are obtained with a simple NMOS –Gm VCO. This proposed VCO has a wide operating range from 300 MHz with a good linearity between the output frequency and the control input voltage, with a temperature coefficient of -5 ppm/°C from -20°C to 120°C range. The phase noise is about -135.2dBc/Hz at 1MHz from the carrier with a power consumption of 5mW.

Key words:
Radiofrequency, VCO, CMOS process, compensated temperature, phase noise.

1. Introduction

The demand for high speed wireless data communication has been increasing tremendously [1]. Wireless applications typically require VCO's having low power consumption, low phase noise, small size and low cost. The size, the cost requirements and the low phase noise make an integrated oscillator in a standard CMOS process with an on-chip resonance LC tank, a good choice [2, 3]. Rings oscillators have poor phase noise performance disqualifies them in many of today's wireless applications [4]. In the recent years fully integrated cross coupled voltage controlled LC tank oscillators received attention [1-6]. The desirable properties of a VCO depend also on the PLL application, low drift with temperature and spectral purity with sinusoidal output [7].
A general LC_VCO model is shown in Fig.1 where inductance L and capacitance C represent a parallel resonance tank and Rp is the parasitic resistance of L and C. In order to compensate losses resulting from Rp, a negative resistance is implemented by means of active components like CMOS transistors [8].
The VCO oscillation frequency is controlled by means of varactor acting on control voltage V_{tune}. The aim is having the ratio between the maximum and the minimum capacitance (C_{max} and C_{min} respectively) superior to two. There are various options available to RF designers for tuning varactor elements in silicon CMOS technology [8].

For a given voltage controlled, temperature variation may introduce a significant drift in the output frequency, resulting in an operation out of the channel frequency range. Efficient compensation is then required to ensure a proper operation of the transceiver system [9]. In recent researches, the temperature compensation is studied for ring oscillators [7], [9] and for LC oscillators with Kocer and al. in [10]. In this work, we purpose a new method for compensating the effect of temperature on the carrier oscillation frequency. This method circuit uses only PMOS transistor without resistance.

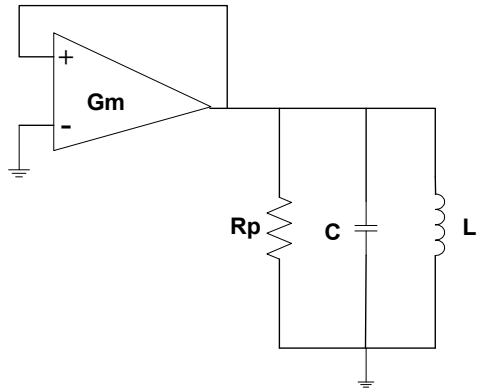

Fig. 1 Oscillator LC model

The Capacitance - Voltage characteristic of PMOS transistor with drain, source and bulk connected together is detailed in section II. Temperature effects are studied in section III. Section IV describes the design of the VCOs. Simulation results of tuning frequency range and sensitivity supply voltage are discussed in section V. The comparison of different topologies regarding phase noise is presented in section VI. Section VII presents the conclusion.

2. MOS Varactor

Different alternatives built on the basic MOS structure have been explored in order to realize varactors with the highest possible quality factor [8]. Moreover, Andreani and Mattison presented a discussion of the different MOS varactors for RF applications [11], [12].
We consider only PMOS transistors, for reducing the bulk effect [12].
Fig.2.(a) shows a varactor topology with a PMOS

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transistor witch the drain, source and bulk are connected together (denoted D=S=B) to form one node of the capacitor. This topology has a capacitance that does not vary monotonically, because the device can operate in accumulation, depletion and inversion mode [12].
In both strong inversion and accumulation region the value of the MOS capacitance C_{mos} is equal to C_{ox} which it is given by

$$C_{ox} = \frac{\varepsilon_{ox} S}{t_{ox}} \quad (1)$$

Where, S and t_{ox} are, respectively, the channel area and the oxide thickness.
In the other regions such as, depletion, weak and moderate inversion, there are few mobile charge carriers at the gate oxide interface which causes a decrease of the capacitance C_{mos} of MOS device [12].
We present in the following two different methods to characterize the PMOS capacitance depending on the voltage tuning:

- The first method consists in polarizing the transistor by a sinusoidal voltage of low amplitude (V_m = 10mV) and of frequency freq = 1GHz, applying the controlled voltage V_{tune} (Fig.2.(a)). We use the following expression to calculate the capacity of transistor PMOS.

$$C_{mos} = \frac{I_m}{2\pi \text{freq}} \quad (2)$$

Where, I_m is the amplitude of the current crossing the PMOS transistor.

- The second method consists in using S_parametrs [13] as standard of simulation which makes the possibility to calculate the impedance Z_{in} at any input circuit (Fig.2.(b)). C is a capacitance of connection and L is a shock inductor.

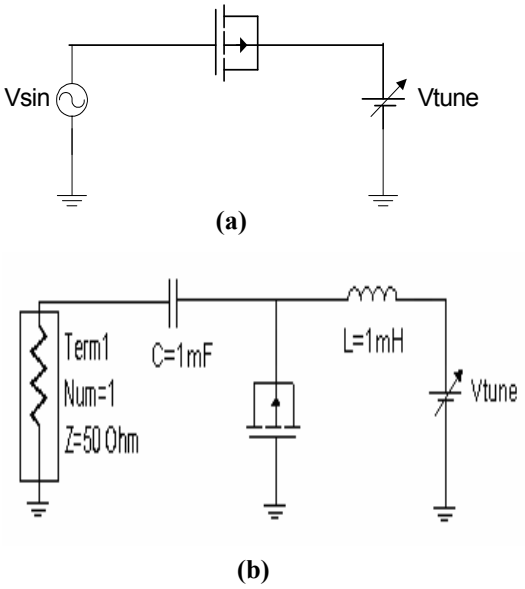

Fig.2 Different methods for characterizing the PMOS capacitance
(a) Small signal (b) S_parameters

The impedance Z_{in} is given by :

$$Z_{in} = R + \frac{1}{j2\pi f_0 C_e} \quad (3)$$

Where, f_0 is the operating frequency, in this case f_0 is equal to 2.5GHz. C_e is the equivalent capacitance of C_{mos} parallel to C, when the value of C is more important to C_{mos} then C_e=C_{mos}
In fact, the equivalent capacity of transistor PMOS is given by :

$$C_{mos} = -\frac{1}{2\pi f_0 \text{imag}(Z_{in})} \quad (4)$$

By varying the control voltage Vtune, the PMOS capacitance varies simulation results are shown in Fig.3.
The proposed circuit has been designed and simulated by ADS in 0.35µm CMOS process. In order to obtain important value of capacitance, we have chosen the width of the PMOS W=1000um and their length L=0.5um.
Fig.3. shows similar characteristics C-V of PMOS resulting from the two different methods for evaluation of the equivalent PMOS capacitance (Fig.2). These characteristics show three different regions of operation of the transistor PMOS ; accumulation region for $V_{tune}<V_{th}$, depletion region for $V_{tune}<|V_{th}|$ and inversion region for $V_{tune} \geq |V_{th}|$.

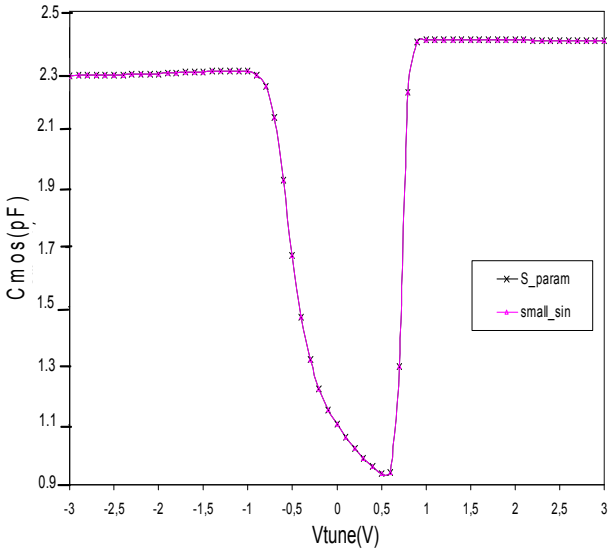

Fig. 3 C-V characteristic of PMOS (L=0.5µm, W=1000µm) resulting with two different methods

According to Fig.3, PMOS capacitance is varying from C_{min}= 0.93pF to C_{max}=2.3pF. The ratio C_{max}/C_{min} is higher than two. Such a rather low value is caused by overlap capacitances between G and D-S, which increasing by more than half the value of C_{min} [4].

3. Temperature compensation

The temperature variation may introduce a significant drift in the output frequency. An efficient compensation

is necessary, for that we propose a new method for the compensating the temperature effect. Let us consider PMOS transistor which the drain, source and substrate are connected together to controlled voltage V_{tune}. While varying the temperature, we obtain the characteristic capacity-voltage (C-V) according to the temperature shown in Fig.4. We note that by varying temperature the equivalent capacity of the PMOS is constant in the both region of operations; accumulation and strong inversion. While in the other mode of operations, the capacity varies differently according to the temperature. If the transistor functions in the mode of depletion (tuning voltage varies from -1.1 to -0.45V), the increase in the temperature involves the reduction in PMOS capacitance. However, if the transistor functions in the moderate inversion region (tuning voltage varies from 0.45 to 1.1V), the increase of temperature causes the increase of PMOS capacitance. According to these results, we purpose to put two PMOS in head-digs for decreasing the effect of the temperature on the capacitive behavior of PMOS. Indeed, the tuning voltage varies positively for one of PMOS and negatively for the second PMOS. Consequently, the increase in the temperature involves the increase in the capacity of one PMOS and the reduction in the capacity of the other PMOS thus the equivalent capacity of two PMOS is almost constant according to the temperature, if the tuning voltage varies [-1.1, -0.45V] and [0.45, 1.1V]. This result is shown in Fig.5.

We calculate the sensitivity temperature of PMOS capacitance by using the sensitivity expression of capacitance at nominal temperature experiment in (ppm/°C), defined by

$$\frac{1}{C_0}\frac{\partial C}{\partial T} \qquad (5)$$

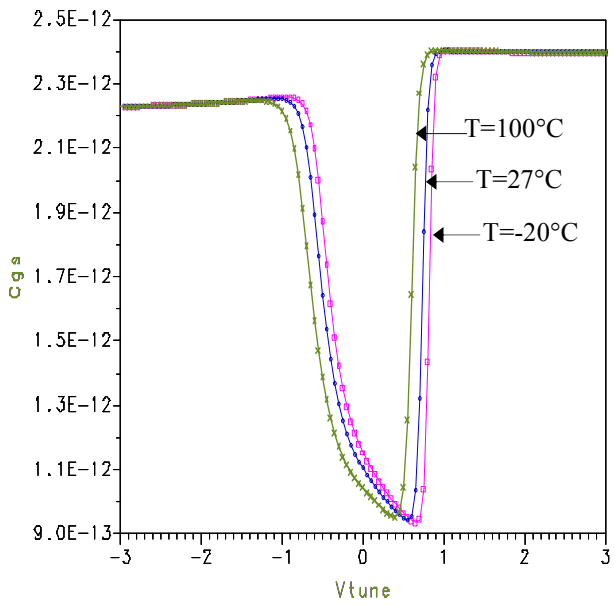

Fig.4. Simulated C-V characteristic of a PMOS (L=0.5µm, W=1000µm) according on temperature

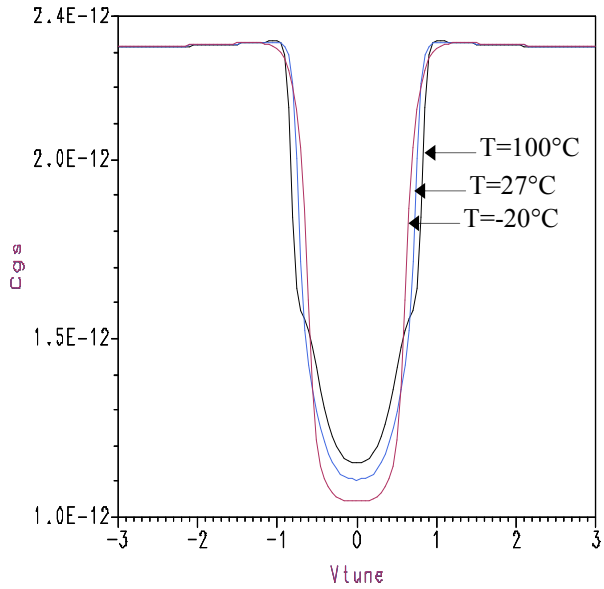

Fig.5. Simulated C-V characteristic of two PMOS put digs-head according on temperature

Table.1, summarizing the results, shows the importance of two PMOS put at the head-digs to decrease the effect of the temperature on the PMOS capacitance.

Table1: Temperature effects on PMOS capacitance

		depletion	Weak inversion	Moderate inversion
$\frac{1}{C_0}\frac{\partial C}{\partial T}$ (ppm/°C)	PMOS	- 1345	- 697	5038
	2PMOS	-813	-1128	2149

4. VCO design

A standard approach for differential VCOs is the use of cross-coupled transistors to generate a negative resistance. This negative resistance should be enough to overcome the equivalent parallel resistance of the VCO tank circuit to generate the desired oscillation. These VCO circuits are known as –Gm LC-tank VCOs [8]. The complementary –Gm oscillator circuit is the result of using both PMOS and NMOS cross coupled pairs in parallel to generate the negative resistance. A simple NMOS oscillator structure consists only in NMOS cross coupled pairs to generate the negative resistance. A number of CMOS –Gm LC VCOs has been reported in the literature [1], [8], [14].

The negative resistance generated by NMOS cross coupled pair is equal to the opposite of the inverse of the transconductance g_m. In fact the size W/L of the cross coupled NMOS, is chosen to fulfill the condition given by the following relation:

$$g_m > \frac{1}{Rp} \qquad (6)$$

Fig.6 shows the schematic view of the complementary –Gm VCO's. It is a standard symmetric CMOS VCO

architecture, where transistor M6 provides the bias current. Transistors M1, M2, M3 and M4 form the negative resistance compensating the VCO losses. The sizes of their length are chosen a minimal value process in order to minimize the flicker noise [7].
Inductors L1 and L2 have a same value of L equal to 1nH. In fact their integration is realised of metal coils with octagonal geometry.
C1 and C2 are variable capacitors in the tank and it is typically a varactor whose capacitance is adjustable by an external voltage. This method allows frequency tuning of the oscillation.
The expression of oscillation frequency is defined by

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad (7)$$

Where, C is the some of the varactor capacitance and the parasitic capacitance C_{gs}, C_{gd} of the pair cross coupled transistors NMOS and PMOS.
Fig. 7 shows the schematic of the simple NMOS –Gm VCO.

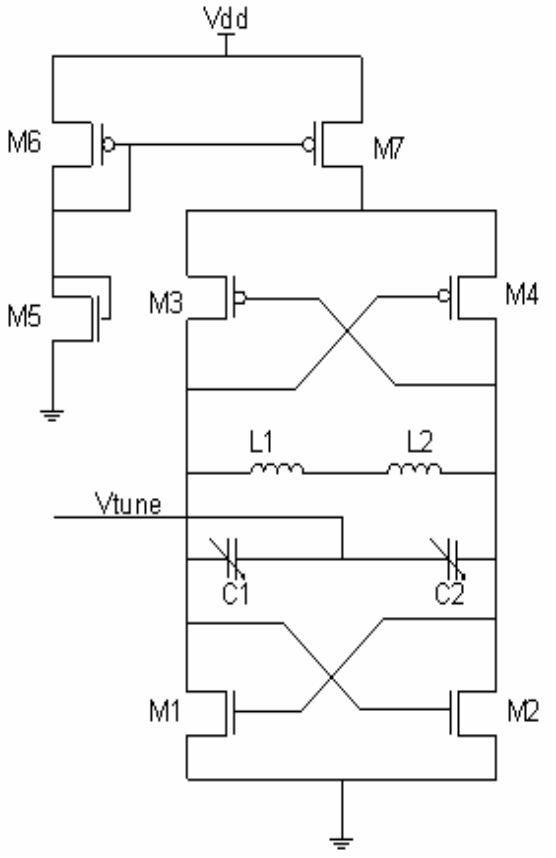

Fig.6. CMOS complementary – Gm oscillator

We present the simulated results of four different structures of –Gm VCOs:
- VCO1 is the complementary –Gm VCO (Fig.6) with the simple PMOS varactor (Fig.8).
- VCO2 is the complementary –Gm VCO (Fig.6) with the simple PMOS varactor (Fig.9).
- VCO3 is VCO2 without current source.
- VCO4 is the simple NMOS VCO (Fig.7) using the composed PMOS varactor for compensating temperature effects (Fig.9).

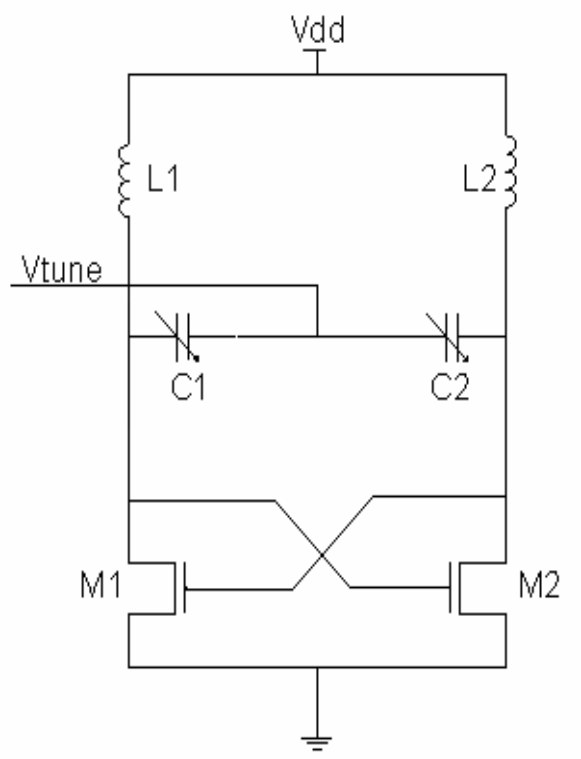

Fig.7. Simple NMOS VCO

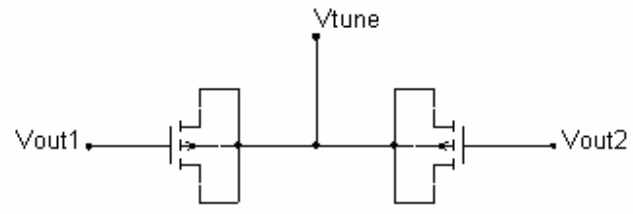

Fig.8. Simple PMOS varactor

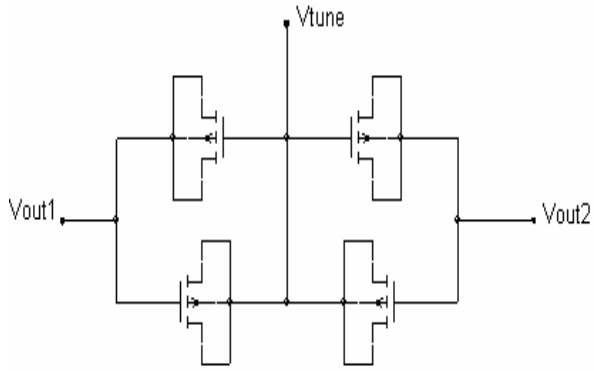

Fig.9. Composed PMOS varactor for compensating temperature effect

Table.2 presents the device scaling of components in the VCO's.

Table 2: Components device scaling (W/L, µm) of VCOs

Structure	M1, M2	M3, M4	M5	M6, M7	Varicaps
VCO1	5/0.35	15/0.35	5/0.35	10/0.35	2020/0.5
VCO2	5/0.35	15/0.35	5/0.35	10/0.35	1030/0.5
VCO3	5/0.35	15/0.35	--	--	1000/0.5
VCO4	15/0.35	--	--	--	960/0.5

These VCOs generate a center frequency fc; we calculate the sensitivity frequency to ward temperature by using this equation:

$$S = \frac{1}{fc}\frac{\partial fc}{\partial T} \qquad (8)$$

Fig.10 shows the deviation of frequency along with the drift of temperature, of –Gm VCOs and the results are summarizing in table.3.

Table 3: Temperature coefficient of VCOs

Structure	VCO1	VCO2	VCO3	VCO4
S_T (ppm/°C)	357	-20	-22.9	-5.8

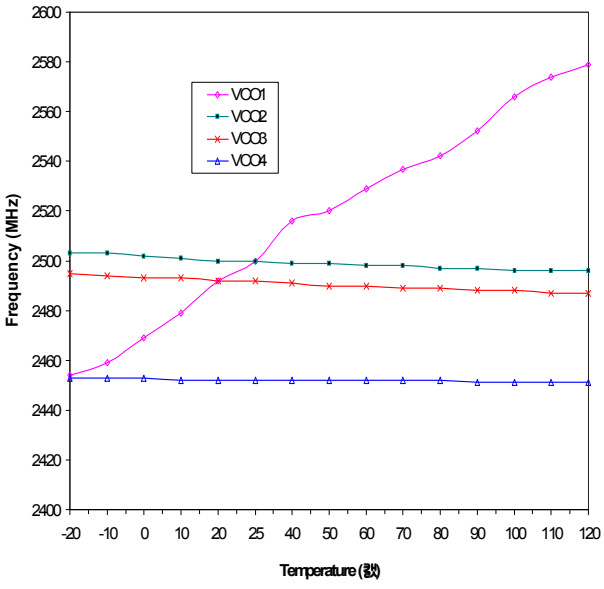

Fig.10. Characteristics of the frequency

The structure of VCO4 presents the lowest temperature coefficient. The operating frequency has a temperature coefficient of 5.8 ppm/°C in the -20 to 120°C range. Comparing this result with the one presented in [7], [9] and [15] where the temperature coefficients are 86 ppm/°C, 73 ppm/°C and 126 ppm/°C, respectively. In fact, the proposed composed PMOS varactor is the best choice for compensating the temperature effect.

5. Tuning frequency and supply sensitivity

The proposed circuit has been designed and simulated by ADS based on 0.35µm CMOS process. Fig.11 shows the tuning characteristics of the proposed VCOs which can operate linearly for a tuning voltage range form -0.6 to 0.6V.

The supply voltage is varying along the time, thus the study of the sensitivity of oscillation frequency is necessary. For a given control voltage 0V and the varying supply voltage from 2.1 to 2.9 ranges for VCO1, VCO2, VCO3 and from 1.1 to 1.9 for VCO4, we evaluate the frequency of VCOs. Fig.12 shows the drift of frequency by varying the supply voltage.

The results are summarized in table.4, it is clear that the VCO4 has the lowest sensitivity supply voltage. The tuning frequency of the VCO1, VCO2, VCO3 and VCO4 are 327, 333, 261 and 219MHz/V, respectively.

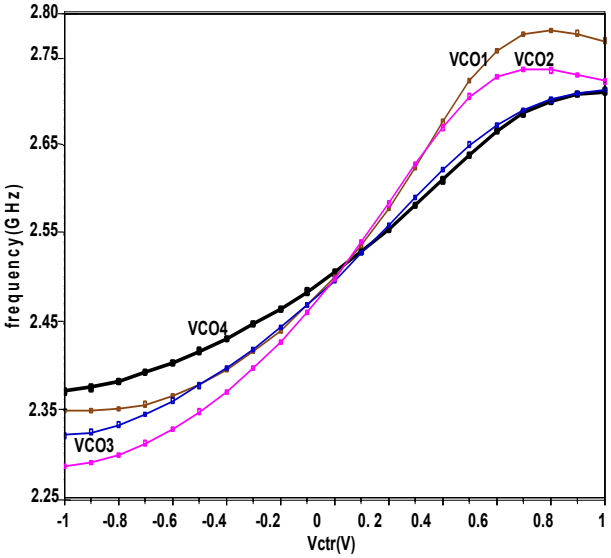

Fig.11. Frequency carrier of –Gm VCO

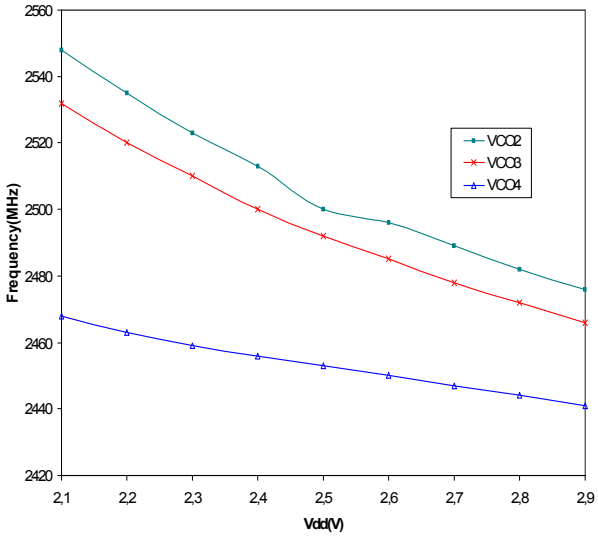

Fig.12. Drift frequency with supply voltage

6. Phase noise

Rael-Abidi identifies the most significant causes of phase noise in oscillators [16] and the expression for evaluating the phase noise of the LC-tank in oscillator at Δf offset frequency. The expression of phase noise in the tank circuit is

$$L(\Delta f) = N_1 N_2 \frac{KTR_p}{V_0^2}\left(\frac{f_0}{2Q\Delta f}\right)^2 \qquad (9)$$

Where T is the ambient temperature, K the Boltzmann constant, f_0 is oscillation frequency, Q the loaded of the resonator, V_0 is output amplitude and R_p is equivalent parasitic resistance.
$N_1 = 2$, $N_2 = 4$ and $V_0 = 2.3$ V
The loaded Q of the resonator will be determined by the loaded Q of the inductor and the loaded Q of the MOS varactor (variable capacitor). Typical Q values for an 'on-chip' spiral inductor at 2.5 GHz is 3 to 5 and the Q values of varactor is superior to 40. Therefore, the loaded Q of the resonator is determined by the Q values of spiral inductor.
The loaded Q of the inductor is determined using this expression

$$Q = \frac{\omega L_s}{R_s} \qquad (10)$$

The inductor used in the design of the VCO has a loaded $Q = 4.34$

The phase noise of the LC-tank in VCO2 is $L(\Delta f) = 1.8610^{-13}$

The active element noise sources are found in the differential pair transistor (switches) and the circuit providing the bias current [17].
The noise of the switches is combination of channel noise and flicker noise in MOSFETs. The expression (19) used to evaluate the noise of differential MOS.

$$L(\Delta f) = \frac{32}{\pi}\frac{\gamma I_0 R_p}{V_0}\frac{KTR_p}{V_0^2}\left(\frac{f_0}{2Q\Delta f}\right)^2 \qquad (11)$$

For the VCO2 the phase noise of switches at 1MHz is $L(1MHz) = 8.9710^{-13}$

The expression (12) is using to evaluate the phase noise of the current source.

$$L(\Delta f) = \frac{32}{9} 2.5 g_m R_p \frac{KTR_p}{V_0^2}\left(\frac{f_0}{2Q\Delta f}\right)^2 \qquad (12)$$

The transconductor of the transistor is given by equation

$$g_m = \frac{2}{R_p} = 5.52 \text{ mS} \qquad (13)$$

For the VCO2 the phase noise of current source at 1MHz is $L(1MHz) = 4.120^{-13}$.

The total phase noise in the VCO2 is the same for the three different sources noise $L_t(1\text{MHz}) = 14.9510^{-13}$
$L_t(\text{dB}) = 10\log(14.9510^{-13}) = -118.25$ dBc/Hz.
Fig.13 shows the output spectrum of VCO4, the frequency centres in 2.5 GHz and presents the 14dBm.

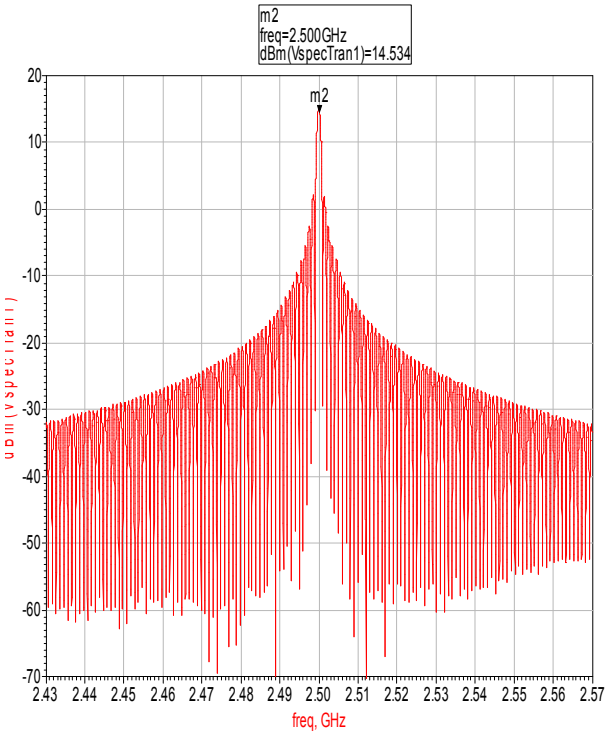

Fig.13. Output spectrum of the VCO4

Fig.14 shows the simulation phase noise in the VCO2, indicate the phase noise of -116.17dBc/Hz at a 1MHz offset, this result is in close proximity to the calculated phase noise.
Resulting plots from ADS simulation of the phase noise of VCO2, VCO3 and VCO4 are shown in fig.14. The phase noise of VCO3 is -122.3dBc/Hz at an offset frequency of 1MHz, this is inferior to the phase noise of VCO2. It is a predicted result because the elimination of the current source minimizes the noise source in the oscillator. It is clear that the VCO4 presents the lowest phase noise. At the offset frequency of 1MHz, The phase noise of the VCO4 is -135.2dBc/Hz.
In order to make a comparison between different VCOs which respect to power, carrier frequency and phase noise, a figure of merit (FOM) expression is used [2, 18, 19, 20].

$$FOM = pnoise(\Delta f) - 20\log\left(\frac{f_{osc}}{\Delta f}\right) + 10\log\left(\frac{P_{loss}}{1mW}\right) \qquad (14)$$

Where f_{osc} is the oscillation frequency, Δf is the offset frequency and P_{loss} is the consumption power (the loss in the tank).

Table 4. Summarized results

	VCO1	VCO2	VCO3	VCO4
f_0 (GHz)	2.5	2.5	2.5	2.5
Bandwidths (MHz)	13.1%	13.3%	10.4%	8.76%
K_{vco} (MHz/V)	327	333	262	219
S_v (%)	3.6	3.6	2.6	1.1
S_T (ppm°C^{-1})	357	-20	-22.9	-5.8
P (mW)	1.1	1.1	1.45	5
Phase noise @1MHz (dBc/Hz)	-119.3	-116.7	-122.3	-135.2
FOM (dBc/Hz)	-186.9	-184.3	-188.6	-196.1

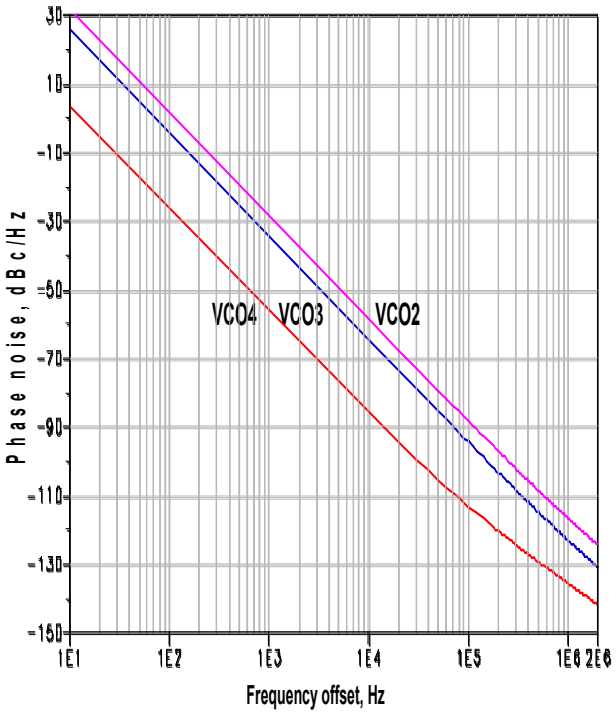

Fig.14. Simulation of the Phase noise of VCO2, VCO3 and VCO4 at 2.5GHz

Table.5 compares the simulated results of this work to some recently reported fully integrated LC VCOs in standard CMOS process.

We note that the VCO3 present a low power consumption comparing to the VCOs presented in these references and the VCO4 presents the lowest phase noise and figure of merite. These results are a compromise between the phase noise and the power dissipation. For the Bluetooth application the VCO4 is the best choice.

Table 5: Compared results with recent VCOs research

References	Frequency (GHz)	Power (mW)	Δf	Phase noise (dBc/Hz)	FOM (dBc/Hz)
[18]	4	7.5	1MHz	-117	-180.3
[19]	4.2	7	1MHz	-122.9	-186.9
This work VCO3	2.5	1.45	1MHz	-122.3	-188.6
This work VCO4	2.5	5	1MHz	-135.2	-196.1
[2]	2.4	1.8	3MHz	-131.4	-187.7
[20]	2.5	2.6	3MHz	-131	-186
This work VCO3	2.5	1.45	3MHz	-133	-189.4
This work VCO4	2.5	5	3MHz	-146	-197.4

7. Conclusion

An efficient and robust method based on two PMOS varactor used to compensate the temperature frequency drift of LC_VCO in this work. We present the simple NMOS VCO compared to the complementary CMOS voltage controlled oscillator. Simulation results show that the performance of NMOS VCO and the CMOS complementary –Gm oscillator without current source. In particular, the NMOS VCO clearly displays the lowest phase noise at large offset frequencies from carrier is about -135.2 dBc/Hz at 1 MHz, and the lowest temperature coefficient is -5ppm/°C in the -20 to 120°C range and the lowest sensitivity with the variation of the supply voltage and the largest tuning frequency 9%. CMOS complementary –Gm oscillator without current source presents the lowest power consumption 1.45 with phase noise -122dBc/Hz at 1MHz.

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