

A Development of Disk Drive with Flash Memory for ATA-6

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Summary

In this paper, we have designed and constructed a flash memory drive using the ATA-6 bus method for flash memories, which is an element of semiconductors, in order to improve the problems with existing general hard disks. General hard disks are sensitive to impact or shock and because of these, errors in the data or disks occur. Also, due to its internal structure, it requires much electricity and is not suitable to make it light-weight. However, by using flash memory, which is an element of semiconductors, to produce hard disks, low electricity start up becomes possible, not to mention light-weight. It is also strong against external impact and is expected to be utilized for embedded systems, black boxes, vehicles, ships, as well as for other industrial and military use.

Key words:

SSD, Disk Drive, Flash Memory, ATA-6

1. Introduction

Currently, the most generally used additional memory devices for PCs and servers are hard disks which use a disk revolution method. With the recent sales of S-ATA hard disks, high-capacity hard disks have now become available at a reasonable price. However, a disadvantage with this, these hard disks are that in order to access data, a spindle motor rotates rapidly, thus costing high electric power. Also, the physical structure of this is that the semiconductor head rises about 0.1 μm above the disk surface in order to read and write data. This structure makes it prone to colliding with the disk surface when impacted or power is suddenly turned off, making it possible for the inability to read or store data. Therefore this treatise deals with the design, production and evaluation of a hard disk using flash memory in order to solve the problems with general hard disks.

2. Hardware Design for ATA-6

In order to design and produce the additional memory device through flash memory for personal computers, we have used the enhanced structure of the ATA-6 interface to design the hard disk.

Since most general PCs use ATA-6 hard disks to boot

their OS, we have placed our objective in realizing an ATA-6 flash disk. Most ATA-6 interfaces support both 8 bit and 16 bit. However, for the sake of simplicity of the system in this paper, we have designed the ATA-6 interface. [1]

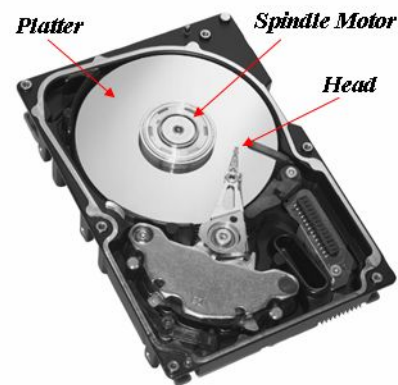


Figure 1. Structure of general hard disk

Finally, in order to embody the most suitable control and high-speed data processing for each part, we have used a Digital Signal Processor, the TMS320F2812 as the main control unit.

Also, in order to solve the problem with the bottleneck effect of the data while the data is being handled between the PC and hard disk, we have added two double type SDRAM buffers. And in order for the efficient address management of the attached flash memory, we have embodied a DMA.

Also, in order to produce flash memory disks of various capacities, we have used single layer flash ROMs K9F1G08 and K9F4G08 and dual layer flash ROM K9W1G08, K9W2G08 and K9W8G08 from Samsung semiconductors.



Figure 2. Hardware of Proposed ATA-6 Drive

3. Firmware Design for ATA-6

For the disk drive using flash memory as proposed in this paper, the internal interface is linked to the FPGA and its structure is made up of a flash memory that uses the existing ATA-6 physical disk and head. In order to process the ATA-6 commands, there is an interface processor which is including the ATA-6 Special Function Registers to communicate with the FPGA.

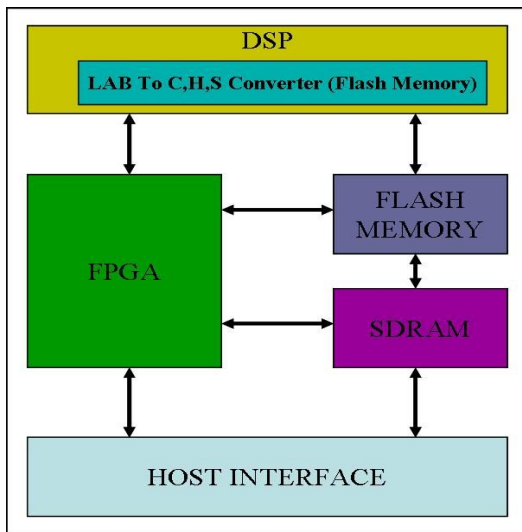


Figure 3. Block diagram of ATA-6 read/write using Flash Memory

In order to analyze these command, it is composed of a microprocessor interface and DMA interface, buffer memory, decoder that can choose each flash memory, boot memory, flash memory banks, and a part which can select the host adopter interface and mode.

4. FPGA Design for ATA-6

The FPGA has two kinds of constructions. The lower structure is made with three kinds of structures to proceed of the command which was generated by host, and the upper structure is made with two kinds of structures those one is to proceed of the command which was generated by DSP and data flow control, and the other is to control of the lower structure.

There are three kinds of the lower structures. First, it is in conjunction with inner register, second is related with data I/O of the PIO mode and the third is that of data I/O of Ultra DMA mode.

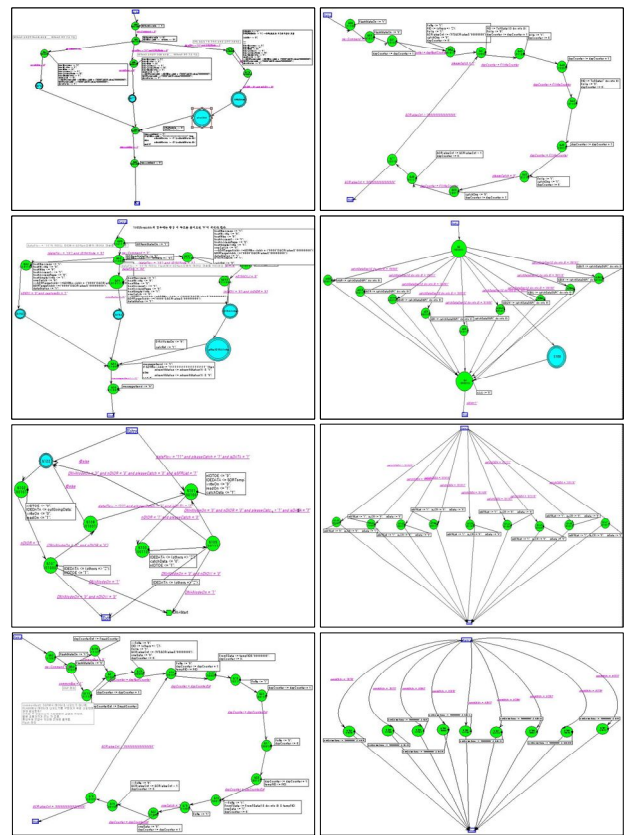


Figure 4. Status of the lower structure

It is controlled of upper structure that of data flow with SDRAM and ATA host, and SDRAM and Flash Memory. It is controlled of lower structure to decode and process of the command which was generated by the DSP.

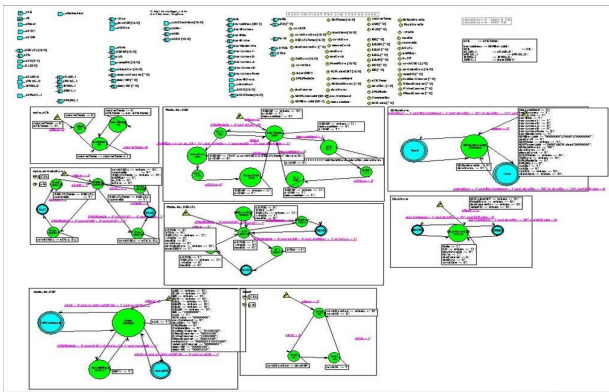


Figure 5. Status of higher structure

There are three sequences to process the command that was generated by ATA host.

1. Transfer the command from the ATA host to the DSP.
2. Transfer the inner command from ATA host to FPGA.
3. Process and report of the DSP command.

5. Results

From the proposed ATA-6 flash drive, we have analyzed of ATA signals which were generated from a host PC to target drive. We can show you the results from figure 6 to figure 13.

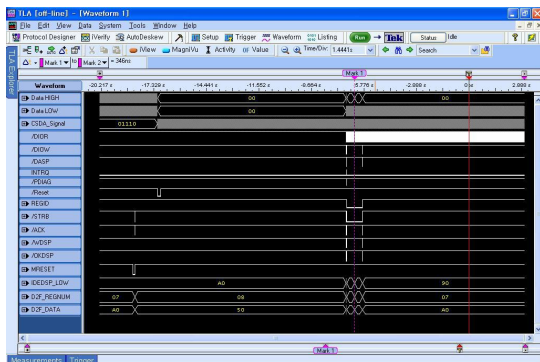


Figure 6. Full signal flows of ID sequence

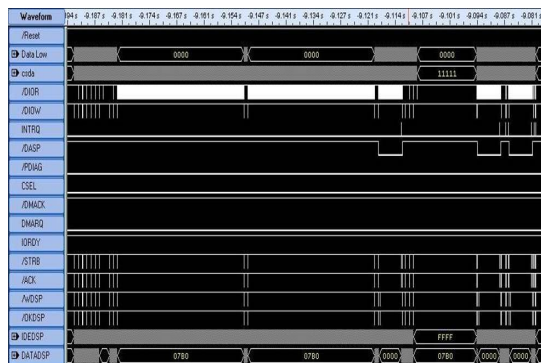


Figure 7. Register Transfer to/from Device

Figure 6 is showed that the host PC would find the proposed ATA-6 drive as a general HDD. If there is any errors on this sequence, the host PC will stop the finding sequence of any device and pass the next sequence.

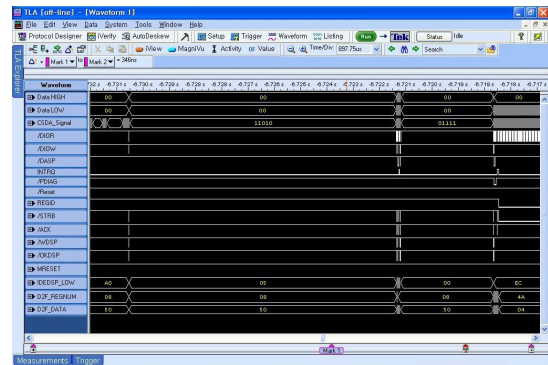


Figure 8. Sequence of finding the master HDD

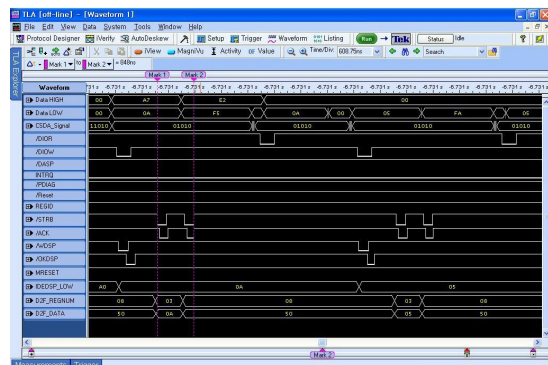


Figure 9. SFR set sequence

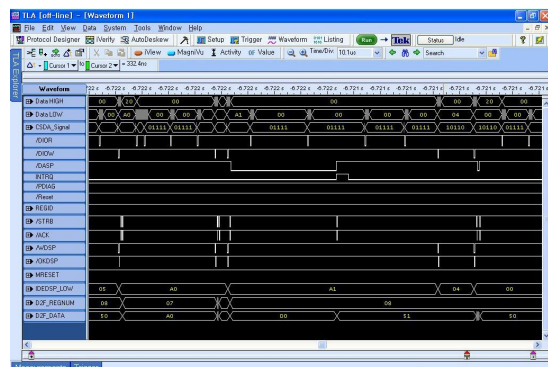


Figure 10. Soft-Reset sequence

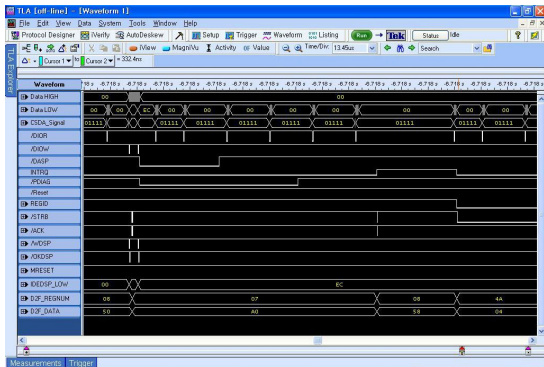


Figure 11. Set sequence for ID information

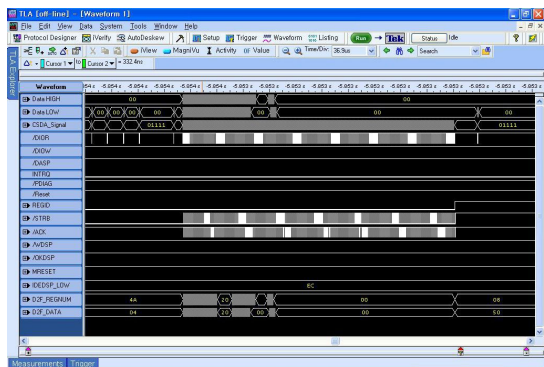


Figure 12. ATA-6 HDD ID sending sequence



Figure 13. HDD ID information on host PC

Figure 13 is showed that the proposed ATA-6 flash drive is working good as general HDD on the personal computer.

6. Conclusion

From this research, we can expect acquirement of key technology of the ATA-6 Flash Memory Drive, and through intellectual rights gained from the design of the ATA-6 Flash Memory Drive, we have secured company competitiveness. Also, the ATA-6 Flash Memory Drive developed in this research is expected to be utilized in

various embedded systems and especially from 2007, when cars will be required to attach it as a recording device, the demand for it is expected to rise. In the future, we are planning to develop it for 1.8 inch laptops and slim-types.

References

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