PSPICE simulation and implementation of closed loop controlled ZVS LCL push-pull DC-DC converter

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Summary

A high performance ZVS LCL push-pull DC-DC converter under closed loop control is analyzed with PI controller. Soft switching acquired by the primary MOSFET switches under LCL combination reduces the switching stress. Single device voltage drop on the primary side and resonating capacitor acting as tuned filter in the load side justifies an efficient converter. Quick settling time of error in the output for PI controller justifies its superior performance over other controllers. Circuit model developed in PSPICE for open and closed loop systems are analyzed and simulated. Various resonant topologies like LCL, LLC are compared and analyzed. Simulation results help in verifying the validity of PI controller for the closed loop controlled system. Experimental results on DC-DC converter match with the simulated results. Microcontroller is used to drive the MOSFET switches of the push pull converter.

Key words:
DC-DC ZVS converter, P and PI controller and push pull technique, Microcontroller.

1. Introduction

DC-DC converter working with limited energy storage battery cells, need to work on conditions like low voltage to high voltage conversions, input current exceeding the voltage of some order, input voltage side disturbances. A closed loop push pull converter is designed aiming the above working conditions. Incorporating some features like single device voltage drop on the input side, maintaining continuous power flow, keeping peak currents down to reasonable value and zero voltage turn on of switches by commutation of transformer magnetizing current [1], the new push pull controller is enhanced with a closed loop PWM controller. The output is maintained at a reference value for any input voltage disturbances by controlling the gate pulses of the MOSFET.A coaxial transformer having two-turn center tapped primary winding with low inter primary leakage inductance results in leakage inductance confined to the secondary side only [2]. Unlike other LCL topologies presented in literature [4]-[6], the topology presented here has the resonant components located after rectifier side which provides for a reduced current turn-off of the primary switches, thus keeping the trapped primary leakage energy to a minimum. Also the capacitor on the load side acts as tuned filter.Figure1 depicts a closed loop system for discussion.

In the literature [1]-[12], the circuit model for closed loop control of ZVS LCL push pull resonant converter is not presented. In the present work, a circuit model for closed loop system is developed. Performance with PI controller is presented. Simulation results justify the performance of the closed loop PI controlled system. The simulated results are experimentally verified by constructing a hardware model of DC-DC converter controlled by a microcontroller.

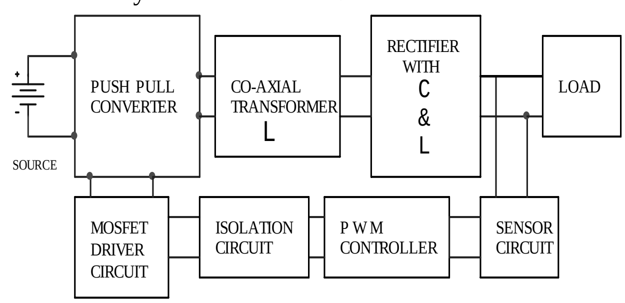

Fig. 1 Block diagram of closed loop system

2. ZVS LCL push pull topology

MOSFET switches S1 and S2 in the primary side of the circuit experience the push pull concept, where at a time one of the switch conducts and the other is off. This readily minimizes voltage drop on low voltage input side. The switches share the current equally providing excellent surge capability each running at 50% duty cycle, 180º out of phase. The square wave from the switches is applied to the transformer. The magnetizing current of the transformer will flow through the body diodes of MOSFET leading to zero voltage turn on.

The coaxially wound transformer with two turn center tapped primary winding is uniquely designed such that all the leakage inductance is confined to secondary side. Leakage flux doesn't pass through the transformer core thereby saturation of leakage inductance is avoided.

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The body diodes of the MOSFET should be avalanched for dissipating some of the trapped energy in the primary side leakage inductance. The transformer inductance along with the capacitor and inductor in the load side from a parallel loaded LCL resonant converter. The capacitor is in parallel with the load. Compared to series loaded resonant converter parallel loaded resonant converter has advantages like it can step up and also step down, better suited for multiple outlets and can operate in a large number of combinations consisting of states of inductor current and capacitor voltage. The final C-L components resonate with the leakage of the transformer twice the switching frequency of S_1 and S_2. By using good quality capacitor and air core inductor the LCL resonant frequency will remain constant over the entire range of converter loading. With less stress on the MOSFET switches the size of the transformer and the resonating elements become small at high frequency switching. The output of the converter is to be maintained to a desired level. A feedback circuit with a PWM controller is modeled in order to achieve the above said criteria.

3. Fundamental modes of operation

The converter has four fundamental modes of operation, wherein in each mode only one switch conducts. In normal operation, modes 1 and 3 represent brief switching transients where the transformer magnetizing current is commutated. The majority of power flows across modes 2 and 4.Both positive and negative values of the inductor currents have their paths through MOSFET or the diodes across the switches. For a given transformer and its leakage inductance, the resonant frequency of LCL tank circuit can be calculated for a range of C and L components.

4. Design consideration

Transformer is selected according to the input and output design values. Cut toroidal ferrite core features exact air gap avoiding saturation. The leakage inductance of the transformer is calculated and for a desired switching frequency a range of L and C components are found. Larger the value of C will reduce the voltage stress upon the rectifier side diode but induces high ripple current. But large value of L will reduce the ripples. Tuning of the capacitor and resistor in the PI controller to optimum value results in better performance.

5. Comparison

Earlier resonant topologies like series resonant converter has its own limitation. Figure 2 depicts the series resonant converter, where the resonant capacitor is in series with the rectifier circuit. The rectifier input will be of current fed and hence the output on the rectifier is a stiff voltage source.

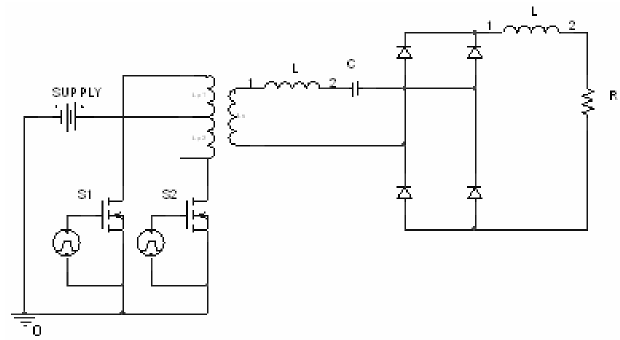

Fig. 2 Series resonant converter

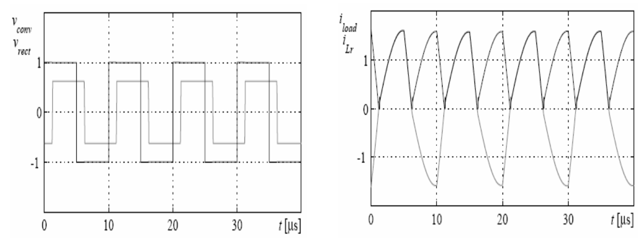

Fig. 3 Voltage and current waveform of series resonant converter

In series resonant converter, if switching frequency is less than resonant frequency, then resonant circuit behaves like a capacitive load else inductive in nature. Also load current if continuous would lead to turn on in hard switching mode and turn off either as ZVS or ZCS mode. Figure 3 reflects the voltage and current waveform for series resonant converter.

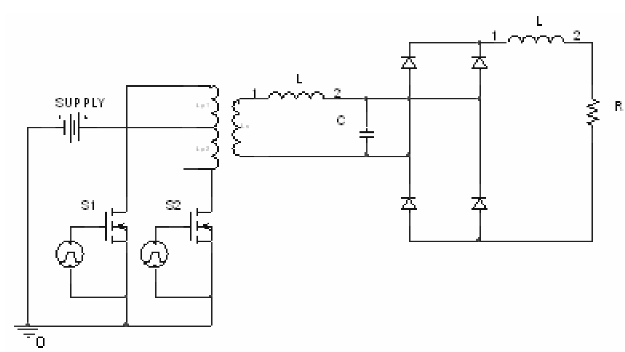

Fig. 4 Parallel resonant converter

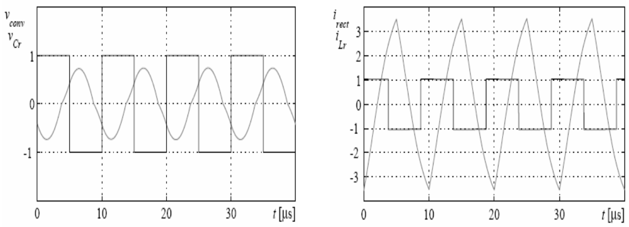

Fig. 5 Voltage and current waveform of parallel resonant converter

Figure 4 depicts parallel resonant converter where the capacitor is placed parallel to the rectifier circuit. Resonant capacitor acts like a voltage source and thus the rectifier output with be a current source. Here continuous load current would have turn on in ZVS mode. In the above topology separate filter capacitor has to be placed after the rectifier output. To avoid the above problem, a new topology where the resonant capacitor is placed to the output of the rectifier, which will act as dual purpose for both resonance and as filter. Figure 5 reflects the voltage and current waveform for series resonant converter.

6. Simulation results

Figure 6 depicts open loop circuit model with a disturbance. This disturbance can be related to unregulated input supply or supply imbalance. The disturbance is initiated after 10 ms delay. The output voltage, which is increased with increase in input voltage, is shown in Figure 7. The simulated resonant inductor current and capacitor voltage, which are disturbed at 10ms, are shown in Figure 8and 9 respectively. We can see that in Figure 10 the input power waveform is discontinuous. This can be avoided by introducing a capacitor in series with the input supply Also the reverse current spike produced during the switching transition in modes 1 and 3 is absorbed by these decoupling capacitances Thus disturbance in the input side affects the entire system, which has to be reduced.

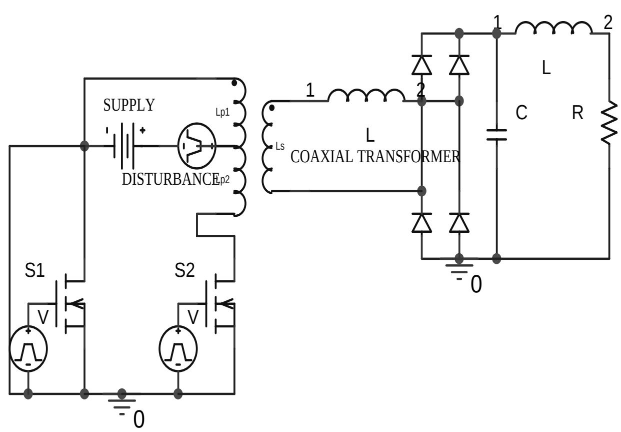

Fig. 6 Open loop system with input disturbance

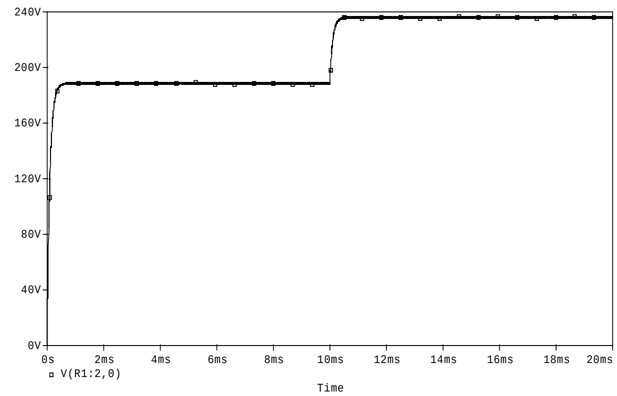

Fig. 7 Open loop output voltage with disturbance

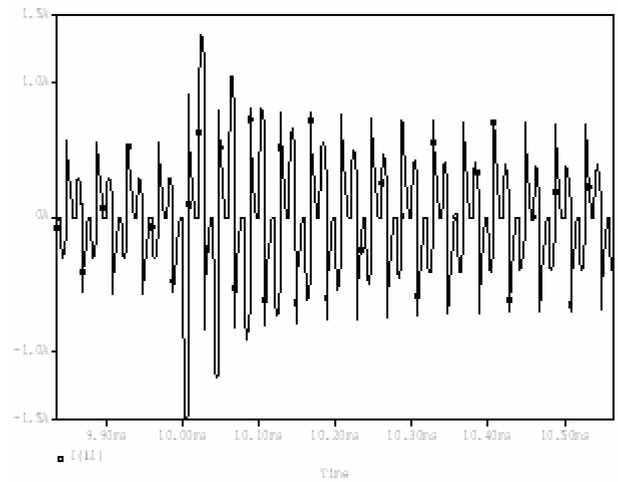

Fig. 8 Open loop inductor current with disturbance

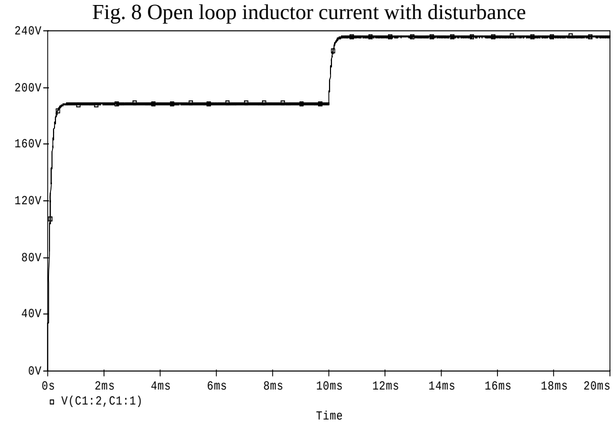

Fig. 9 Open loop capacitance voltage with disturbance

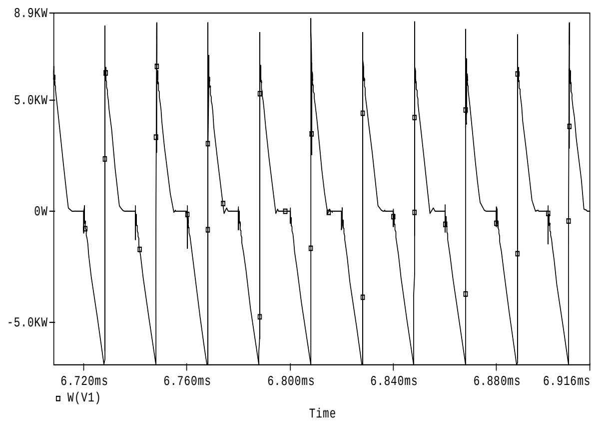

Fig. 10 Open loop input power with disturbance & without decoupling capacitance

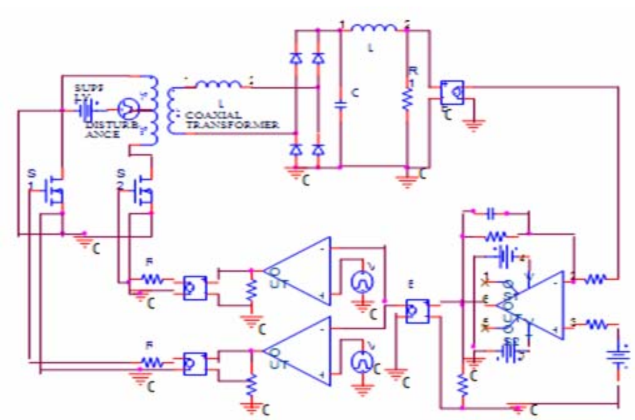

Fig. 11 Closed loop circuit model with PI controller

Figure 11 depicts the closed loop simulation circuit using PI controller where input side voltage disturbances are created at a specified time. The output voltage remains constant till the time of disturbance. The input voltage disturbance gets reflected in the output side, leading to overshoot in the output voltage. The closed loop PI circuit with PWM controller helps in reducing the overshoot. The output voltage is continuously compared with a reference voltage using a differential amplifier. The differential signal is amplified and fed to a comparator circuit, which compares it with a triangular wave. The comparator output is fed to one of the MOSFET switches. Another triangular wave which is phase shifted by 180º is compared with the same differential amplifier output and the output of the second comparator is fed to the other MOSFET. Thus changes in the output voltage are reflected in the differential amplifier output and in turn in the comparator output. Figure.12 shows how the width of the gate pulse is reduced from the instant of disturbance. At exactly 10ms the output voltage shoots up to a higher value. The on time of MOSFET pulses are reduced and the output voltage is brought down to nominal value.

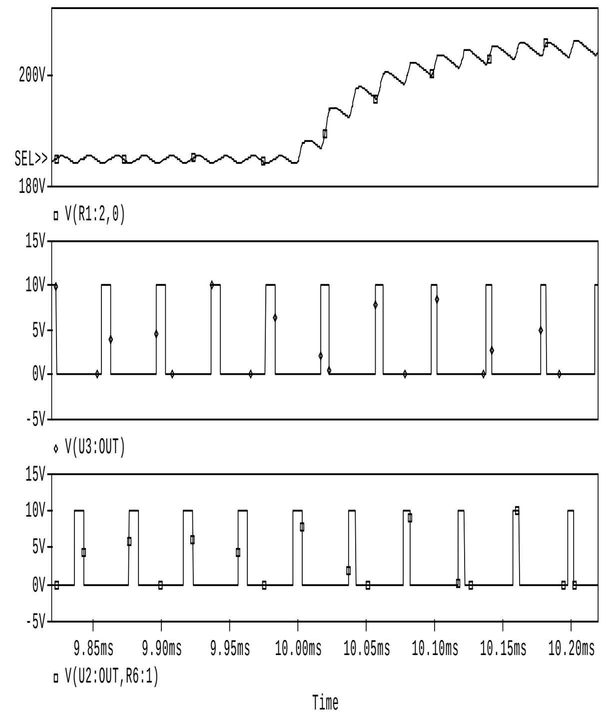

Fig. 12 Output voltage, Pulses of MOSFET 1, 2 before & after disturbance

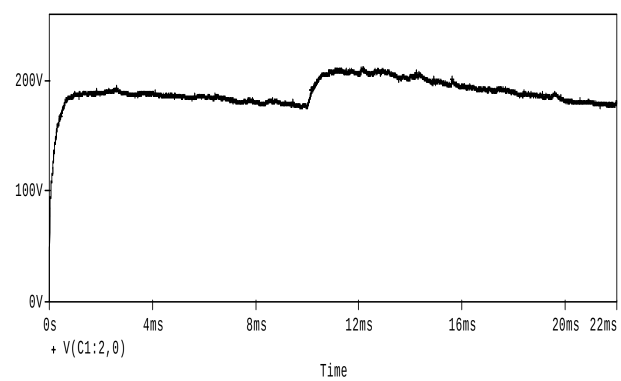

Fig. 13 Closed loop output voltage

Figure.13 shows the voltage response curve for closed loop system with PI controller when a disturbance is applied at 10ms.The settling time of error signal is 10ms.After 20ms seconds it reaches a constant value which is same as the original output voltage. The tuning of resistance and capacitance in the PI controller results in better output voltage. The R and C are responsible for reducing the settling time in the output voltage. Table1. shows the error voltage for P and PI controllers. The error voltage for P controller is nearly 18V.But for PI controller the error voltage goes to zero at 20ms.

Table.1.Output voltage values at different instances

	Before disturbance	After disturbance		
Time (msec)	8	12	18	20
P controller Output voltage	190	208	208	208
PI controller Output voltage	190	208	200	190

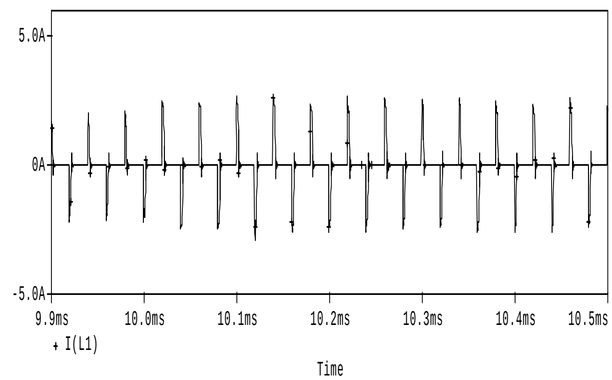

Fig. 14 Closed loop Inductor current

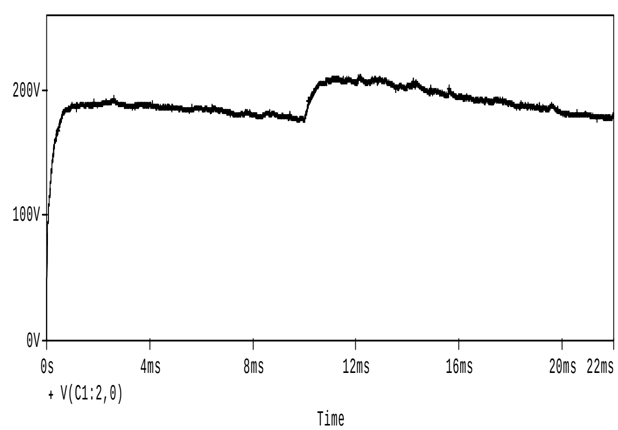

Fig. 15 Closed loop capacitor voltage

Figure.14 and Figure.15 indicate the inductor current and capacitor voltage for PI controller system. Peak value of inductor current was reduced with PI controller system. Thus the PI controller shows better performance than P controller.

7. Experimental Results

DC-DC converter is fabricated and tested. Atmel microcontroller 89C2051 is used to generate driving pulses for the MOSFETs. The control circuit is shown in Figure.16.

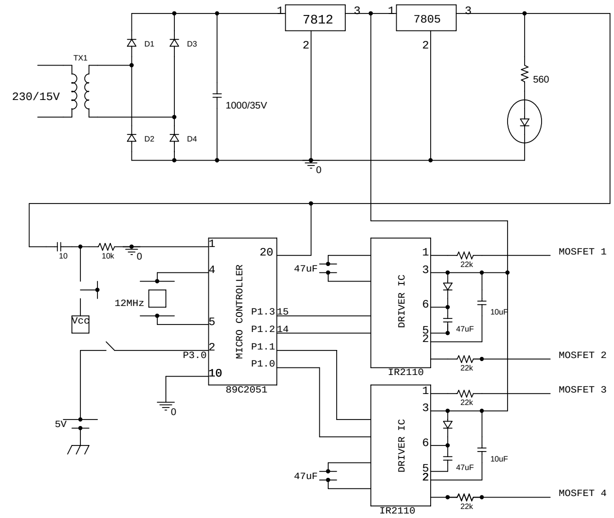

Fig. 16 Control circuit

The hardware module is shown in Figure.17.The oscillogram of output of push pull converter is shown in Figure.18. The oscillogram of output of the driving pulse generated by the microcontroller for both the MOSFET switches is shown in Figure.19.The AC output of the transformer secondary is shown in Figure.20. The oscillogram of output of the DC-DC converter is shown in Figure.21.

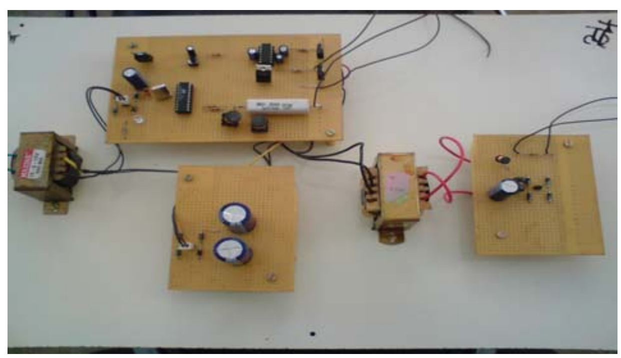

Fig. 17 Hardware module

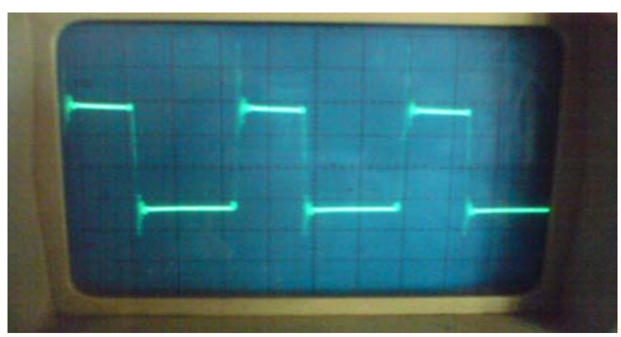

Fig. 18 Oscillogram of output of push pull converter output voltage

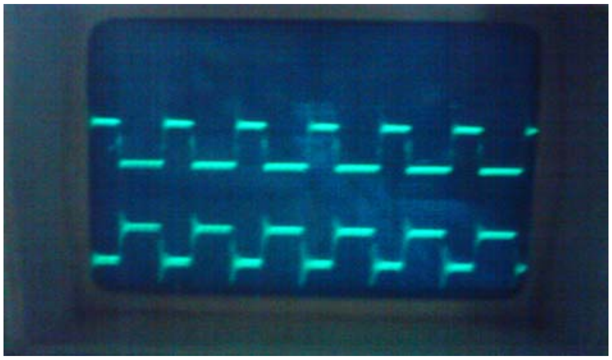

Fig. 19 Oscillogram of driving pulses.

Fig. 20 Oscillogram of transformer secondary voltage

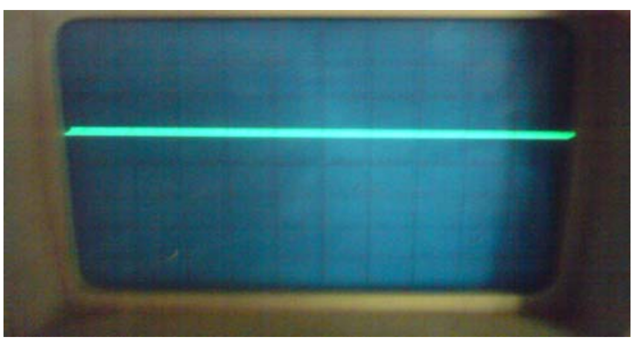

Fig. 21 Oscillogram of output of DC-DC converter

8. Conclusion

The PSPICE circuit model for closed loop system with PI controllers was developed and the DC to DC converter system was successfully simulated using this model. The LCL resonant topology is suited for unregulated DC-DC conversion from a low voltage to a high voltage source. The circuit exhibits ZVS for the MOSFET switches and capacitively snubbed operation for the output rectifier. The LCL resonance reduces the energy trapped in the primary leakage inductance at turn off. Compared to other topologies LCL topology gives better result.The open loop and closed loop ZVS LCL resonant push pull DC-DC converter results are presented. The PI controller exhibits better performance when compared to P controller. The settling time with PI controller is 10ms. The steady state error was reduced by tuning the PI controller. The simulation results agree with the experimental results.

9. References

[1] M.Shoyama and K.Harada, "Zero-voltage-switching realized by magnetizing current of transformer in push-pull DC-DC converter", in Proc. IEEE, IETELEC'91, 1991, PP.640-647.

[2] M.S.Rauls, D.W.Novotny and D.M.Divan," Design considerations for high frequency co-axial winding power transformer", in conf.Rec.IEEE-IAS- Annu.meeting, 1991, pp.946-952.

[3] M.S.Rauls, D.W.Novotny, D.M.Divan, R.R Bacon and R.W.Gascoigne," Multiturn high frequency co-axial winding power transformer", in conf.Rec.IEEE-IAS Annu Meeting, 1992, pp. 956-963.

[4] R.P.Severns," Topologies for three element resonant converter", IEEE Trans. Power Electron. Vol.7, pp.89- 98, Jan.1992.

[5] "Generalized topologies for converters with reactive energy storage", in conf. Rec. IEEE-IAS Annu. Meeting, 1989, pp.1147-1151.

[6] I.Batarseh," Resonant converter topologies with three and four energy storage elements", IEEE Trans.Power Electron, vol.9, pp.64-73, Jan.1994.

[7] K.H.Liu and F.C.Lee," Zero voltage switching technique in DC-DC converter", in conf.Rec.IEEE PESC'86, 1986, .58-70

[8] Michael J. Ryan, William E. Brumsickle, Deepak M. Divan and Robert D. Lorenz, "A new ZVS LCL Resonant push-pull DC-DC converter topology", IEEE Trans Industrial applications, vol 34.No 5 oct 1998

[9] H.Pinheiro and P.Jain, "Comparison of UPS topologies based on high frequency transformers for powering the emerging hybrid fiber coaxial networks." In Proc. IEEE Int. Telecommunications Energy Conf. Copenhagen Denmark 1999, Paper 11-2.

[10] P.Alou. O. Gareia.J.A.Cobos.J.Ueeda and M.Raseon, "Fly back with active Clamp: A suitable topology for low power and very wide input voltage range applications." Proc.IEEE Applied power electronics Conf APEC.Anaheim.CA.2002.PP.242-248.

[11] J.de.la Pena.M.Rivas.A. Huertas.M.Perez and M. Raseon, "Wide input range module for rectified AC power distribution demonstrator for telecommunication system." Proc.IEEE Applied power electronics Conf APEC.Anaheim.CA.2002.PP.1202-1207.

[12] Arturo Fernandez, Member, IEEE,Javier Sebastian, Member IEEE, Maria Hernando Member IEEE, "Multiple output AC/DC Converter with an Internal DC UPS." IEEE Trans on Industrial Electronics.vol.53.no.1.Feb 2006.

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