Sequential Circuits In The Framework Of (2n+1)-ary Discrete Logic

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Abstract
This paper is concerned with the formulation of a novel paradigm called (2n+1)-ary logics and their ultimate use in the development of multiple valued logic based processor. Apart from a preliminary introduction to the binary valued logic systems, this paper introduces the notion of *Truth values Reliability-Unreliability model* and a brief exposition of multiple valued logic in the framework of switching algebra. Finally the paper discusses the simulation results of implementing primarily ternary and penta logic switching functions using traditional binary logic circuits.

Keywords:
Multiple Valued Logic, Switching functions

1. Introduction

Until late 1960's, theoretical nature of computing techniques has been established using binary valued digital systems. Even today, the latest computing systems are designed and developed using binary logic only. Alternatively, people have also been working on the possibilities of using multi-valued logic for developing faster computing techniques. It is but natural to assume the 10-valued logic (decimal) systems as an alternative to binary systems, since decimal machines would gain rapid acceptance if they could be produced reliably and inexpensively. Unfortunately, the present state of technology is more amenable to implementing lower radix systems. In real life situations, there is no clear cut binary yes/no requirement; situations such as yes/no/not defined, or up/down/stop, or left/right/straight ahead abound in the real world scenario. This amounts to saying that multi valued logical systems, for instance, a three-valued (radix 3) digital realization would be more appropriate than binary [2]. The significance of using higher radix is the possibility to reduce the number of interconnections per system or subsystem. As the value of radix increases, the information carrying capacity of each connection also increases [5].

In this paper, we explore the possibilities of realizing sequential switching circuits using multi valued logic or more precisely using what we call as (2n+1)-ary discrete logic.

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2. Binary Logic

In view of describing the notion of multivalued logic (MVL), we first consider the primary logic levels 0 and 1 and the associated Boolean logic in our discussion [3]. In 1938, Shannon proved that a two-valued Boolean algebra (whose members are most commonly denoted 0 and 1, or false and true) can describe the operation of two-valued electrical switching circuits. In modern times, Boolean algebra and Boolean functions are indispensable in the design of computer chips and integrated circuits [6]. Boolean algebras have recursive structures apparent in the Hasse diagrams shown in figure 1, which illustrates Boolean algebras of orders n = 2, 3, 4 and 5. These figures illustrate the partition between left and right halves of the lattice, each of which is the Boolean algebra on (n-1) elements. The complexity of Hasse diagrams increases as the order increases, which, of course, could be easily solved out by implementing these logics into a semiconductor chip.

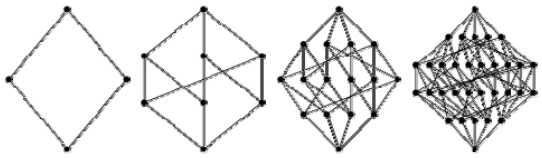


Figure 1: Hasse diagrams illustrating Boolean algebra

The binary logic levels can also be represented using Venn diagrams which originated in Venn (1894). Figure 2(a) represents a two variable example and 2(b) represents a three variable example which are self explanatory [4].

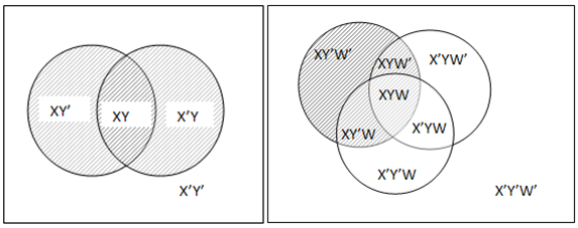


Figure 2
(a) Venn diagrams representing for a two variable map, $n = 2$.
(b) Venn diagrams representing for a two variable map, $n=3$.

A three variable Boolean algebra yields 256 Linear Boolean Functions (LBF). In general, an n-variable Boolean algebra deals with 2^{2^n} Linear Boolean Functions. Similarly, a k-variable (2n+1)-ary discrete algebra deals with $[2(n+1)]^{[2(n+1)]^k}$ Linear Algebraic Functions. Model theory is basically understood as a union of algebra and logic. Boolean algebra is a model of Boolean logic. Any algebraic system, for that matter, is a model of classical logic that works on truth values T and F. However, in a real life situation, one would admit to the fact that decision made on observations do not precisely comply with 'True', 'False' values. On the other hand, there is always an uncertainty in deciding these values, rather, one would come across situations wherein one has to accept multiple decision values like to what extent the decision may be true and to what extent the decision may be false [6]. This argument is sufficient enough to support for the truth value model shown in figure 3.

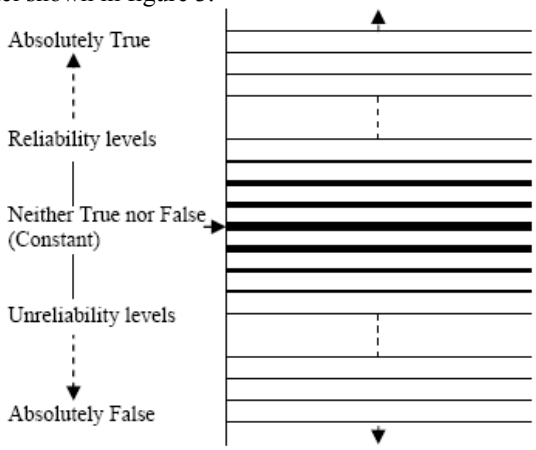


Figure 3: Truth values Reliability-Unreliability model

3. Multivalued Logic

Traditional calculi are only two valued for any proposition. **Multi-valued logics** are logical calculi in which there are more than two truth values. Multivalued system has several important advantages over existing binary system. Expanding the existing logic levels to ternary and penta levels, higher processing rates could be achieved in various applications like memory management, communication throughput and domain specific computation. An evident advantage of a ternary representation over binary is economy of digits. To represent a number in binary system, one needs 58% more digits than that of ternary [5]. For example, to represent a 15-digit decimal number, one requires 34 ternary digits instead of 54 binary digits. Ternary representation admits sign convention also. The most significant advantage is that there is reduction in the interconnection required to implement a logic function. This in turn causes reduction in the chip area while designing devices [6].

In contrast to the design it is also necessary to assess the cost of manufacturing of these types of multiple valued logic circuits. Let R be the radix, d be the number of digits to express a range of N numbers is given by $N = R^d$. Assume that the number and/or cost of the basic hardware components C is proportional to the "digit capacity" R X d, then we have

$$C=k(Rd) = k(R \frac{\log_e N}{\log_e R})$$

where k is some constant. Differentiating this cost equation with respect to the radix R and equating to zero gives that R should equal e(=2.718) for minimum cost. From this analysis R=3 should be more economical than the binary radix R=2. If we consider that devices or circuits are available which provide two, three four or more stable digital signals without any increase in individual costs for the higher-valued radices, then in such ideal circumstances total cost C would be proportional to d. Hence,

$$C=kd = k \frac{\log_e N}{\log_e R}$$

which is a gradually decreasing total cost C with increasing R [12].

Table 1 shows representation of decimal numbers using ternary symbols. The decimal number D in terms of ternary symbol is given by

$$D = \{T_n 3^n + T_{n-1} 3^{n-1} + \ldots + T_1 3^1 + T_0 3^0\}$$

where T = ternary digit -1, 0, +1

n= significance of the ternary digit,

T_0=least significant

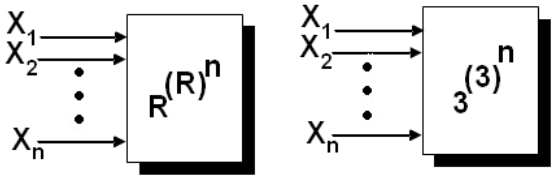
T_n = most significant.

However, the -1, 0, +1 numbering system has a unique advantage that any number can be changed from a positive value to the corresponding negative value by merely changing all -1's to +1's and vice versa, leaving all zeros unchanged [12].

Table 1: showing representation of decimal numbers using ternary symbols

Decimal Number D	Ternary notation using the number -1, 0, +1	Decimal Number D	Ternary notation using the numbers -1, 0, +1
0	0 0 0 0	4	0 0 1 1
1	0 0 0 1	5	0 1 -1 -1
2	0 0 1 -1	6	0 1 -1 0
3	0 0 1 0		

For a system with n multi-valued inputs X_1 to X_n and one multi-valued output f(x), (Refer to figure 4(a)), the different number of signal input combinations is R^n and the number of different functions f(x) of the n inputs is R^{R^n}. For example, a ternary system of three variables (Refer to figure 4(b)) has 3^n input combinations and 3^{3^n} possible ternary valued functions.



a) R-Valued b) three-valued (ternary)

Figure 4: Multivalued system

4. Algebraic Contemplation Of Multivalued Logic

A ternary operation on {0, 1, u} is said to be regular if its truth table satisfies the following condition: *A given column (row) contains 1 in the u row (column) only if the column (row) consists entirely of 1s; and likewise for 0* [2]. Any subset of a set of r truth value E(*r*) ≡{0,1,….,*r*-1}is called a set-value and a logic whose truth values are set values on E(*r*) is called an *r*-valued set logic [1]. In this paper we concentrate on discrete interval truth values. Let E(s,r) be a set of truth values {*s-1,s-2,……,0,1,…..r-2,r-1*}. Then we will define a set I_r as a collection of intervals {*k, k+1,…..l-1,l,0,i,i+1,….j-1,j}* of E(s,r), where *s,r,i,j* ⊆ E(r) and i ≤ j, s ≤ r respectively, i.e., I_r {{*k, k+1,…..l-1,l,0,i,i+1,….j-1,j*}} ⊆ E(s,r) | s-1 ≤ k ≤ l ≤ 0 ≤ i ≤ j ≤ r-1}. It is evident that the set I_r forms a partial ordered set with regard to the set-theoretic inclusion ⊆ . This is why the set-theoretic inclusion ⊆ is one of the most important partial ordered relations on the set I_r which is a non-monotonic function in our case. Every element in I_r is usually determined by its minimum and maximum elements respectively.

The values of the signals used in a multiple-valued system of radix R are most commonly the extension of the positive integer binary notation, giving the set{0, 1, …, R-1} for any R-valued system. An exception to this where the radix is odd, in which case we may find the balanced system

$$\left\{-\left[\frac{R-1}{2}\right], \quad -\left[\frac{R-3}{2}\right], \ldots, 0, \ldots, \left[\frac{R-3}{2}\right], \left[\frac{R-1}{2}\right]\right\}$$

This is particularly relevant for ternary arithmetic giving values {-1, 0, +1} [12].

5. Sequential Logic Circuits Using (2n+1)-ary Discrete Logic

One can design (2n+1)-ary logic based sequential electronic circuits making use of the concepts discussed so far in the previous sections, however, the discussion on such design principles is beyond the scope of this paper. The hardware associated with multiple level logic is quite different from that associated with binary level logic, yet one can examine the possibility of simulating (2n+1)-ary logic swiching functions using traditional binary level logic circuits. To exemplify such a possiblity, SR, JK and D switches are simulated using binary flip flops [13]. The truth tables and circuit diagrams are shown.

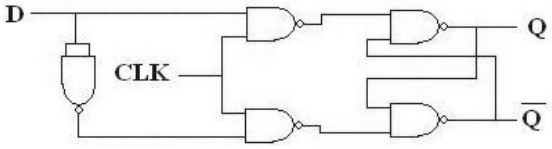


Figure 5: Logic diagram of a D type switch

D	CLK	Q	$\bar{Q}$
-1	-1	-1	1
-1	0	-1	1
-1	1	-1	1
0	0	0	0
0	-1	0	0
0	0	0	0
1	1	1	-1

Figure 6 (a)

D	CLK	Q	$\bar{Q}$
-2	-2	-2	2
-2	-1	-2	2
-2	0	-2	2
-1	1	-1	1
-1	2	-1	1
-1	1	-1	1
0	0	0	0
0	-1	0	0

D	CLK	Q	$\bar{Q}$
0	-2	0	0
1	-1	1	-1
1	0	1	-1
1	1	1	-1
2	2	2	-2
2	1	2	-2
2	0	2	-2

6 (b)

Figure 6: Truth table for D type switch with (a) ternary (b) penta logic

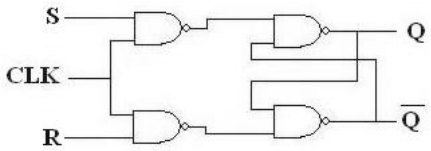


Figure 7: Logic diagram of clocked SR type switch

CIK	S	R	Q	$\overline{Q}$
-1	-1	1	-1	1
0	-1	0	-1	1
1	-1	0	-1	1
0	0	1	0	0
-1	0	-1	0	0
0	0	1	0	0
1	1	-1	1	-1
0	1	-1	1	-1
-1	1	0	0	0

Figure 8(a)

S	R	CLK	Q	$\overline{Q}$
-2	2	-2	-2	2
-2	-1	-1	-2	2
-2	0	0	-2	2
-1	1	1	-1	1
-1	-2	2	-1	1
-1	0	1	-1	1
0	1	0	0	1
0	2	-1	0	1

S	R	CLK	Q	$\overline{Q}$
0	-1	-2	0	0
1	-2	-1	1	-1
1	-1	0	1	-1
1	2	1	1	1
2	0	2	1	0
2	1	1	1	1
2	-2	0	2	-2

8 (b)

Figure 8: Truth table for clocked SR type switch with (a) ternary logic (b) penta logic

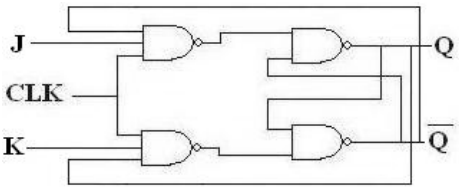


Figure 9: Logic diagram for JK type switch

J	K	CLK	Q	$\overline{Q}$
-1	0	-1	-1	1
-1	1	0	-1	1
-1	-1	1	-1	1
0	0	0	0	0
0	1	-1	0	0
0	-1	0	0	0
1	0	1	0	0
1	1	0	0	0
1	-1	-1	0	0

Figure 10 (a)

J	K	CLK	Q	$\overline{Q}$
-2	2	-2	-1	1
-2	-1	-1	-1	1
-2	0	0	-1	1
-1	1	1	-1	1
-1	-2	2	-1	1
-1	0	1	-1	1
0	1	0	0	0
0	2	-1	0	0

J	K	CLK	Q	$\overline{Q}$
0	-1	-2	0	0
1	-2	-1	0	0
1	-1	0	0	0
1	2	1	0	0
2	0	2	0	0
2	1	1	0	0
2	-2	0	0	0

10 (b)

Figure 10: Truth table for JK type switch with (a) ternary logic (b) penta logic

6. (2n+1)-ary Logic Simulation Results Using MATLAB

The set theoretic functions delineating multivalued logic are implemented using MATLAB software. The following figures show the functional relationships with inputs. The switching functions for three valued (ternary) and five valued (penta) are simulated using normal binary logic circuits.

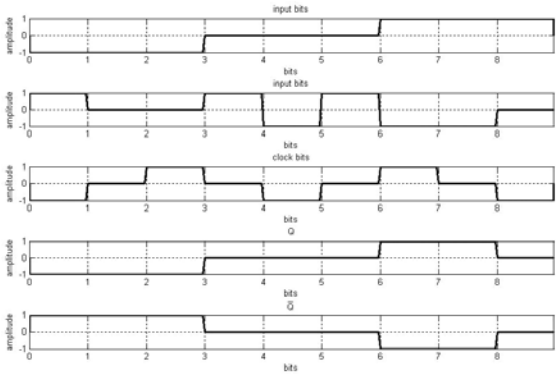


Figure 11: Ternary logic based clocked SR type switching function

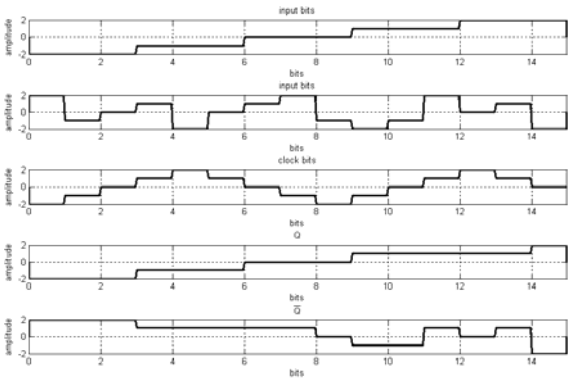


Figure 12: Penta logic based clocked SR type switching function

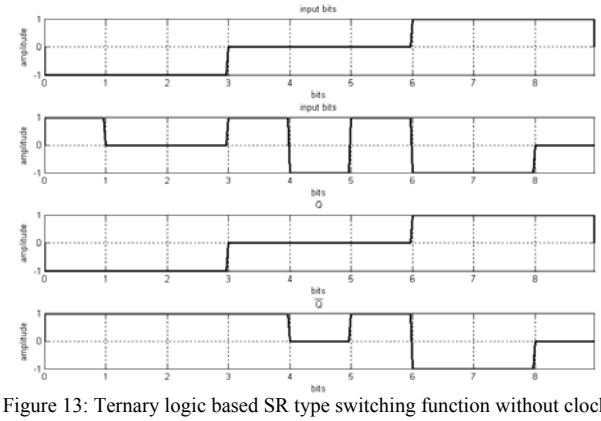


Figure 13: Ternary logic based SR type switching function without clock

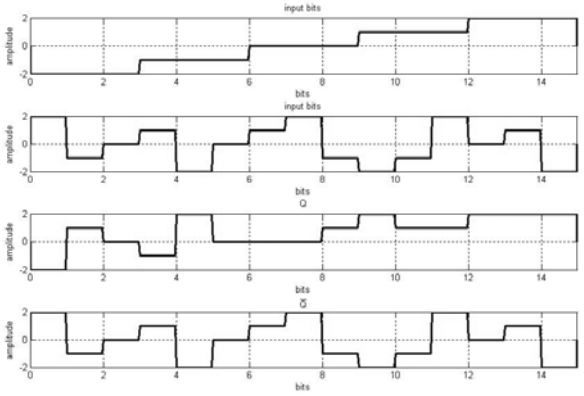


Figure 14: Penta logic based SR type switching function without clock

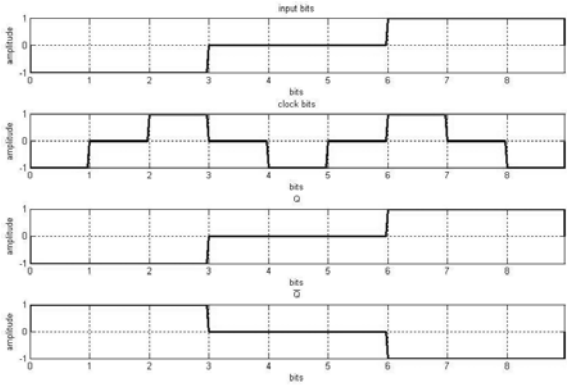


Figure 15: Ternary logic based D type switch function

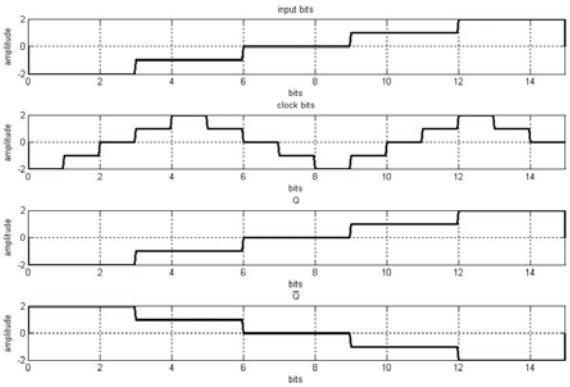


Figure 16: Penta logic based D type switch function

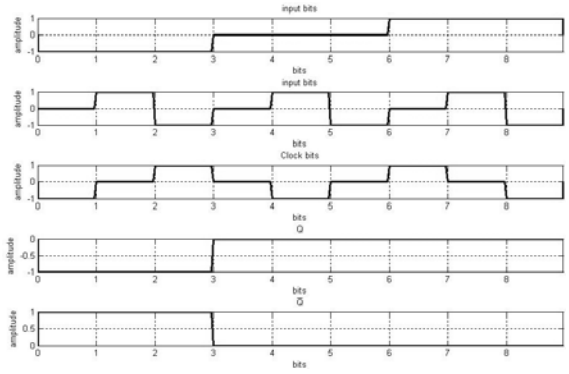


Figure 17: Ternary logic based JK type switching function

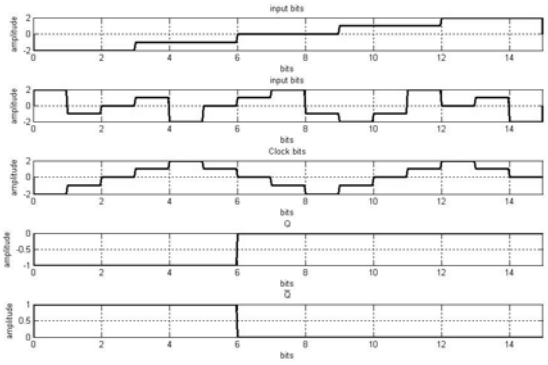
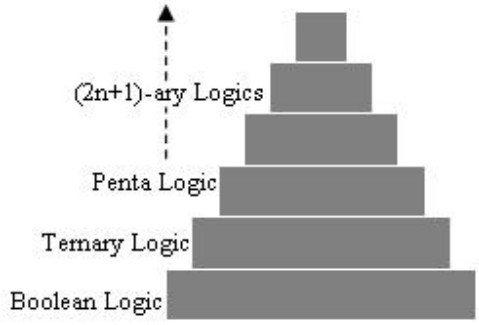


Figure 18: Penta logic based JK type switching function

6. Conclusions

With the application of multivalued logic we have achieved higher logic levels which intend much faster processing rates. The (2n+1)-ary logic is a hierarchical system of logics as shown in the following figure.



The switching functions for three valued (ternary) and five valued (penta) are simulated using normal binary logic circuits.

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