Design and Performance analysis of efficient bus arbitration schemes for on-chip shared bus Multi-processor SoC

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Summary
In the resource sharing mechanism of multi-processor SoC, the on-chip communication architecture plays an important role and directly affects the performance of SoC. The traditional shared bus arbitration schemes show the several defects such as bus starvation, and low system performance. In this paper, we discuss about the static & dynamic Lottery Bus algorithms. ATM switch architecture is also discussed which is based on a probability and uses an adaptive ticket value method to solve the problem of Lottery Bus arbitration schemes. The discussed architectures are modeled using VHDL, and simulated in ModelSim software. The comparison of these three arbitration schemes with respect of performance parameters such as average latency, acceptance rate & bandwidth waiting time are presented. The simulation results shows the ATM switch architecture decrease the bus request latency by 49%

Key words:
System-on-Chip (SoC), Bus Arbiter, VHDL, Multiprocessor

1. Introduction

SoC is a technology that integrates heterogeneous system components such as microprocessor, memory ,logic and DSPs into a single chip[1&3].The performance of multiprocessor systems depends more on efficient communication among processors and on the balanced distribution of computation among them, rather than on pure speed of processor[9].Although there are many possible communication architectures, shared bus is very popular in small number of processors system for its simplicity and area efficiency .The arbitration plays a crucial role in determining the performance of bus based system as it assign the priorities with which processor is granted the access to the shared communication resources. An efficient contention resolution scheme is required to provide fine-grained control of the communication bandwidth allocated to individual processor and avoid starvation of low priority component.

In this paper, the Lottery Bus algorithm such as static and dynamic lottery Bus algorithm are briefly discussed. Also the ATM switch architecture based on the probability bus distribution algorithm is discussed to solve the problem of Lottery Bus algorithm. The comparison of these three arbitration schemes with respect of performance parameters such as average latency, acceptance rate, bandwidth waiting time are discussed

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2. System on Chip Communication Architectures: A Review

2.1. Static Fixed Priority Algorithms

Static fixed priority is a common scheduling mechanism on most common buses [7&2].In a static fixed priority scheduling policy, each master is assigned a fixed priority value. When several masters request simultaneously, the master with the highest priority will be granted. The advantage of this arbitration is its simple implement and small area cost. The static priority based architecture does not provide a means for controlling the fraction of communication bandwidth assigned to a component. If masters with high priority requests frequently, it will lead to the starvation of the ones with low priority.

2.2 .TDM/Round-robin algorithm

Time division multiplexed (TDM) scheduling divides execution time on the bus into time slots and allocates the time slots to adapters requesting use of the bus[4-7]. Each time slot can span several physical transactions on the bus. A request for use of the bus might require multiple slot times to perform all required transfers. However, in this architecture, the components are provided access to the communication channel in an interleaved manager, using a two level arbitration protocol.

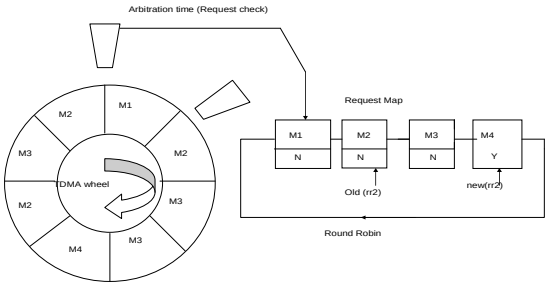

Figure 1: Time division multiplexed / Round Robin Architecture

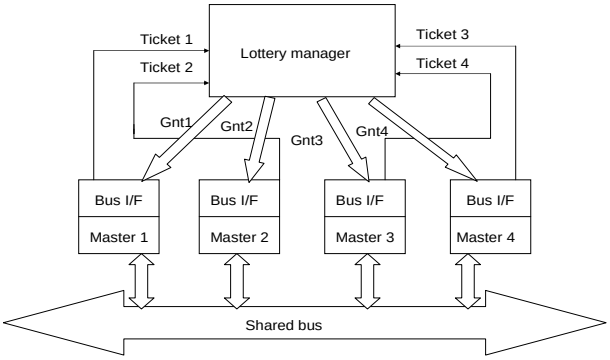

Figure 2: Lottery manager for a bus in a Lottery bus-based communication architecture

The first level of arbitration uses a timing wheel where each slot is statically reserved for a unique master. In a single rotation of the wheel, a master that has reserved more than one slot is potentially granted access to the channel multiple times. If the master interface associated with the current slot has an outstanding request, a single word transfer is granted, and the timing wheel is rotated by one slot. To alleviate the problem of wasted slots, a second level of arbitration is supported. The policy is to keep track of the last master interface to be granted access via the second level of arbitration, and issue a grant to the next requesting master in a round-robin fashion, at figure 1, the current slot is reserved for M1, but it has no data to communicate. The second level increments a round-robin pointer rr2 from its current position at M2 to the next outstanding request at M4.Advantage of this algorithm that it is easy to implement. Disadvantage is that it leads to the mistake of data transfer

2.3 Static Lottery bus Communication Architecture

The core of the LOTTERYBUS architecture is a probabilistic arbitration algorithm implemented in a centralized “lottery manager” for each bus in the communication architecture[4][5]. The architecture does not presume any fixed communication topology. Hence, the various SoC components may be interconnected by an arbitrary network of shared channels or a flat, system-wide bus.

The lottery manager accumulates requests for ownership of the bus from one or more masters, each of which is (statically or dynamically) assigned a number of “lottery tickets,” as shown in figure 2. The manager pseudo-randomly chooses one of the contending masters to be the winner of the lottery, favoring masters that have a larger number of tickets, and grants access to the chosen master for a certain number of bus cycles. Multiple word requests may be allowed to complete without incurring the overhead of a lottery drawing for each bus word. However, to prevent a master from monopolizing the bus, a maximum transfer size is used to limit the number of bus cycles for which the granted master can utilize the bus Also, the architecture pipelines lottery manager operations with actual data transfers, to minimize idle bus cycles.
The inputs to the lottery manager are a set of requests (one per master) and the number of tickets held by each master. The output is a set of grant lines (again one per master) that indicate the number of words that the currently chosen master is allowed to transfer across the bus. The arbitration decision is based on a lottery. The lottery manager periodically (typically, once every bus cycle) polls the incoming request lines to see if there are any pending requests. If there is only one request, a trivial lottery results in granting the bus to the requesting master. If there are two or more pending requests, then the master to be granted access is chosen using the approach described next [8].

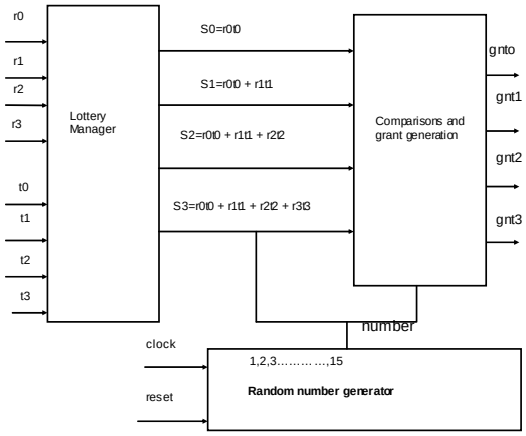

Figure 3 Static Lottery bus communication architecture

The architecture (fig 3) is model using VHDL for four masters. Ticket values are keeping fixed. Figure 4 shows the waveforms for the discussed architecture. Here t0, t1, t2 & t3 are tickets values and gnt0, gnt1, gnt2 & gnt3 are grant signals of the master processor. Signal n1 is random number generated signal and signal h0, h1, h2 &h3 are calculated value for the master or processor according to its ticket value and request signal r.

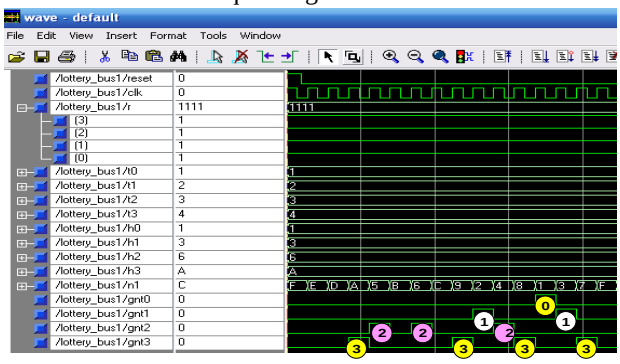

Figure 4: Waveform with VHDL for static Lottery bus

2.4 Dynamic Lottery bus architecture

In this architecture (fig 5), the inputs to the lottery manager consist of a set of request lines (r0r1r2r3), and the number of tickets currently possessed by each corresponding master that are generated by ticket generated by ticket generator[8]. Therefore, under this architecture, not only can Range of current tickets vary dynamically, it can take on any arbitrary value (unlike the static case, where it was fixed). Therefore at each lottery, the lottery manager needs to calculate for each component C_i, the partial sum $\sum_{j=1}^{n} r_j * t_j$. This is implemented using a bit wise AND operation and tree of adder, as shown in Fig 4.The final result, T=r0t0+r1t1+r2t2+r3t3, defines the range in which the random number must lie. A limitation of this implementation is that distribution of the resulting random number is not uniform. The rest of the architecture consists of comparison and grant hardware, and follows directly from the design of the static lottery manager.

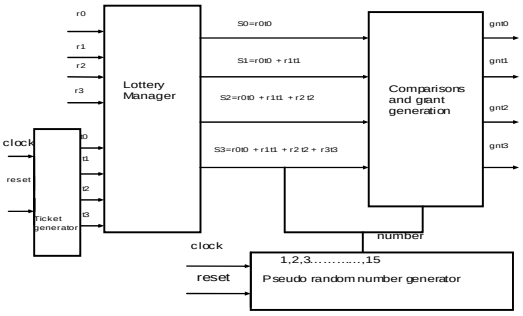

Figure 5: Lottery manager architecture with dynamically varying tickets

The architecture is modeled using VHDL. Ticket values are keeping varying. Figure 6 shows the waveforms for the discussed architecture. Here t0, t1, t2 & t3 are tickets values and gnt0, gnt1, gnt2 and gnt3 are grant signals of the master processor. Signal n1 is random number generated signal and signal s0, s1, s2 and s3 are calculated value for the master or processor according to its ticket value and request signal r.

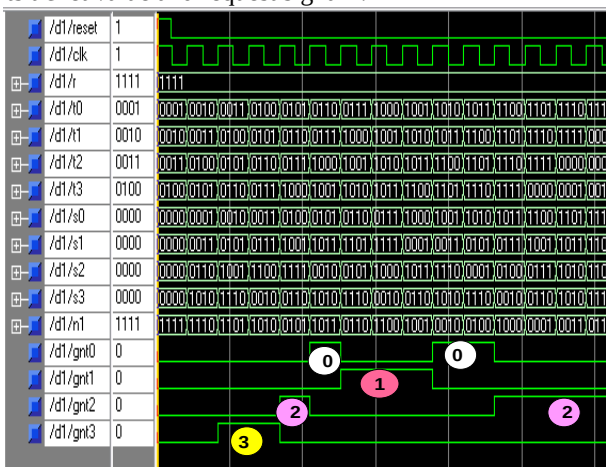

Figure 6: Waveform with VHDL for Dynamic Lottery bus

Advantages of Static lottery Bus architecture is that all the masters that are requesting gain the control of bus
Disadvantages of dynamic lottery bus architecture is that if the pseudo random number is greater than total ticket value then none of the masters will get the grant signal. Master having low ticket value has a large average latency

2.5 ATM switch architecture

In this arbitration algorithm, it accepts three parameters (Requests, Tickets, Adaptive signal) for the input of arbiter. Request and Ticket are the input for the static bus distribution. Adaptive signal value is used as an additional input to improve the probability of the bus grant. This adaptive signal value is transmitted from the master that requires the bus grant more than another master because of the stressful traffic. Since we do not know which IP is used for the shared bus in advance of the SOC design, the adaptive signal can be fixed by the specific parameter. In this paper, the master counts the buffer position storing the ATM cell and if the data approaches to the limited amount, the adaptive signal is generated to improve the drawing probability [5][6].

$$P(Ci) = \frac{r_i(t_i + a_i)}{\sum_{j=1}^{n} r_j * (t_j + a_j)}$$

Above equation shows the shared bus probability for each master. The current pending request and ticket value is used to obtain the shared probability of each C_i. In order to improve the probability of the master, a_i values are obtained from the look up table and two of the master requests accomplish the bit-wise AND operation by the values i a is the additional ticket value to solve the problem that if the total ticket value is lower than the pseudo random value, the bus is assigned to the master of the low priority by the priority inversion.

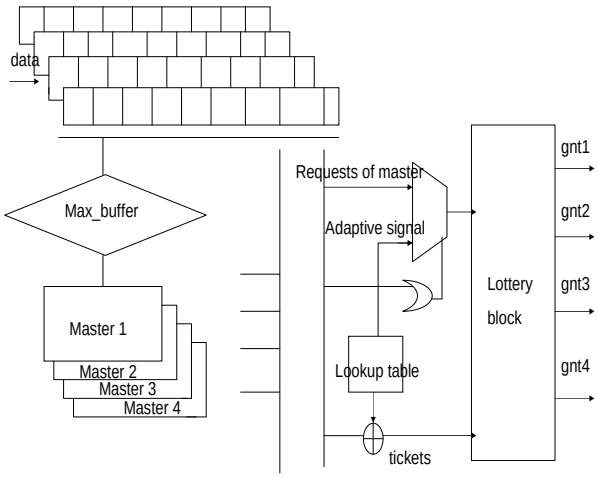

Figure 7: ATM Switch architecture

The architecture (figure 7) is modeled using VHDL. Figure 8 shows VHDL result for ATM switch architecture arbiter.

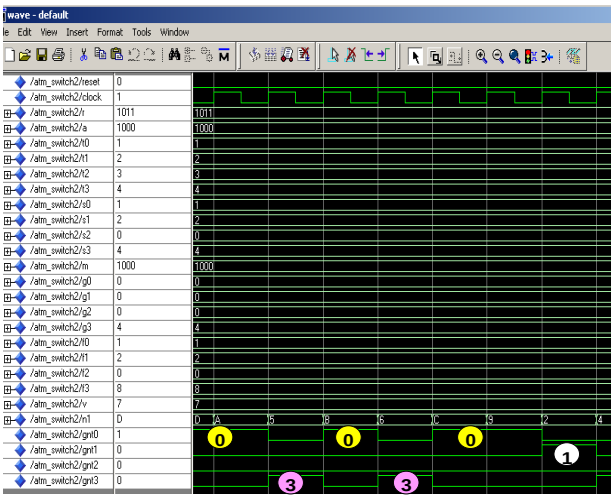

Figure 8. Waveform with VHDL for ATM switch architecture

Advantages of ATM switch architecture is that the adaptive signal is used to solve the problem that the characteristics of LFSR are disappeared if the pseudo random number is bigger than total ticket value

3. Results

The discussed three algorithms are designed using VHDL and simulation results are presented in figure no 4, 6 &8. This scheme tested for performance parameter by using VHDL test bench and comparative results are presenting

below. While testing the scheme, the length of data is not considered and that's why grant signal is consider only for one cycle.

3.1 Average Latency (Cycles/word)

Average Latency (Cycles/word)of every processor Under different arbitration schemes:-

Table 1: Average Latency (Cycle/ Word)

Bus Arbitration schemes	M0	M1	M2	M3
Static Lottery Bus	11.2	2.1	2.3	1.2
Dynamic Lottery Bus	1.93	2.93	2.53	2.9
ATM switch Architecture	5.8	1.3	1.6	1.14

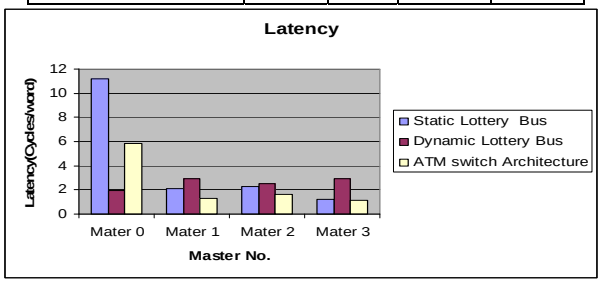

Figure 9: Comparative Graph for Average Latency (Cycle/ Word)

3.2 Acceptance rate

Acceptance rate of every processor under different arbitration schemes

Table 2: Acceptance Rate

Bus Arbitration schemes	M0	M1	M2	M3
Static Lottery Bus	24.9%	24.9%	24.9%	24.9%
Dynamic Lottery Bus	24.9%	24.9%	24.9%	24.9%
ATM switch Architecture	30.3%	20.3%	23.1%	23.1%

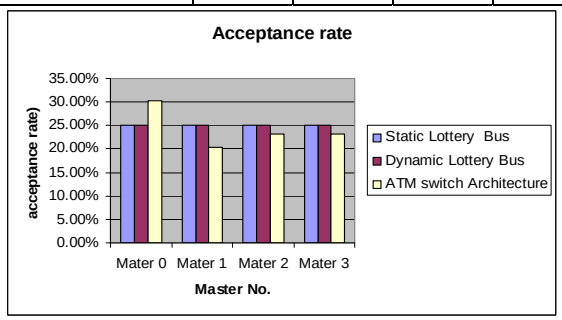

Figure 10: Comparative Graph for Acceptance Rate

3.3 Average waiting time

Average waiting time (ps) of every processor under different arbitration schemes.

Table 3: Average waiting Time (Pico Sec)

Bus Arbitration schemes	M0	M1	M2	M3
Static Lottery Bus	373.33	233.33	73.33	206.67
Dynamic Lottery Bus	40	133.33	220	93.33
ATM switch Architecture	6.67	146.67	106.7	160

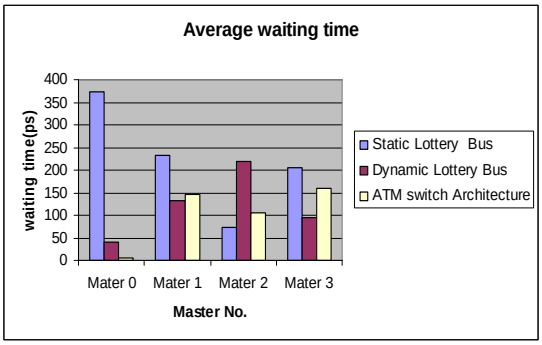

Figure 11. Comparative Graph for Average utilization Bandwidth

3.4 Average Bandwidth

Table 4: Average waiting Time (Pico Sec)

Bus Arbitration schemes	M0	M1	M2	M3
Static Lottery Bus	7.19%	38.09%	51.89%	2.83%
Dynamic Lottery Bus	15.29%	53.01%	10.9%	20.71%
ATM switch Architecture	13.83%	22.47%	35.2%	28.5%

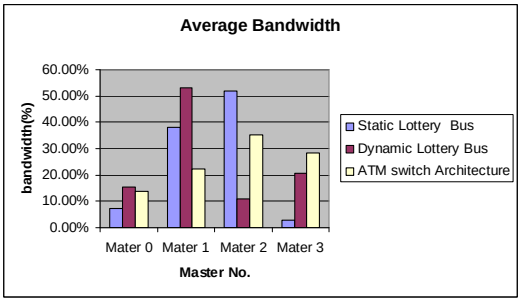

Figure 12: Comparative Graph for Average utilization Bandwidth

In the above analysis four processor are taken into consideration. Label M0, M1 etc. indicate Master (Processor) 0, 1 and so on.

4. Conclusion

Static and Dynamic Lottery Bus architecture solve the problem of priority algorithm but it shows some drawback. To overcome the drawback of Lottery Bus architecture the ATM switch architecture is presented that is based on probability bus distribution Algorithm. In this paper, author describes new high-performances communication architecture for system on chip designs. This architecture uses an adaptive ticket value method. The architectures are model in VHDL and some of the simulation results are presented taken by Modelsim simulation software and found satisfactory. By writing the test benches, various performance parameters such as latency, bandwidth**,** acceptance rate **a**nd average writing time are calculated & presented. The simulation results shows the ATM switch architecture decrease the bus request latency by 49%

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