Folding ADC Design for Software Defined GSM Radio-Mobile Station Receiver

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Summary
Software Defined Radio is emerging as a new trend in the field of wireless communication. The Software Defined Radio is aimed for providing single radio unit, which can operate on different wireless and mobile standards only by modifying its software. The study of wireless communication systems reveals that integration of various wireless communication technologies is a goal of next generation communication system and it is a major challenge. Multimode, multiband Software Defined Radio can provide one of the best solutions for designing a single radio that can accommodate such different standards. Total flexibility and reconfigurability can be achieved when all radio functions can be implemented through software. This is the basis of ideal Software Defined Radio, where A/D/A conversion is carried out at RF stage of the radio immediately after the antenna. Role of ADC is very critical in software radio. ADC with high resolution and performance is essential. A 17 bit ADC with conversion rate greater than MSPS is required for Software Defined GSM Radio receiver. The work presented in this paper contributes in the design of high performance Folding analog to digital converter for digitization at RF stage in Software Defined GSM Radio mobile receiver application. Results of the work specify the critical specifications of this ADC architecture. Results of this work also specify the critical specifications of internal components used to build the Folding ADC architecture for Software Defined GSM radio receiver. The work is supported by MATLAB simulation platform.

Keywords:
SDR, GSM, ADC, MS, MDAC

1. Introduction

Next generation mobile communication systems mainly focus on seamless integration of existing wireless technologies and standards such as GSM, wireless LAN, and Bluetooth etc. Goal of next generation wireless system is defined to have a single radio that will accommodate different wireless standards and operate on different frequency bands [1], [2]. These standards have different system specifications and operational requirements therefore it is very difficult to integrate them to have a single radio system. State of art programmable digital radios are not able to satisfy this goal. In this scenario, Software Defined Radio (or Software Radio & abbreviated as SDR) can be thought as a better solution over this problem. In Software Defined Radio, all radio functionalities are implemented using software. Two hallmarks of Software Radio architecture, as described in [3], are placement of A/D/A converter as close to antenna as possible, and definition of radio functions in software. This requires digitization of wide band radio frequency communication signals that are accompanied by channel noise and interference. Simple model for Software Radio, as suggested in [4], is as depicted in figure 1. In this paper, high performance ADC viz. Folding ADC is designed for digitization at RF in Software Defined GSM radio mobile station (abbreviated as MS) receiver and its performance is analyzed analytically.

2. ADC Specifications for Software Defined GSM Radio Receiver

Analog to digital converter (abbreviated as ADC) is one of the key components in the receive signal path of a wireless communication receiver. ADC specifications are architecture dependent, and also function of performances of circuit elements used to build an ADC. ADC specifications [5] for digitization at RF in Software Defined GSM Radio receiver as estimated are listed in table 1. ADC characterization results for MS are depicted in table 2 [5],[6],[7].These results show that ADC, characterized for sampling at RF, is required with high figure of merit (F), high power consumption (P_{diss}). Noise Figure and Third order intercept point are estimated using GSM-900 standard, as specified in [8].

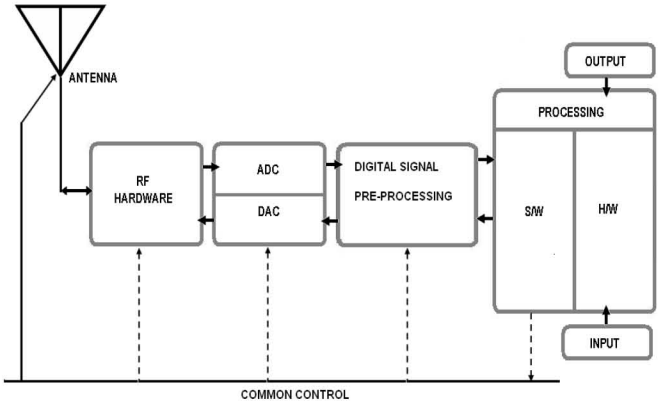

Fig 1: Simple Model of Software Radio

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Table 1: ADC Specifications for Ideal Software Defined GSM Radio MS Receiver

Sr.No.	*Parameters*	*Value*
1.	Full scale range (FSR)	5 Volts
2.	ADC power supply voltage (V_{cc})	+5 Volts
3.	Master reference voltage (V_{ref})	+5 Volts
4.	Input Signal Frequency (maximum)	960 MHz
5.	Sampling rate (Nyquist Sampling at Nyquist Rate)	1920 MSPS
6.	Maximum conversion time of ADC	520 pS
7.	Number of bits	16 -18
8.	Noise figure	42.39 dB
9.	Third order intercept (IIP3)	-99.00 dBm
10.	Sample time uncertainty	5.06 pS

Table 2: Characterization of ADC for Digitization at RF Stages for MS Receiver

Sr. No.	*Characterization*	*ADC at RF (MS)*
1.	SNR bits	16 bits
2.	P	125829120000000
3.	P_{diss}	0.04587 W
4.	F	2743168083714846.30

3. Design of 17 bit Folding ADC

Folding ADC employs a technique of folding an input signal prior to quantization. Folding technique is used to achieve high resolution by reducing number of comparators than that required in Flash ADC architecture. In this ADC architecture, number of comparators required is reduced by the degree of folding and at the same time advantages of high speed and low converter latency are maintained. Various issues related with folding operation are as discussed next. Folding characteristic is typically piece-wise linear input output characteristic. Based on these requirements, two type of characteristics are specified viz. saw-tooth and triangular. Saw-tooth transfer characteristic is difficult to realize. Saw-tooth waveform suffers with problem of discontinuity [9]. Slew rate increases infinitely at a point of discontinuity. Most commonly triangular transfer characteristic is preferred. This characteristic also suffers with problem of rounding effects at higher frequency. The rounding effect results in loss of resolution. Figure 2 depicts simulated folding characteristics. Folding operation is performed either in serial fashion or parallel fashion. Parallel folding technique achieves high speed but number of differential amplifiers grows exponentially with increase in number of bits to be resolved. In this technique, each parallel channel uses a separate folding circuit. Different analog Folding ADC architectures that inherits parallel nature of preprocessing techniques, used for folding operations, are reported in literature [9], [10], [11]. 'Serial Signal Folding' is efficient in multi step folding operation and it employs cascade stages. Analog residue signal forwarded by folding circuit should not affect overall linearity of ADC. Improper operation of folding circuit can add errors in ADC operation. Effect of gain error of folding circuit on its output is depicted in fig. 2 (d). This introduces error in ADC circuit operation due to loss of resolution. Reduction rate of number of comparators is equal to a folding rate. Folding rate fixes number of coarse bits. Inaccuracy in gain, offset and breakpoint of analog circuits will eventually limit overall linearity. High bandwidth of folding circuit impose strong trade-offs among speed, gain and power dissipation. Errors in preprocessing put constraints on ADC resolution. Design of sub ADCs plays critical role in the folding ADC performance. In this design, for the selection of coarse bits (N1) and fine bits (N2), two major factors are considered and are as described next.

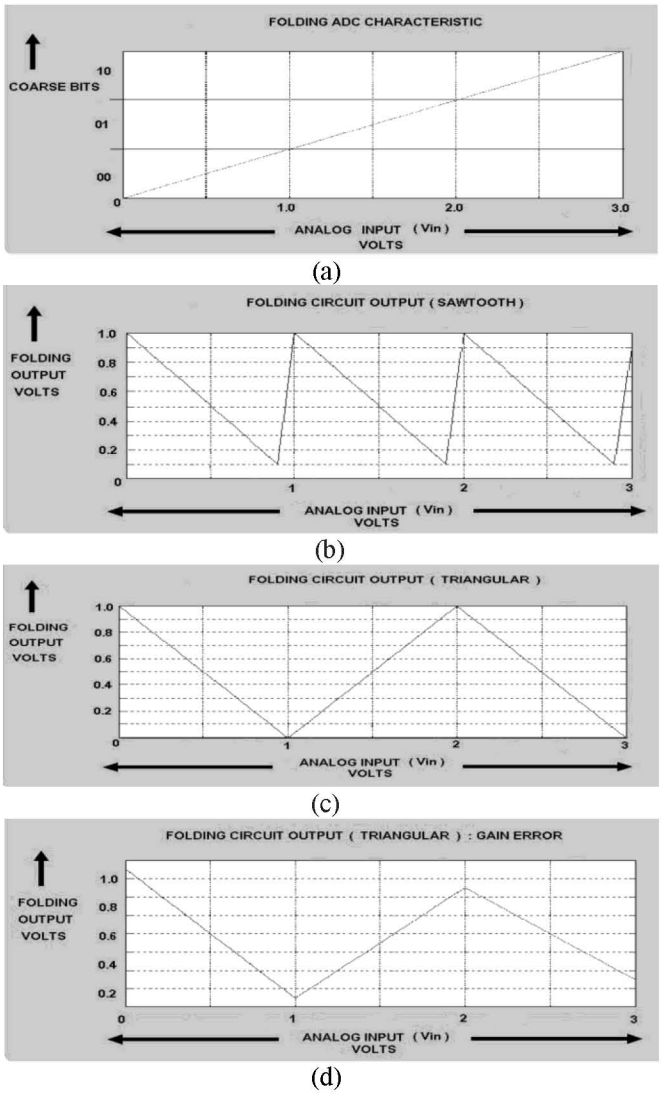
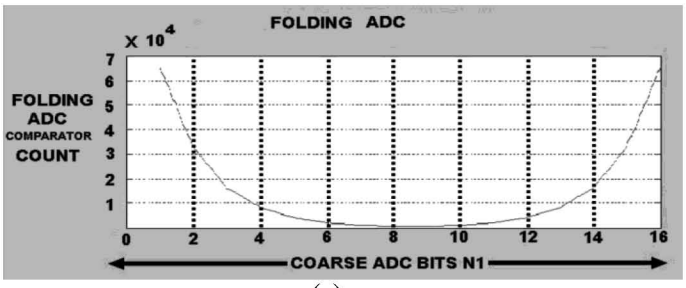
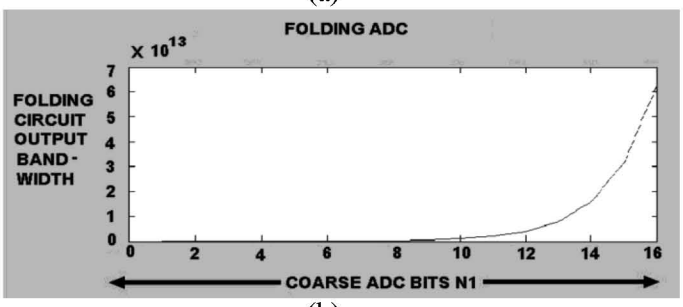


Fig 2: (a) Input Signal to Coarse and Fine Quantizer (b) Simulated Saw Tooth Folding Characteristic, (c) Simulated Triangular Folding Characteristic, and (d) Effect of Gain Error.



(a)



(b)

Fig 3: Coarse Quantizer Resolutions vs. (a) Total Comparator Count and (b) Output Bandwidth of Folding Circuit

These parameters are low comparator count in Folding ADC, and low output bandwidth of folding circuit. High bandwidth of folding circuit impose strong trade-offs among speed, gain and power dissipation. Figure 3 depicts graphical relationship between total number of comparators required for folding ADC and number of coarse quantizer bits. Figure 3 depicts that for lower value of the output bandwidth the comparator count is very high. So design must be optimized by compromising these two factors. For the proposed 17 bit ADC, lowest possible comparator count is 766. Apply criterions of minimum output bandwidth of folding circuit, coarse quantizer of 8 bits and fine quantizer of 9 bits is justified. Folding rate fixes number of coarse bits. Inaccuracy in gain, offset and breakpoint of analog circuits will eventually limit overall linearity.

4. Results

Table 3 depicts the results of analytical model for 17 bit Folding ADC design. Serial folding technique is employed for the analysis purpose. These design values typically considered the standard Flash ADC architecture as coarse and fine quantizer. This table depicts the estimated design values of the internal components and devices those are used for folding ADC Design. This design suffers with requirements of total 768 resistors with single resistor value is well below than an ohm. At the same time 766 comparators with very low offset voltage, bias current, propagation delay, and input capacitance are essential for the design. As large number of comparators is required in

Table 3: Design Summary of Folding ADC Design

Course Quantizer [8 bit Flash ADC]		
Sr.No.	***ADC Parameters***	***Value***
1.	LSB voltage (Minimum value) (V_{LSB})	19.53125 µV
2.	Number. of comparators	255
3.	Number. of resistors	256
4.	Resistor Ladder (Maximum Value)	20.32 Ω
5.	Single resistor Value in the resistor ladder	0.079 Ω
	Comparator Design	
6.	Bias current (for INL < ½ LSB)	5.8427 X 10^{-8} A
7.	Gain	42.144 dB
8.	Offset	V_{LSB} > Vos
9.	Dynamic Range	48.10 dB
10.	Propagation Delay for Lower Comparator	0.115 ns
11.	Propagation Delay for Upper Comparator	0.225 ps
12.	Slew Rate (Output transition between 0 to 2.5 V)	10869565217.4 V/s
13.	Total Input Capacitance	3.31 pF
	Digital Design	
14.	ROM size	256 x 8 bits
15.	Number of gates	> 256
Fine Quantizer Design [9 bit Flash ADC]		
16.	LSB voltage (Minimum value) (V_{LSB})	38.4453125 µV
17.	No. of comparators	511
18.	No. of resistors	512
19.	Resistor Ladder (Maximum Value)	0.499 Ω (Max)
20.	Single resistor value in the resistor ladder	974.8 mΩ
	Comparator Design	
21.	Bias current (for INL < ½ LSB)	1.1755 X 10^{-9} A
22.	Gain	96.26 dB
23.	Offset	V_{LSB} > Vos
24.	Dynamic Range	54.11 dB
25.	Propagation Delay for Lower Comparator	0.115 ns
26.	Propagation Delay for Upper comparator	0.113 ps
27.	Slew Rate (Output transition between 0 to 2.5 V)	10869565217.4 V/s
28.	Total Input Capacitance	6.47 fF
	Digital Design	
29.	ROM size	512 x 9 bits
30.	Number of gates	> 512
Folding Circuit Design		
31.	Folding factor	256
32.	Folding amplifiers	255
33.	Output bandwidth of the cascaded folding circuit	245.76 × 10^9 Hz

coarse quantizer and fine quantizer, the propagation delay variation between upper comparator and lower comparator is observed. This may generate an error in the output code. Digital section typically includes ROM based encoder. Thus these results, most importantly, specify the performance limiting factors of the folding ADC architecture.

5. Conclusion

Study of 'Folding ADC for Software Defined Radio receiver' reveals that in Folding ADC architecture number of comparators required is 766 for 17 bit ADC. This count is high for battery operated receivers. Concept of additional analog signal preprocessing is proved to be useful for reduction in comparator count as compared to Flash ADC architecture. This preprocessing requires additional 255 differential amplifiers. Performance of ADC depends on performance of comparators used in coarse quantizers and differential amplifiers used in analog preprocessing. Comparator specifications, such as resolution, dynamic range are somewhat relaxed for coarse quantizers but not so specifically for fine quantizer. Output bandwidth of folding circuit is also very high due to large number of folding circuit requirement. Large number of comparators is a crucial factor for this 17 bit Folding ADC. This large number of comparators imposes critical performance burdens on the other devices and components required to build such ADCs. High input signal frequency also critically imposes burden of front end ADC components. Thus the Folding ADC architecture is less suitable for receiver application for GSM-900 standard when used for digitization at RF stage of Software Defined Radio mobile station receiver. ADC that consists of less number of comparator should be used for digitization at RF stage of the Software Defined GSM Radio – mobile station receiver.

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