New Approaches to Routing Techniques of MANET Node for Optimal Network Performance

M.Ramakrishnan[1], S.Shanmugavel[2]
1, Dept of Electronics and Communication Engineering, SSN College of Engineering, Chennai 603110,
2, Dept of Electronics and Communication Engineering,
College of Engineering, Anna University, Chennai 600025, India.

Abstract

Mobile Adhoc Network is a collection of wireless mobile nodes forming a temporary network without the aid of any established infrastructure. In wireless networks, routing is undoubtedly one of the most demanding areas where flexibility and cost are of significant importance. The aim of the current work is the study of various routing techniques for MANET nodes to obtain the route through which data is to be transferred to the destination with maximum throughput. The first technique is to study and implement the change over of routing protocols from DSR to AODV using Glomosim simulator. In second routing technique we have adopted self healing routing methodology for ad hoc on demand routing protocol with shortest path using the Glomosim. We have proposed the third routing technique which is an adaptable routing strategy for MANET node with reconfigurable FPGA. One among the popular protocols like DSDV, DSR, AODV and TORA is configured in the MANET node on the fly using a reconfigurable FPGA. Therefore, the individual protocols are modeled using VHDL and implemented in FPGA and finally integrated using an Automatic Throughput Control algorithm (ATC). This ATC selects the required routing protocol based on the throughput value. It works on the principle of throughput calculation and comparison with a minimum threshold value to initiate the protocol selection process. Therefore then and there, by shifting to the effective protocols on the fly, the throughput obtained is made consistent. Hence an automatically reconfigurable node for MANET application is a trustworthy solution. The maximum speed of operation for the proposed routing architecture is about 138.64 MHz. We have synthesized the code using Xilinx Virtex II (V200EFG256-7) FPGA.

Keywords: MANET, DSDV, AODV, DSR, TORA, Reconfigurable Architecture, FPGA (Field Programmable Gate Array) etc

1 Introduction

The term node is defined as a device and it may be a laptop, personal digital assistant or cellular mobile phone. It runs a routing protocol and exchanges data with other nodes within MANET [1]. A node has at least one wireless interface connecting it to the MANET network. In this work, node means source or destination and router node means intermediate node and routing section or router means the add-on card section containing routing protocol in FPGA and PROM (Programmable Read Only Memory) memories etc. Routing is the most fundamental research issue in ad hoc networking. Routing protocols for ad hoc networks must deal with limitations such as high power consumption, low bandwidth, high error rates and arbitrary movements of nodes etc. Generally, protocols can be classified into three types in which DSDV (Destination Sequence Distance Vector) belongs to table driven or proactive and AODV (Adhoc On demand Distance Vector), DSR (Dynamic Source Routing) and TORA (Temporally Ordered Routing Algorithm) belong to on demand or reactive categories.
Though significant work has been carried out in the routing issues, there is no specific routing protocol developed that works well for all the scenarios [2]. The path obtained using any protocol for different network condition is a variable one [3]. Most of the related works on performance comparison say throughput is varying for different occasion and different protocols [4]. Hence we study and propose three routing techniques to improve the performance and efficiency of MANET. They are Dynamic Reconfigurable Routing, Self Healing Routing and Adaptive Routing. The first proposed technique is simulated using Glomosim for change over of routing protocols from DSR to AODV and vice versa whenever the throughput plunges into low value. This technique proved that by reconfiguring the MANET node for different protocols, it is possible to keep the throughput consistent. Another routing technique is further proposed in this chapter called self healing routing technique of ad hoc on demand routing protocols using Glomosim. During packet transmission, this work monitors the existence of shortest path and uses the same so that packet delivery rate is increased and so is throughput. In the third adaptive routing technique a reconfigurable node using reconfigurable FPGA is designed for popular routing protocols like DSDV, AODV, DSR and TORA. For the selection of various

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routing protocols, an Automatic Throughput Control algorithm (ATC) is also proposed. Dynamic selection of routing protocols brings out the consistency in throughput with respect to network conditions.

The various sections in this paper are organized as follows: Section 1 gives a brief introduction to MANET and the routing protocols including the problem statement and objectives. Section 2 explains literature review of performance evaluation and comparison of various protocols and the various other methods in literature of obtaining high throughput. Section 3 and Section 4 discuss implementation details for the first two. Section 5 presents the third method of change over of protocols using reconfigurable FPGA. Section 5 also presents the implementation of four protocols and ATC in Hardware Description Language (HDL) and simulation and synthesis reports. Section 6 describes conclusions and future work.

2 Literature survey

The performance comparison of various protocols in literature reveals that

- DSDV is most suitable for small networks where topology changes are limited.
- AODV has the best all round performance and suitable for maximum QOS parameters considered.
- DSR is suitable for networks with moderate speed of nodes, lowest control over head, low BW (Bandwidth) and power constraint network.
- TORA is suitable for multicasting, large no of nodes, highly dynamic environment.
- Characteristics and efficiency of one protocol outperform the other in different network conditions.
- The optimal routing strategy depends on the underlying network topology and its rate of change and traffic pattern.

The above performance comparison of protocols was the result of the experiments and simulations conducted using software at Huaxhong University of Science and Technology, Wuhan, China. There is no best ad hoc routing protocol suitable for all circumstances [5]. Hence, some new routing strategy like adaptable routing [6, 7, 8, 9, and 10] has to be applied to MANET node for higher and consistent throughput. In fact, what we need is a single protocol that gives the best features of all in a suite of reactive and proactive protocols. Therefore, three routing technique are proposed. The first technique DRR (Dynamic Reconfigurable Routing) is to study and implement the change over of routing protocols from DSR to AODV and vice versa using Glomosim. In the second routing technique we have adopted self healing routing methodology to find shortest path for ad hoc on demand routing protocol. We have proposed the third routing technique which is an adaptable routing strategy for MANET node with reconfigurable FPGA.The proposed reconfigurable node will be based on effective selection of any of four protocols, most suitable for existing network condition. The selection is done by another algorithm called ATC.

3 Implementation of DRR

The first proposed technique [11] is simulated using Global Mobile Simulator (Glomosim). DRR method monitors the throughput continuously. When the throughput value plunges down due to sudden change in mobile speed or due to increase in number of nodes in real time scenario, Glomosim is modified to adapt to different protocol to maintain the throughput. With the dynamic adaptation of DSR or AODV, DRR maintains the throughput level of value 3600 bytes per second in which 256 bytes correspond to a packet. In the performance graph shown in figure 1, between node speed and throughput, the DRR goes to maximum using DSR upto 4m/s and using AODV from 4m/s speed to 20m/s. In the figure 2, between no of nodes and throughput, the DRR goes to maximum using AODV upto 200 nodes and using DSR from 200 to 700 nodes .Therefore by manipulating configure.sys file in Glomosim, we are able to achieve max throughput for all the speed upto 20m/s. Likewise performance are studied for throughput versus terrain size and pause time etc.

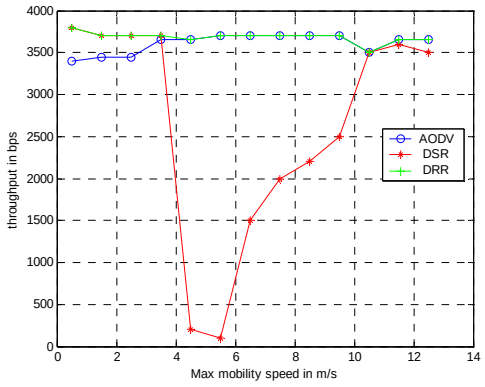


Figure 1: Node speed vs Throughput for AODV and DSR

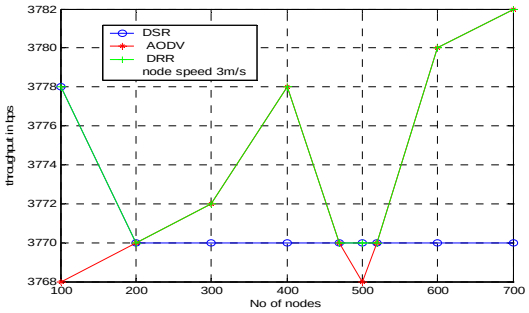


Figure 2: Number of Nodes vs Throughput for AODV and DSR

4 Self healing routing technique

Second routing technique proposed is called self healing routing technique of ad hoc on demand routing protocol [12]. This explains an algorithm that, whenever for a route already obtained using a routing protocol, a short path is also available subsequently, the new route will be considered so that further transmission of packets will increase throughput. AODV protocol is used with this approach.

Paths generated by the on-demand ad hoc routing protocols can deviate far from the shortest path. Because of the mobility of the nodes in ad hoc networks, the shape of routing paths may change significantly while the connectivity is intact. Most of the previously proposed on-demand routing schemes do not initiate a new path discovery process until there is a link failure (a node fails or moves out of range). This leads to reduction in throughput and increases end to end delay. The proposed self healing routing technique will monitor the network for topology changes and gradually start self healing the link before it is getting broken. Different types of routing protocols work in different manner, we need to have different algorithms for short-cut identification and reaction. Path aware self healing distance vector (Pa-sh-dv) algorithm works with AODV. The self healing technique is simulated using Glomosim and the results are obtained for packet delivery rate versus node speed between 0 m/s and 35m/s. Both AODV and AODV-SH are simulated. The results show the increase in delivery rate for both single source single destination and multi source multi destination category. In figure 3, at lower speed for both protocols delivery rate may be same but once speed picks up, delivery rate for plain AODV goes down whereas the delivery rate is maintained for AODV- SH. Also in the figure 4, the same effect is witnessed in the graph for multi source multi destination (MSMD).

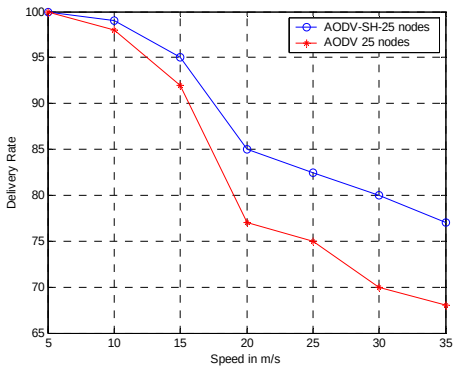


Figure 3: Delivery rate vs Node speed in m/s

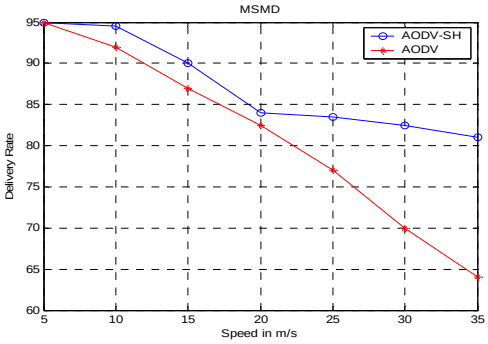


Figure 4: Delivery rate vs Node speed in m/s for MSMD

5 Adaptable routing technique

In this work a reconfigurable MANET node using reconfigurable FPGA is designed for popular routing protocols like DSDV, AODV, DSR and TORA. For the selection of various routing protocols ATC is also proposed. Further all these protocols and ATC are individually hardware implemented using VHDL and the code is synthesized using Xilinx Project Navigator. The implementation details and their results are discussed in this section.

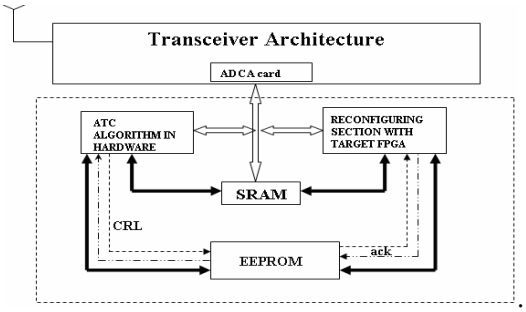


Figure5: Transceiver architecture of node

Before implementing the protocols, the node's architecture should be understood which is shown in the figure 5. Other than transmitting and receiving the data and routing packets through its wireless interface, the node contains an integral part for routing section. This routing section or router is shown in the dotted lines forming an add-on card (ADCA). Routing section or router is used to discover the route for sending its own data to other nodes or to process the data packet from other nodes. The routing section or router consists of PROMs, target FPGA and ATC unit. The EEPROM is a bank of PROM memories to hold the implemented details of the routing protocols.

5.1 Routing section architecture using FPGA

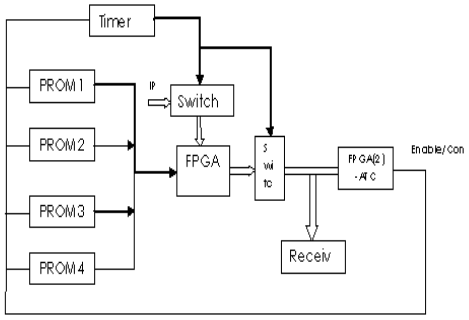


Figure 6: Proposed reconfigurable routing section architecture

The detailed block diagram of the reconfigurable routing section architecture is shown in the figure 6. The hardware synthesized code (JTAG file) for four protocols are downloaded into four separate PROMs. The PROM memory will contain the stream of bits as JTAG files. The procedure of obtaining JTAG files for every protocol is understood from the references [13, 14]. The control unit with ATC algorithm which is present in another one time programmable nonvolatile FPGA is responsible for finding which protocol is to be downloaded into target FPGA based on the throughput. Whenever a particular PROM is enabled as per the ATC, that protocol's JTAG file is transferred into target FPGA for configuration. Once the target FPGA is configured, it starts working on the protocol to find the route. The ATC algorithm is a systematic procedure briefed in section 5.2. ATC is also implemented and downloaded into another one time programmable nonvolatile FPGA.

The following steps are used for the implementation of the new routing section or router architecture:

- VHDL modeling is done for four routing protocols namely DSDV, DSR, AODV and TORA individually; simulation and synthesis are done using Modelsim and Xilinx project navigator respectively.
- The synthesized codes are brought out as PROM files or JTAG files (e.g. PROM_DSR, PROM_AODV etc) for the above four protocols.
- These different JTAG files are loaded into four separate programmable ROM memories.
- ATC functions are modeled using VHDL and simulation and synthesis reports are obtained.

Normally a MANET node, as a source node when in need of transmitting data packets invokes a particular routing protocol in the routing section of add-on card. The router or routing section works on the particular protocol and collects the route before sending the data packet. The procedure of forming the route request packet and sending route request etc are as per the routing protocol invoked in the router. But route request [RREQ] packet should contain the information in one of its field about the routing protocol to be used by the router node to find the route. The source node does not use one routing protocol continuously for ever because of change in network conditions. Instead in the reconfigurable routing section, present protocol at the source will be changed as per the throughput value. This change over of protocols is done by using ATC. This shifting of protocols is done automatically at the source node by comparison with the throughput value. But reconfiguration of routing protocols at intermediate nodes is done using information in the RREQ from the source. The reconfiguration at router node cannot be decided by itself but by information from source only.

5.2 Procedure of ATC algorithm

Though all the nodes in MANET contains reconfigurable router as in figure 6 in hardware, the following procedure [15] conforms to the condition that the referred node here is a source. Here the reconfiguration is done first in the source as DSDV protocol (default) .Once the target FPGA is reconfigured for any protocol, target section becomes that router. Then the routing section will start broadcasting Route Request through node's wireless interface. As it is the source node it instructs the other nodes to reconfigure to the same protocol by inserting a command in the reserved bits field of RREQ. After obtaining the route using the default protocol, ATC allows the sender to start sending the data packet for 10 sec, calculates the throughput, determines the threshold value and compare this value with the subsequent throughputs. The comparison will decide either to continue the present route or use next protocol in the suite to find the new route. The full procedure and conditional statements of this algorithm are presented in the conference paper [15].

5.3 Implementation of protocols and ATC

The route creation, route maintenance and route deletion in case of link break are studied for above four protocols. As we have already pointed out, router or routing section contains routing capability at a time with any one of the four routing protocols. When the routing section works with DSDV protocol we call it as DSDV router and likewise for others. To work as any of the four routers, the target FPGA should be provided with an architecture containing routing processor with input output buffer memories and cache, FIFO memories etc. The architecture of individual protocol routers differs as per the rules and conditions of that protocol. Therefore individually separate protocol architectures are to be discussed .For implementation procedure of any protocol; the finite state machine and the state modeling are used to create VHDL coding. Then the codes for DSDV, DSR, AODV, and TORA protocols are simulated and synthesized using Xilinx project navigator [16, 17, 18, and 19]. For this purpose a suitable FPGA is selected to accommodate any protocol at any point of time. In this paper, only architectures of all the protocols and ATC algorithm are shown in simplified form. The results of synthesis will follow the architectures.

5. 3.1 DSDV architecture

The basic block diagram for this DSDV protocol architecture [16] is shown in the figure7. Using these functions and their Finite State Machine (FSM) model, VHDL codes are written. The architecture includes the Route Information Memory (RIM), DSDV processor, input and output buffers for temporary storage and the control unit that helps to coordinate the various processes. The routing processor of any protocol architecture performs

1. Store and update the routing table by flooding.
2. Forwards the data packet to destination using router node.
3. Reconfigure the routing architecture using control signal from ATC.

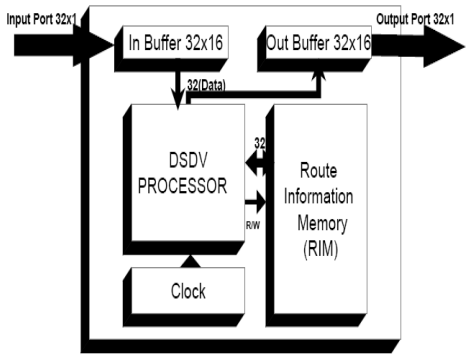


Figure 7: Proposed DSDV Architecture

5. 3.2 DSR architecture

Dynamic source routing (DSR) protocol utilizes source-based routing rather than table-based, and source-initiated rather than hop-by-hop. The functional block diagram of DSR protocol hardware architecture [17] is shown in figure 7. The functional block diagram consists of all the FSM states along with the FIFO and cache memories. DSR protocol consists of two main functions such as route discovery and route maintenance. If there is a data packet to transfer, the route check state checks the availability of the route in the cache memory. If the route is available, data packet is transmitted in the send data state, else route discovery process is initiated by broadcasting Route Request packets (source id, destination id, request id) to the router nodes until it reaches the destination node. The Route Request packet is stored in a table to avoid repeated route discovery. If the route discovery time exceeds, then the node goes into the idle state. The Route Reply state writes a Route Reply in a piggy back manner. Using this FSM model, VHDL codes are written.

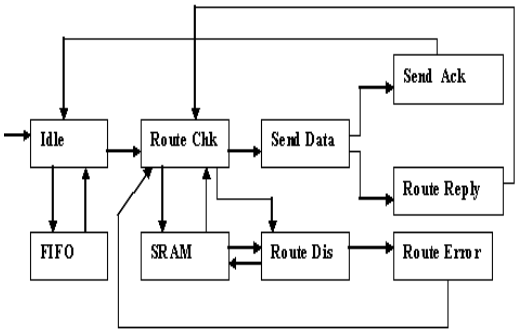
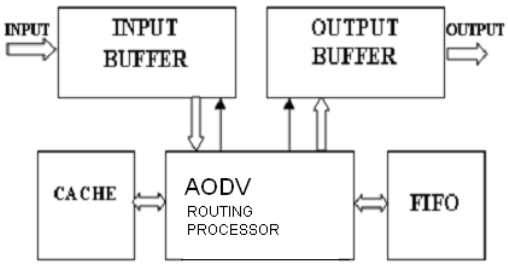


Figure 8: Proposed DSR Architecture

5. 3. 3 AODV architecture

The basic block diagram for this AODV architecture [18] is given in figure 9. It includes the cache memory for route table, FIFO memory for data, and AODV router processor, input and output buffers for temporary storage. Using these functions and their FSM model, VHDL codes are written.



. Figure 9: Proposed AODV Architecture

5. 3.4 TORA architecture

Temporally ordered routing algorithm (TORA) is a highly adaptive, distributed, multi hop and multi path reactive protocol. It is loop free and provides fast routing in highly mobile environment. The basic building block [19] includes the various memory structures, main router processor, buffers for temporary storage, neighbor status and link status memories and the control signals that help to coordinate the various processes. TORA architecture also is more or less similar like AODV router. The basic block diagram of TORA Architecture is shown in figure 10.

The three basic functions performed by the router include 1.Creating routes, 2. Maintaining routes and 3.Erasing routes. Using these states and FSM modeling, VHDL codes are written.

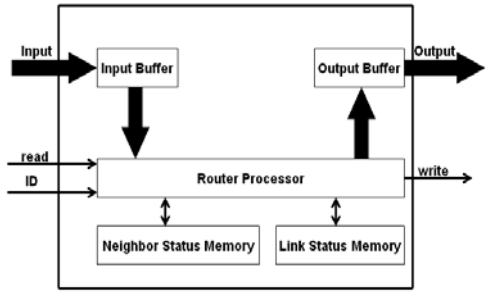


Figure 10: Proposed TORA Architecture

5. 4 Synthesis and simulation results of DSDV, DSR, AODV and TORA

All the Four protocols are modeled by VHDL and its functionalities are verified by the simulation using Modelsim.

Table 1: Device utilization Summary

Device selected: V200EFG256-7

Name of Protocol	Device parameter				
	Slices used	Flip flops slices used	Lut's used	Iob's used	Gclk's used
DSDV	153	111	186	169	4
DSR	191	122	362	33	1
AODV	832	1108	1400	69	1
TORA	1559	379	2456	27	4

Table 2: Timing Summary

Name of Protocol	Minimum input arrival time before clock in ns	Maximum output required time after clock in ns	maximum frequency in MHz
DSDV	3.203	6.436	138.646
DSR	16.800	6.14	63.613
AODV	9.947	6.14	85.594
TORA	15.58	6.34	103.1

Then VHDL models of four protocols are synthesized using Xilinx tool and the obtained device utilization and timing summaries are shown in table 1&2 respectively. Implementations used the same FPGA device V200EFG256-7 so that at any point of time any protocol can be downloaded for configuration.

5. 5 Synthesis and Simulation results for ATC

The ATC algorithm is modeled by VHDL and its functionality is verified by the simulation using Modelsim. Then VHDL model of ATC is synthesized using Xilinx tool and the device utilization and timing summary are obtained.

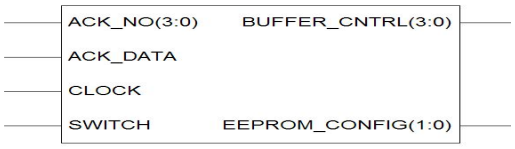


Figure 11: Entity of ATC processor

Figure 11 shows the entity of ATC processor which consists of 4 input pins as acknowledgement trigger, acknowledgement data number from the destination, clock for synchronization and switch to make the processor on or off.

The simulated waveform results obtained for ATC algorithm using Modelsim are shown in figure 12. The simulation graph shows that whenever the throughput plunges to a value lower than the threshold value, new protocol in the suite is downloaded to the target FPGA. Using this routing protocol, throughput is monitored and compared with the threshold continuously.

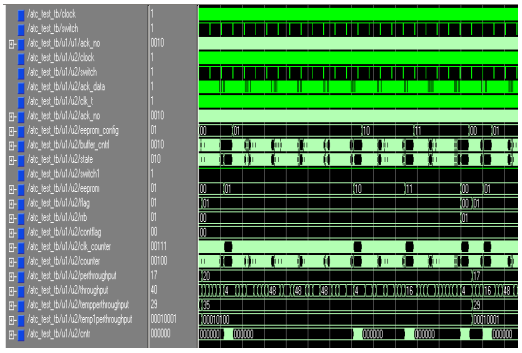


Figure 12: ATC simulated waveform

The comparison may lead to continuation of the same protocol or switching to next protocol. The simulation graph shows the occurrence of change of protocols from DSDV to DSR when throughput does not satisfy the condition of 20 packets as threshold. Likewise other protocols are also invoked. In the simulation, the change of protocol occurs at throughput values of 4, 4, 16 and 4 packets. After a complete cycle of four protocols, fresh threshold value is fixed at 17 with a reduction of 3 from 20 packets. Now the next cycle starts from DSDV. Like wise the throughput monitoring for every 10 sec will lead to either sustaining of the present protocol or shifting to the next protocol so that throughput is consistent.

6 Conclusions

The nature of mobile ad hoc networks makes it very challenging to come up with an efficient routing protocol for all network conditions. A MANET node design is discussed with three routing techniques for this purpose. The first routing technique is simulated to have effect of change over of routing protocols from DSDV to DSR using Glomosim. This study proved that the throughput consistency is achieved due to overall strategy of change of protocols. Next a study was done on a new routing strategy for AODV, called self healing routing technique using Glomosim. The paths generated by any of routing protocols may deviate far from the optimal because of the lack of knowledge about the global topology and the mobility of nodes. While using this technique, all the neighboring nodes monitor the route and try to optimize it if and when a better local sub-path is available. Thus this technique enhances the packet delivery rate with respect to node speed and no of nodes.

The later part of the paper documents the design and FPGA implementation of certain routing processing functions in MANET. It also demonstrates how the reconfigurability offered by FPGAs can be exploited to implement routing protocols. A novel algorithm ATC for dynamic selection of routing protocol has been proposed and implemented. This aided the integration of the individual routing protocol implementations into a new adaptable routing strategy using reconfigurable FPGA. This work shows that the functions of a node traditionally implemented in software have the potential to be implemented in hardware for a significant performance boost.

To summarize:

1. The individual routing protocols DSDV, DSR, AODV and TORA – designed and implemented in a reconfigurable target FPGA.
2. In order to provide reconfigurability for routing section and the selection process, it is proposed and implemented a novel algorithm ATC to switch among protocols.
3. Throughput variations occurring at the destination is monitored continuously and compared with the threshold value. The result of comparison leads either to continue or reject the current routing protocol to choose next in turn.
4. The ATC algorithm is also hardware implemented in another FPGA.
5. Finally the router section is simulated using Modelsim to study the effect of throughput variation and evaluation.

This new adaptive routing strategy to MANET node using reconfigurable FPGA is one of the first designed nodes with dynamic routing protocol selection capability. To the best of our knowledge no work has been taken up in hardware to design a MANET node which can use an adaptable routing strategy to meet the network conditions. The work can be extended to new protocols and get evaluated and compared with the existing protocols.

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