FPGA Implementation of Tunable FFT For SDR Receiver

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Abstract
 The purpose of this paper is to compare competing techniques for wideband channelisation, and to assess the flexibility of each of these methods in the context of a software defined radio (SDR) receiver. Distinction is drawn between architectures where all channels are equally spaced and of equal bandwidth, and those architectures which afford greater flexibility. The architecture requires that an input signal be separated into a number of different frequency channels. If these channels are of equal width and equally spaced, then techniques such as the Fast Fourier Transform (FFT) or the pipelined frequency transform (PFT) can be employed. The most common solution is to employ a number of digital down converters (DDC) each responsible for an individual channel. The tunable pipelined frequency transform (TPFT) provides similar functionality to a stack of DDCs. It gives the user freedom to specify channels by centre frequency and bandwidth define filter characteristics and reconfigure to another frequency plan as required. Furthermore, spectral shaping masks can also be directly applied onto the outputs within the architecture itself. This paper describes the TPFT architecture and will highlight the advantages of this technique over competing solutions.   The proposed architecture is coded using VHDL and the simulation and synthesis reports are discussed.

Keywords:
FPGA, FFT, Reconfigurable etc

1. Introduction

In many existing SDR receivers, one of the most expensive components is the analogue circuitry required to carry out the initial down conversion prior to digitization. With present available ADC technology which provides high-resolution digitization at sample rates of up to several hundred MHz. So it is required to implement latter downconversion stages digitally. This is most especially the case when a large number of signals are required to be monitored or downconverted at the same time.

The most common technique involves the use of a Digital Downconverter (DDC). The DDC process is often carried out using custom ASIC chips, of which there are many different varieties available, although DDC FPGA cores are also available from many vendors. Typical DDC functionality is illustrated in Figure 1. First function is a frequency shift of –f to centre the required channel at DC, including conversion from real to complex. Filtering is the second function to remove all the unwanted out-of-band signal components that would otherwise alias into the pass band on decimation and decimation by a user-specified factor D and it is achieved by using a decimating CIC. The CIC filter shape is corrected by further decimate-by-4 low pass filter and applies a user-defined filter to the output. Usually, in a digital receiver where the DDC output is being fed into a demodulator, the required output rate is close to an integer multiple, R, of the symbol rate where R is typically in the order of 2 to 4.
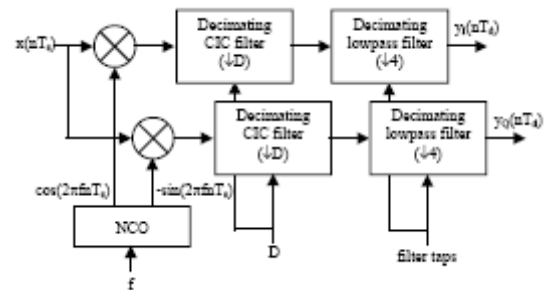

Figure 1: DDC chip architecture

Most DDCs permit the user to control the decimation rate and the filter characteristics, although the precise level of flexibility depends upon the implementation. Typically, a fully programmable DDC ASIC chip supports around 4 independent channels, extracted from digitized inputs, although some reduced functionality DDC chips are now available that support larger numbers of channels (e.g. only supporting a single communication standard). DDC cores for FPGA often have more flexibility, though they can require a lot of silicon.

There are many cases where several hundred relatively narrowband (100s of kHz) channels are required to be down converted from a single wideband (100s of MHz) digitized data stream. In this case, it is normally attractive to replace a large number of ASIC DDC chips with a single integrated channeliser. If the required signal parameters are known at design time, it is possible to eliminate some of the flexibility of the DDC approach to provide far more silicon-efficient down converter structures that are tailored to meet specific requirements. Generally, these structures are implemented in FPGA since they are not required for volume applications; however, there is no limitation to their implementation on ASIC. A further advantage of using FPGA technology is that it provides a degree of future proofing, in that if a different channel structure is required at a later date, a different FPGA image may be provided that meets this requirement without the need for a complete redesign of the board.

RF Engines have various patented and proprietary channeliser architectures that can be used to meet a wide range of requirements. These may be classified in to three types. First one is Wideband DDC cores providing down conversion of a few relatively wideband sources from a wideband input source. Second is Flexible multichannel down converter cores providing channelisation of a large number (a few hundred) of relatively narrowband sources from a wideband inputs. These channeliser cores can be used to efficiently extract signals from any dynamically selectable frequency with a very wide variety of channel sample rates and filter characteristics. Third is fixed multichannel down converter cores that channelise a very large number (more than a thousand) of channels from fixed channel locations, where the channels have a fixed spacing and all share the same filter shape and output sample rate. Each of these variants has advantages for different applications.

Figure 2 summarizes the applications for the different down converter techniques. In this figure, wideband DDC cores are seen to provide significant flexibility for a limited number of channels; the fixed down converter cores are at the other end of the scale, providing limited flexibility but a large channel capacity. The flexible down converter cores occupy the parameter space between the above two where a core can be provided that meets the required flexibility versus efficiency tradeoff for a particular application. In general, silicon usage increases both with the number of channels and the required flexibility.

The remainder of this paper will concentrate firstly on the implementation of fixed multi-channel down converters, including mixed radix FFT-based architectures and secondly on flexible multichannel down converter architectures.
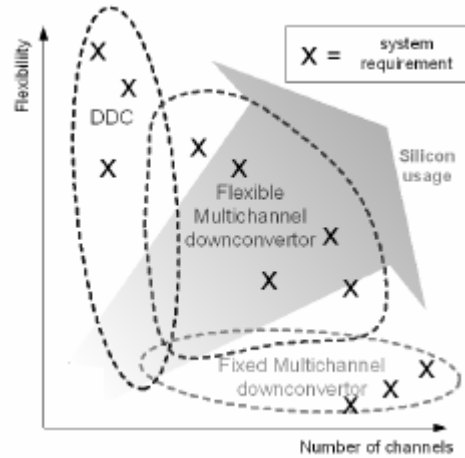

Figure 2: Suitability of Different Channeliser Architectures

FPGA Implementation of Tunable PFT Fixed Multi Channel Down Converters

The WOLA or Polyphase FFT

The K-point FFT is considered as a critically decimating filter bank, providing K equally spaced channels. All filtered by a K-point moving average filter response and decimated by a factor $D = K$. To modify the filter response and change the decimation factor an additional filtering stage is provided in the Weight Overlap Add (WOLA) FFT. The Polyphase FFT technique is has less flexibility in the selection of the decimation factor. The following are the design parameters for the WOLA FFT:

1) The input sample rate (f_s)
2) The length (number of points) of the FFT, K, which provides the channel spacing from the equation, $f_\Delta = f_s / K$;
3) The decimation factor through the WOLA, D, which provides the output sample rate per channel via the relation, $f_{demod} = f_s / D$.
4) The filter impulse response, $\{h[n], 0 = n < L-1\}$. The channel spacing, f_Δ, is fixed by the communication standard and the required sample rate f_{demod} is specified for the demodulator; f_{demod} is normally very close to an integer times the symbol rate. To meet out the above requirements the following is the condition to be satisfied.

$$K / D = f_{demod} / f_\Delta \text{--------- (1)}$$

The implementation of WOLA DFT structure is as shown in Figure 3, where all lines represent complex data.

The input sample is divided into frames of D samples and they are passed into a delay line. After they are weighted by the filter impulse response, then it is divided into blocks of K samples and overlapped to pass through the FFT. Finally the phase of the outputs is corrected.
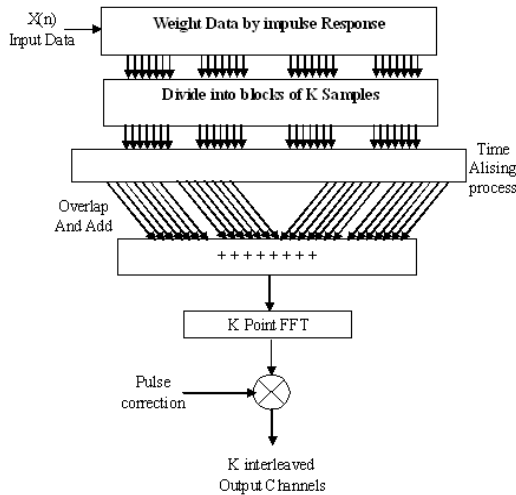

Figure 3 WOLA FFT Structure.

Flexible Multi Channel Downconverters

The Tunable PFT

The principles behind the Pipelined Frequency Transform (PFT) is a simple Radix-2 PFT achieves its channelisation by a process of frequency band splitting, as shown in Figure 4 below. In this design, the silicon efficiency would be very low due to the sample rate reduction at each stage. Full usage of available silicon is made by interleaving the samples at each stage and the proposed design is shown in figure 5. This structure allows simplification of the complex up /down conversion required at each stage. This architecture can be realized as a multiplier-less architecture. The key feature of this proposed structure is the simultaneous proceeding of availability of outputs at each stage of resolution, providing the basis for a flexible multi-resolution filter bank.
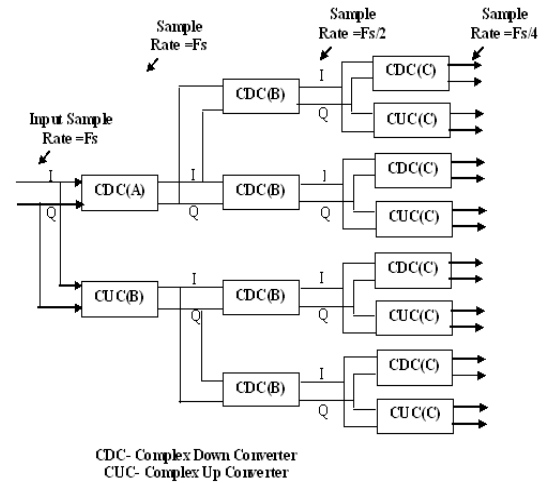

Figure 4: PFT – Simple Tree System

The Tunable PFT was designed and the flexible architecture is shown in figure 5 where the selected bins from each stage are interleaved into a single complex stream. This is possible since, at this point; there is an integer relationship between the sample rates for each stage. Fine tuning of each filter centre frequency may be achieved by passing the interleaved samples through a single polyphase structure consisting of a complex up or down conversion (CUC / CDC) and a final channel filter. The latter allows each channel to have the required filter response (e.g. root-raised cosine). The only remaining requirement, to allow efficient demodulation, is a multirate section which allows the final sample rate to be more accurately matched to a multiple of the symbol rate. This is a common requirement for both fixed and flexible down converters.
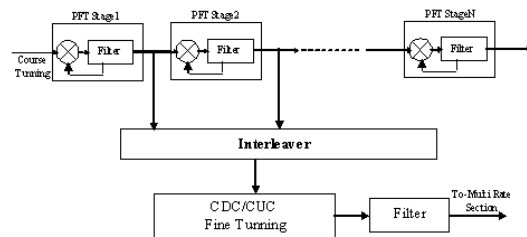

Figure 5 Schematic of Tunable PFT Architecture

Hybrid Tunable Structures

It is frequently the case that the widest channel required is still a small fraction of the overall bandwidth being channelised. The PFT is likely to be less efficient and have higher latency than the polyphase FFT for single resolution filter bank. It can be useful to realize the first

part of the flexible channeliser in the latter form. This can then be followed by a tunable PFT to achieve the flexibility required. To make more efficient where a wide difference exists between successive stages of filter resolution is to replace some of the final stages with more conventional decimating filters.

RF Engines suggested that hybrid architectures support a maximum aggregate output bandwidth which may be divided between a large number of narrow band channels, relatively fewer wideband channels, or some combination thereof. The user may reconfigure channels at run-time providing the overall bandwidth limit is not exceeded. These techniques exploit resource sharing principles to ensure that silicon resources are minimized for any particular configuration, and show great promise for future flexible channelisation designs, particularly where there is a wide variation in channel sizes.

Multi-Rate Structures

The above architectures described are able to flexibly filter and down convert narrow band channels from a wideband input spectrum. The sample rate of the resulting channelised signals is often determined by fixed decimation factors through the design. The above sample rates are not suitable for the subsequent processing, and hence an efficient additional structure is required to resample each signal to produce the desired sample rate. RF Engines have suggested that highly efficient architecture for this purpose that can resample many channels in an interleaved fashion. Use of fractional resembling techniques allows the channel sample rates to be selected with a resolution which is better than 0.01 Hz.

Simulation Results and Discussion

The figure 6 shows the simulation result of proposed system and the table 1 shows the device utilization summary of proposed design. The figure 7 shows the RTL View of the proposed Design.
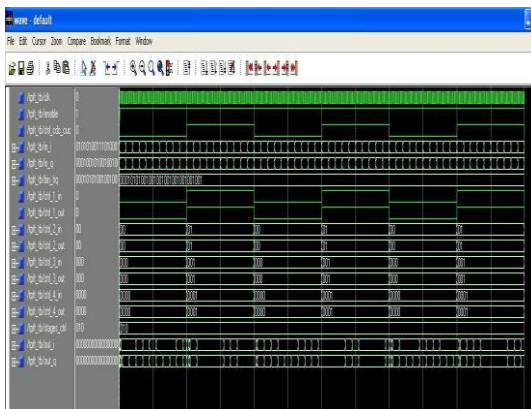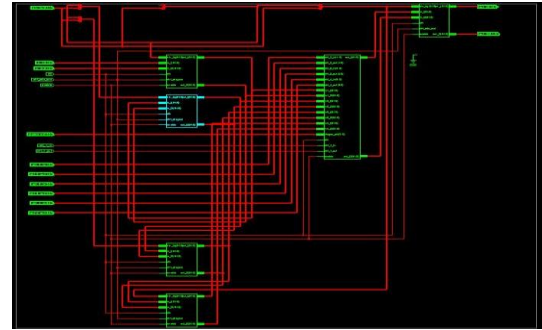

Figure 6 Simulation result

Figure 7 RTL view of the proposed design

Table 1 Device utilization summary:

Selected Device: 2v500fg256-5

Sl. No	Description	used	Available	% Usage
1	Number of Slice Registers	2240	3072	73%
2	Number of Slice LUTs	5811	6144	95%
3	Maximum Frequency			614.8MHz

Conclusion and Future Work

In this paper discussed the various range of approaches for performing the down conversion function in a digital radio receiver, including the classic DDC, FFT based architectures, and novel approaches such as the TPFT. In general there is a trade-off between the level of flexibility offered by the architecture and the silicon resources required for implementation. The DDC offers excellent flexibility with the user able to select the bandwidth and centre frequency of a channel with high level of resolution. However, this approach suffers from the disadvantage of requiring a large amount of silicon which may preclude its use in systems with more than a few channels. FFT based approaches, such as the WOLA and Polyphase FFT, are at the opposite corner of the flexibility/resource space. These approaches are highly efficient, with example implementations supporting several thousand channels on one FPGA. However, the inherent use of the FFT requires that all channels must have equal bandwidths, and must be regularly spaced across the input bandwidth. The TPFT

and hybrid variants offer an excellent compromise between these two extremes. A 64-channel down converter has been shown which offers flexibility which is comparable to a standard DDC architecture and fits comfortably within a Xilinx Virtex II Pro 30. Architectures such as these are a cost effective solution for down-conversion in multi-channel digital receivers, and represent a critical building block for flexible software defined radios of the future.

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