A 0.4V - to - 1.4V Inverter Based 5-bit Flash ADC in 0.18μm CMOS Technology for UWB Applications

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Abstract

In this paper, 5-bit flash analog-to-digital converter (ADC) for low voltage and high speed ultra wideband (UWB) applications is presented. To achieve high speed threshold inverter quantization (TIQ) technique is utilized in comparators design. The thermometer to binary decoder can be designed using fat tree decoder, wallace tree decoder, ROM decoder, multiplexer-based decoder etc. We implemented multiplexer-based decoder which has advantages of having regular structure and shorter critical path over existing decoder circuits. The 5-bit flash ADC has been designed and simulated in 0.18μm CMOS technology using tanner design tools and achieved INL, DNL values less than 1LSB and effective number of bits of 4.29-bits.

KeyWords:

Analog-to-digital converter (ADC), flash, high speed, multiplexer-based decoder, threshold inverter quantization.

1. INTRODUCTION

Trends in many communication systems, such as ultra-wideband (UWB), cognitive, and software-defined radio, require ever wider signal bandwidths, increased flexibility, and system integration with lower power consumption and smaller area to meet cost targets [1]. Typical requirements of these system architectures demand medium-resolution (5-bit) and high-speed (GHz) analog-to-digital converters (ADCs). If the ADC is designed with sufficient input bandwidth, it is able to subsample the wideband RF signal and achieve a solution that even further dramatically reduces implementation cost.

Conventionally, a flash-type converter is often chosen when the sample rate is high, since it can perform the conversion in a single clock cycle. However, this comes at the expense of an exponential dependence of area and power on the resolution, as well as offset variations. This paper presents the design of a 5-bit flash ADC in 0.18μm CMOS technology.

The rest of the paper is divided into four main parts. In section 2, the architecture of high-speed Flash ADC is reviewed. Section 3 describes the design of flash ADC and its various components. The simulation results obtained are presented in section 4 and the conclusions are drawn in section 5.

2. A/D CONVERTER ARCHITECTURE

The architecture of the flash ADC is shown in Fig. 1. It mainly consists of two blocks. First block is composed of a column of comparators with different reference voltages usually provided by a resistor ladder. The number of comparators is 2^N-1, where N is the number of bits at the output of flash ADC. It is also termed as resolution of ADC. Under perfect conditions, all comparator outputs below the input level are ones, and all comparator outputs above the input level are zero. The second block is the thermometer-to-binary decoder. This decoder converts the output of comparator block in thermometer code format to binary code format [2]. The point where the code changes from one to zero is the point where the input signal becomes smaller than the respective comparator reference voltage levels.

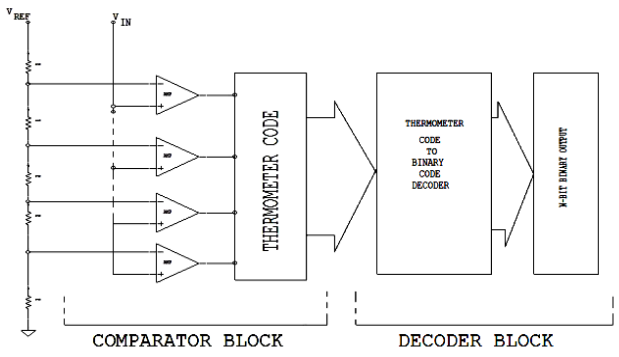

Fig. 1 Architecture of high-speed Flash ADC

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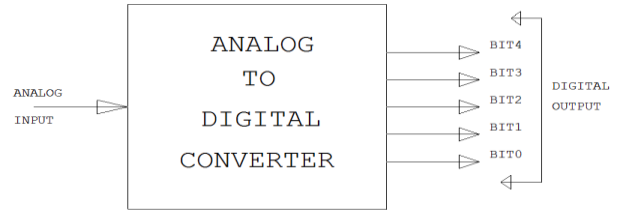
The thermometer coded output of the comparators is converted to binary code by a thermometer-to-binary decoder which corresponds to the digital output equivalent to the applied analog input.

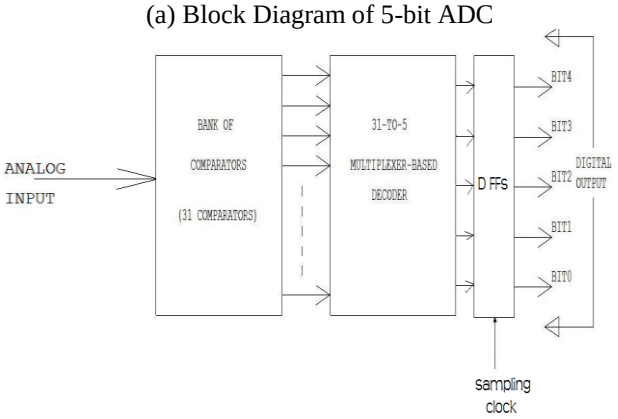
3. DESIGN OF FLASH ADC

This section describes the design of 5-bit flash ADC. It consists of three blocks: (1) Comparator bank, and (2) 31x5 multiplexer-based decoder and (3) D-Flip Flops.

Fig. 2 shows the schematic representation of a 5-bit flash ADC. It accepts an analog input such as voltage or current and gives out 5-bit binary number as the output. As explained earlier the flash ADC is the preferred architecture to choose when one is designing a high speed low resolution ADC. The ADC has been designed to meet the V_{LSB} which is the quantization step as 31.6 mV.



(a) Block Diagram of 5-bit ADC



(b) Detailed block diagram of 5-bit ADC

Fig. 2 Schematic representation of 5-bit flash ADC

3.1. TIQ comparator

The comparator structure is the most critical part in flash ADC architectures. The main problems of the conventional comparator structures used in ADC designs are: 1. Resistor or capacitor array requirement 2. DC bias requirement 3. Large transistor area for higher accuracy 4. Metastability errors 5. High power consumption 6. Charge injection errors. In this work Threshold Inverter Quantizer (TIQ) technique has been applied. The TIQ CMOS inverter design is based on systematic transistor sizing. It eliminates the resistor array implementation of conventional comparator array flash designs. Therefore no static power consumption is required for quantizing the analog input signal which is attractive for battery-powered applications. However it has disadvantages such as requirement of 2^N -1 number of different area-sized quantizer designs. The TIQ consists of two cascaded CMOS inverters as shown in Fig. 3.

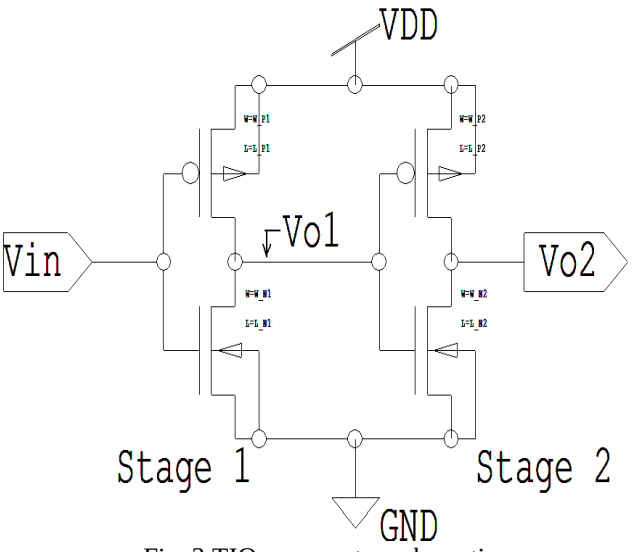


Fig. 3 TIQ comparator schematic

A CMOS inverter consists of one PMOS and one NMOS transistors, with the inverter switching threshold voltage depending upon the transistor sizes. If one fixes the length of both the PMOS and NMOS transistors at a constant size, one can obtain different inverter switching threshold voltages (Vm) by simply varying the transistors' widths [3]. The sizes of NMOS and PMOS transistors in a comparator are same and are different for different comparators. The length of NMOS, PMOS transistors are fixed at 180nm, where as width of NMOS varies between 7200nm to 180nm and width of PMOS varies between 180nm to 13950nm to achieve switching voltages for TIQ comparators from 425mV to 1.37V.

3.2. Decoder

Thermometer-to-binary decoder can be implemented by various approaches, e.g., a ROM, Wallace-tree (or ones-counter), multiplexer-based decoder, fat-tree decoder and logic-based decoder [4]. Among various types of decoders available multiplexer-based decoder requires less hardware, has more regular structure and shorter critical path. The combination of having medium power consumption, low transistor count, more regular structure and shorter critical

path makes the 5-bit multiplexer-based decoder is suitable for efficient flash ADC design [5].

The design of multiplexer-based thermometer-to-binary decoder [4] is shown in Fig. 4. This decoder is based on 2-to-1 multiplexers connected as a tree. Each level of the tree divides the input thermometer scale in two and calculates one of the bits in the binary output. In comparison with the wallace tree decoder the length of the critical path is approximately reduced to one third. The amount of hardware is also reduced, which will translate to a power saving, compared with the wallace tree decoder.

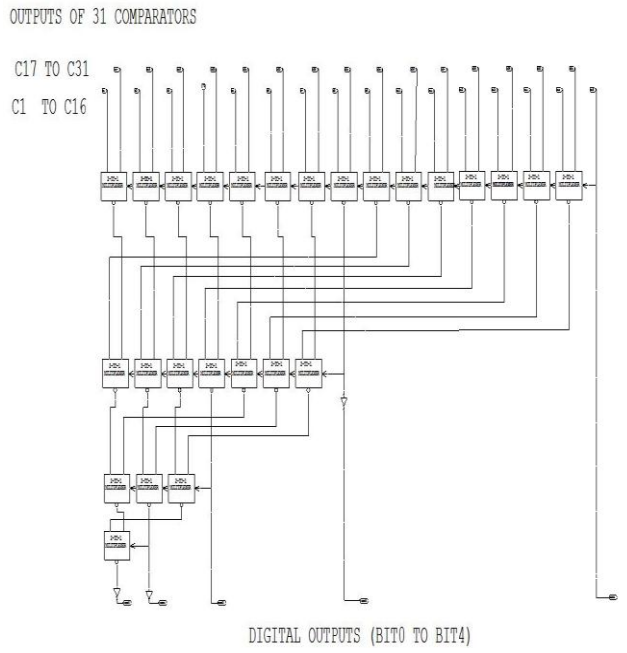


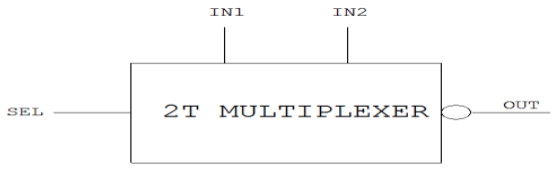
Fig. 4 Multiplexer-based thermometer-to-binary decoder

For an N-bit flash ADC the most significant bit (MSB) of the binary output is high if more than half of the outputs in the thermometer scale are logic one. Hence MSB is same as the thermometer output at level 2^{N-1}. To find the value at the second most significant bit (MSB-1) the original thermometer scale is divided into two partial thermometer scales, separated by the output level at 2^{N-1}. The partial thermometer scale to decode is chosen by a set of 2-to-1 multiplexers where the previous decoded binary output is connected to the control input of the multiplexers. MSB-1 is then found from the chosen partial thermometer scale in the same way as MSB was found from the full thermometer scale. The chosen scale is there by the scale that contains the information about MSB-1, i.e. the lower partial thermometer scale if the output at level 2^{N-1} is logic 0 otherwise the upper partial thermometer scale is used.

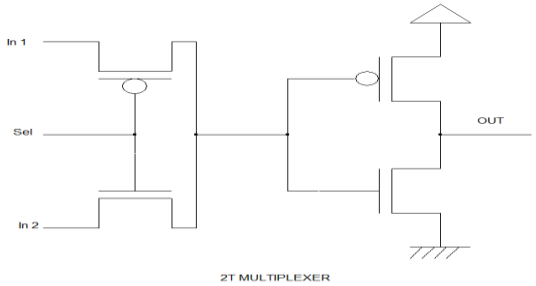
This is continued recursively until only one 2-to-1 multiplexer remains. Its output is the least significant bit of the binary output. The 5-bit multiplexer-based decoder is realized using 26 instances of 2-to-1 multiplexers, 28 instances of inverters, is realized with total of 108 transistors with 2.5408e-005 watts of average power consumption [5]. Due to its regular structure, it can easily be expanded to operate in a system of higher resolution than 5-bits. 2-to-1 multiplexer can be implemented in 2TMux (pass-transistors), CMOS transmission gate, CPL, CVSL, DCVSPG, DPL, EEPL, LEAP, PPL, SRPL and Static CMOS logic styles . Among them 2T multiplexer is suitable for multiplexer-based decoder implementation which is characterized by high speed with minimum power compared with all other realizations [6]. The implementation of 2T multiplexer is shown in Fig. 5.

3.3. D Flip-Flop Implementation

The inverter based D Flip-Flop implementation is shown in Fig. 6. It has *DATA, CLK* as inputs and *Qout* and *nQout* as outputs. The cross coupled connection of inverters forms latch. When *CLK* is high, provided the inverters are sized correctly, the *DATA* input is connected to *Qout* and complement logic is available at *nQout*. When *CLK* goes low the value of *DATA* is remembered and latched.



(a) Leaf cell of Multiplexer-based thermometer-to-binary decoder



(b) Realization of 2T Multiplexer

Fig. 5 Schematic of 2T Multiplexer

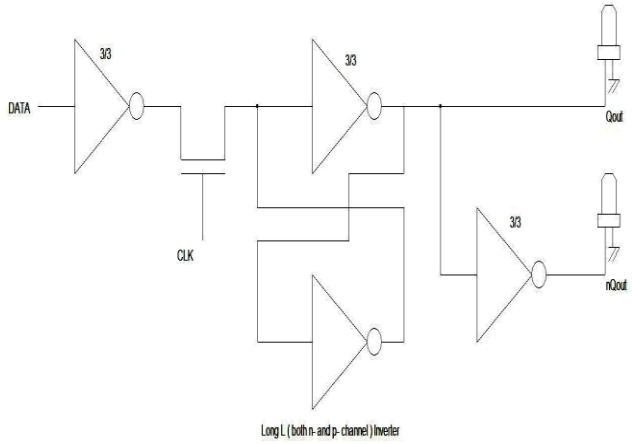


Fig. 6 Inverter based D Flip-Flop implementation

4. SIMULATION AND CHARACTERIZATION RESULTS OF 5-BIT FLASH ADC

By integrating the previously designed components, 5-bit flash ADC is designed and simulated using Tanner simulation tools in 180nm CMOS technology.

4.1. Functional Simulation

An input sinusoidal wave of 1MHz with 1.5 V_{pp} is provided to the flash ADC to test its functionality for the entire dynamic range. Fig. 7 shows the transient response simulation result of 5-bit flash ADC and can be seen that bit4 represents the MSB and bit0 represents the LSB of the digital output of the 5-bit flash ADC. Fig. 8 shows the transient response simulation result of a 5-bit flash ADC for ramp signal. The digital codes were obtained correctly, going from 0 to 31 at the output, indicating the correct functionality of ADC.

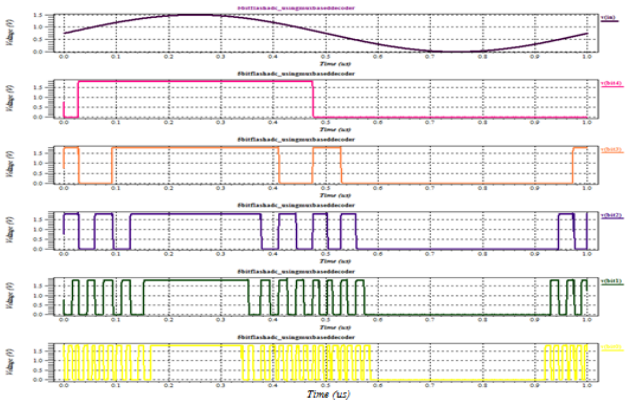


Fig. 7 Transient response of the 5-bit flash ADC for sinusoidal signal of 1MHZ

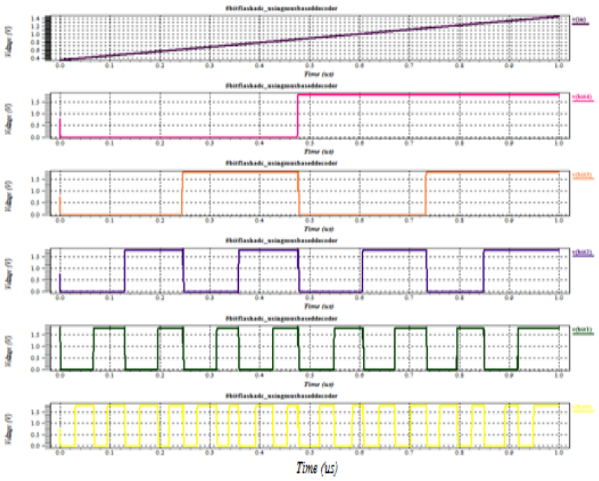


Fig. 8 Transient response of the 5-bit flash ADC for ramp signal

4.2. Power Simulation

Fig. 9 shows the instantaneous power plot of the designed 5-bit flash ADC. The flash ADC is fed with a ramp input signal which covers the entire full-scale range. From the plot, it is observed that peak power of 3.5766mW and average power of 1.0631mW is consumed.

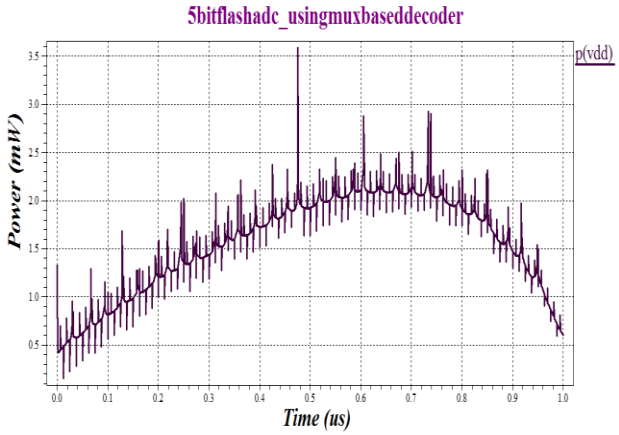


Fig. 9 Instantaneous power plot of the 5-bit flash ADC

4.3. Characterization

The designed 5-bit flash ADC is characterized for parameters like differential non-linearity (DNL), integral non-linearity (INL) (Static performances), signal-to-noise ratio (SNR), signal to noise and distortion ratio (SNDR) and effective number of bits (ENOB) (Dynamic performances) as shown in Table 1. These parameters have been measured at an input frequency of 1MHz which covers the entire full-scale range. For 5-bit flash ADC the

transient simulations are done using Tspice and the transient analysis values are processed

Table 1 The simulated performance of designed 5-bit flash ADC

Parameter	Specification	Parameter	Specification
Architecture	Flash	Max Speed	900MHz
Resolution	5-bit	SNDR	24.15dB
Power Supply	1.8V	SNR	24.11dB
CMOS technology	0.18µm	THD	3.01dB
Analog Input range	0.4V-1.4V	SFDR	4.77dB
Average Power	1.0631mW	ENOB	4.29
V_{LSB}	31.6mV	DNL	+0.88/-0.53LSB
Transistor count	371 MOS	INL	+0.23/-1LSB

to plot and calculate code coverage by ADC, differential non-linearity (DNL), integral non-linearity (INL) [7], signal-to-noise ratio (SNR), signal to noise and distortion ratio (SNDR), total harmonic distortion(THD), Spurious-free dynamic range (SFDR) and effective number of bits (ENOB)[8]. The code coverage plot is shown in Fig. 10 and the DNL and INL plots are shown in Fig. 11. The results in the frequency domain are displayed with an FFT plot in Fig. 12 and it shows the signal, along with higher harmonics. It is observed that, all the higher harmonics are overlapped at a single point. To distinguish all harmonics locations within the FFT plot, signal is excluded and a new plot is plotted to visualize higher harmonics and is shown in Fig. 13.

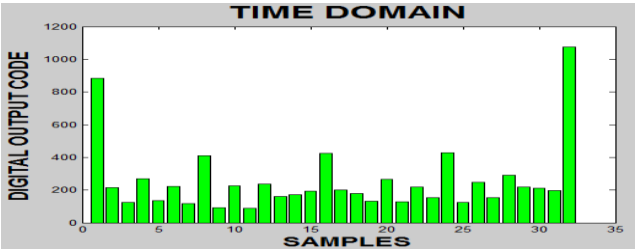


Fig. 10 5-bit flash ADC code coverage

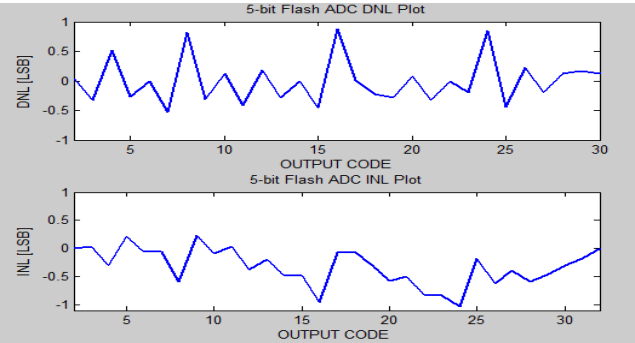


Fig. 11 DNL and INL plot of the designed 5-bit flash ADC

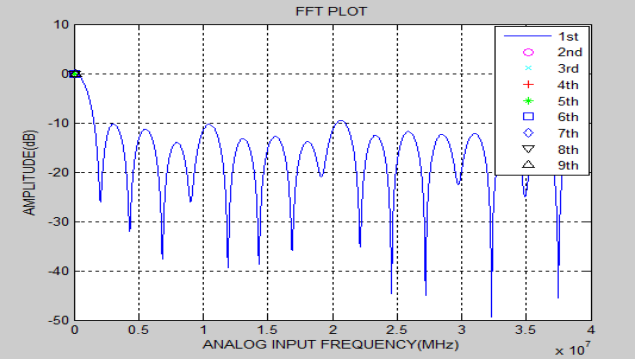


Fig. 12 The FFT plot of the flash ADC

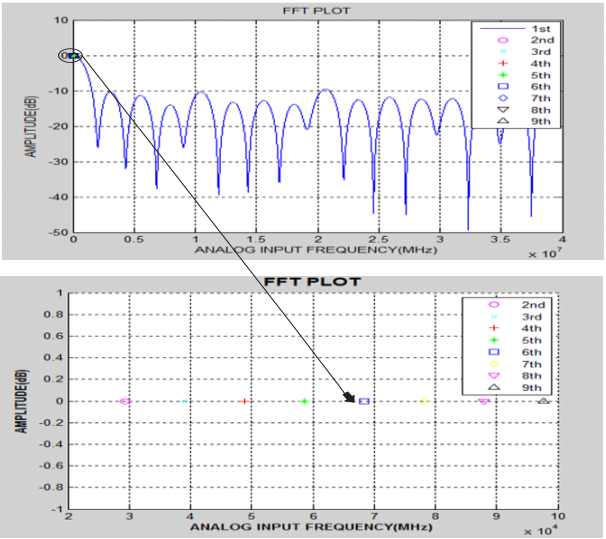


Fig. 13 FFT plot for clear view of higher harmonics

Fig. 14 Shows the DC analysis of the 31 TIQ comparators output.

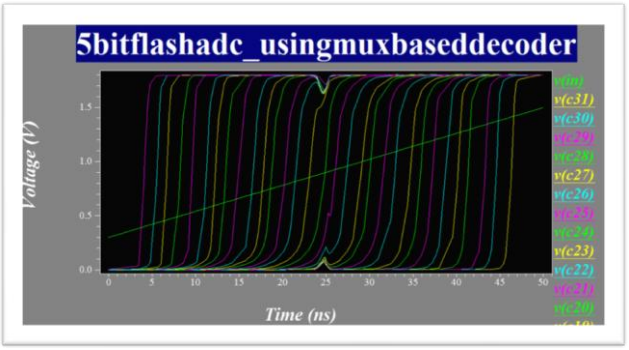


Fig. 14 DC analysis of the 31 TIQ comparators

5. CONCLUSION

A 5-bit high speed flash ADC for UWB applications has been designed in 0.18µm using CMOS technology. It is realized using 31 threshold inverter quantization based comparators and 31x5 multiplexer-based thermometer-to-binary decoder. These comparators are designed by varying the transistor dimensions to generate internal reference voltages. The pass transistor 2T multiplexer is used for realizing multiplexer-based thermometer-to-binary decoder. The combination of having medium power consumption, low transistor count, more regular structure and shorter critical path makes the multiplexer-based decoder as best choice for efficient flash ADC design when compared with all other thermometer-to-binary decoders. This thermometer-to-binary decoder also helps in reducing the area and power of flash ADC. The proposed flash ADC consumes an average power consumption of 1.0631mW, effective number of bits of 4.29-bits, DNL/INL values of 0.88/0.23 LSB when operating at 900MHz speed.

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