

FPGA Implementation and Mask Level CMOS Layout Design of Redundant Binary Signed Digit Comparator

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Abstract

In this paper a comparator is designed using Redundant Binary Signed Digit (RBSD) Number System. Radix-2 or signed binary digit number representations are of particular interest here. The redundant number system can be implemented by a digit set which has more digits in the set than the value of the radix and the set consists of digits $\{-1, 0, +1\}$. This allows a given number to have more than one representation. Each digit within these digit sets with the exception of zero is present in both positive and negative polarities. The RBSD comparator is designed by VHDL as well as in Verilog and its RTL view is generated by its FPGA implementation. Keeping view the low power VLSI design, the gate level circuit is implemented by CMOS with the help of Verilog and its mask level Layout is designed and simulated. The FPGA Implementation is done by Libero IDE v6 environment, which is a product of Actel Inc. The mask level layout design is done by the high end EDA tool i.e. Microwind2. For the performance evaluation it is compared with binary comparator.

Keywords:

Redundant Binary Signed Digit (RBSD), comparator, VHDL, FPGA implementation, CMOS etc.

1. Introduction

Data path components in modern high performance super scalar processors employ a significant amount of associative addressing logic based on the use of comparators that dissipate energy on a mismatch. These comparators are

used to detect a full match, but as mismatches are much more common than full matches in some components of the CPU, considerable energy-inefficiencies occur within the associative logic. The proposed designs are evaluated using SPICE simulations of actual VLSI layouts of the comparators in 0.12 micron

6-metal layer process and micro-architectural level statistics.

The high-speed comparator is a fundamental computation element for most digital systems, such as the state-of-the-art microprocessor and DSP design. Wang et al. [9] proposed the use of a tree structure with all-n-transistor (ANT) dynamic CMOS logic to build a fast comparator. Heavy pipelining is used for this design and it can achieve a very fast clock speed. For applications that need a single cycle comparison, this design may not be suitable.

Recently Huang and Wang [4] proposed a single-cycle comparator based on the priority encoding algorithm and dynamic circuit design technique. It was shown that it is 16% faster than Wang's design [9] when measured by the total execution delay.

The core element of the computation is the priority encoder, which is based on a dynamic NAND-gate design [10]. The long discharge path of the large-fan-in dynamic NAND gate becomes the bottleneck of the performance of the comparator. Here a RBSD comparison algorithm is developed with the help of Karnaugh Map, which does not need a priority encoder. The algorithm facilitates the use of NOR gate logic in the implementation and hence results in high performance when dynamic logic is used.

Today's world requires faster processor for the computation purposes for any digital system. With the constant growth of computer applications in every field of engineering such as signal processing, communications and Neural Networks, fast arithmetic logic units (ALU) are increasingly required. The ALU of any processor perform many functions such as Addition, Subtraction, Multiplication, Division and Logical Comparison etc.

Use of non-conventional number systems in designing comparator is gaining attention in recent years because of their facility to provide carry free addition thus enhancing the achievable processing speed. For making the processing faster a carry free addition technique is adopted by using Redundant Binary Number System [Aviz 1961]. The property of carry propagation chain elimination tends to make the processing faster. To design a RBSD arithmetic logic unit, it is necessary to design a RBSD comparator.

Advances in VLSI technology have made it possible for the designers to integrate many complex components in a single crystal Silicon, which was not possible earlier. Various high-speed Comparators have been proposed and realized. Keeping in view the various factors of VLSI Technology such as Speed, Area, Power and Cost, it's required to design a high-speed processor, which meets all the factors for the welfare of mankind.

The methodology involves an extensive study of Redundant Binary Signed Digit Number System & the design of Comparator circuit by using this number system with the help of HDL Based Language & its FPGA

Implementation followed by synthesis process. The extracted EDIF netlist is to be described by verilog and the mask level CMOS layout design is the main interest over here.

In this paper a digital system is designed by solving various possible combinations using Karnaugh Map and its description in VHDL. The above said objective is achieved with the help of simulation by using HDL based Simulator such as Active-HDL of Aldec Inc. and its FPGA implementation in Libero IDE v.6. (Integrated Design Environment) of Actel Inc. The mask level CMOS Layout Design is to be done by Microwind and the EDIF netlist (Electronic Design Interchange Format) in the form of RTL is to be captured by Schematic editor of DSCH 2 tool.

The rest of this paper is organized as follows: In Section 2, we discuss background information on a novel Redundant Binary Signed Digit (RBSD) number system and introduce some basic concepts of VHDL. In Section 3 the design of RBSD and binary comparator and its FPGA Implementation is discussed and it has been implemented in VHDL. The results are verified and presented in the form of waveforms. In Section 4 the mask level CMOS Layout Design of comparator circuits has been presented and its simulation on layout is also shown. The various characteristics graphs of nMOS and pMOS are presented. Comparison and conclusions part are given in the last Section.

2. Carry Free Addition using RBSD Number System

The redundant binary signed digit number (RBSD) representation makes it possible to perform addition with carry propagation chains limited to a single digit position and has been used to speed up the arithmetic operations. In order to cope with the problem of carry propagation the most appropriate approach is elimination of carry propagation. If the numbers can be represented in such a manner that addition does not require carry propagation then the addition is said to be carry-free or carry eliminated addition. The application of interval arithmetic in which carry propagates only one position and no additional carry is generated; makes possible carry free addition [Raj 1999]. The addition using interval arithmetic is described as:

Addition of operands = position sums = Interim sums + transfer carry.

Interval arithmetic provides interim sums and transfer carries in such a manner that the summation of interim sums and transfer carries fit into allowable digit set and do not propagate carries. The RBSD carry propagation free addition is performed in two steps.

Step1:

In order to eliminate the carry, at each position the transfer digit $t_i \in [-1, 0, 1]$ and interim sum digit $w_i \in [-1, 0, 1]$ is determined according to the table 2.1.

$$X_i + Y_i = 2t_i + w_i \quad (1)$$

Step 2:

The incoming transfer digit is added with the interim sum to obtain the final sum digit with no new transfer digit i.e. $S_i = w_i + t_i$.

Table 1

X_i	Y_i	$X_i + Y_i$	(X_{i-1}, Y_{i-1})	t_i	w_i
-1	-1	-2	X	-1	0
-1	0	-1	Both are non negative	0	-1
0	-1	-1	Otherwise	-1	1
-1	1	0			
1	-1	0	X	0	0
0	0	0	X	0	0
0	1	1	Both are non negative	1	-1
1	0	1	Otherwise	0	1
1	1	2	X	1	0

3. Design and FPGA Implementation of RBSD Comparator

3.1 Design of one digit RBSD comparator

To design the RBSD Comparator, the various conditions have been tabulated and minimized by Karnaugh Map. The two input vectors such as A and B are taken into consideration. The one digit RBSD comparator is designed by VHDL and is shown by Figure 1, in which both the input and outputs are treated as bit vector having width of two. The same one digit RBSD comparator is also designed by Data flow model, taking bit as the inputs and outputs to the comparator and is shown in Figure 2. The simulation results are verified with its corresponding logic diagram and are shown in Figure 3.

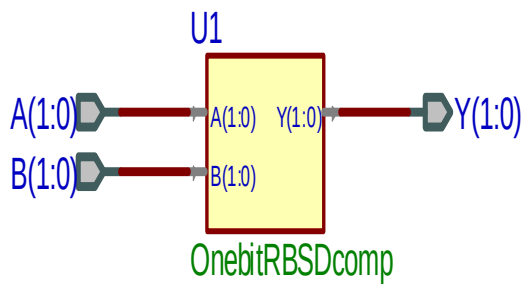


Figure 1 IC of One Digit RBSD Comparator (Bit Vector Form)

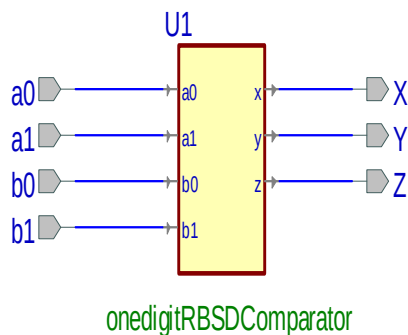


Figure 2 IC of One Digit RBSD Comparator (Bit Form)

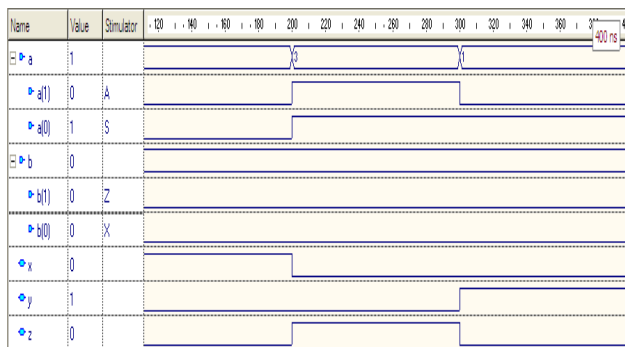


Figure 3 Simulation Results of One Digit RBSD Comparator

3.2 Design of two digit RBSD comparator

The design of two digit RBSD comparator undergoes in two steps. The first stage and second stage are the constituents of the two digit RBSD comparator.

3.2.1 Design of first stage of RBSD comparator

Here two single digit RBSD comparator blocks are cascaded to form the First stage of comparator. Though each Signed Digit is represented by two bits, that's why in case of two digit RBSD comparator, two blocks are to be cascaded together, which is seen in Figure 4. The IC form of two digit RBSD comparator is shown in Figure 5. Here

the inputs are in the form of bit vector having bit width of two i.e. $\{a1a0\}$ and $\{b1b0\}$ are the inputs to the first stage of comparator. In case of RBSD number system the inputs may be $\{-1, 0, 1\}$, which can be encoded in two bit format such as $-1 = \{-11\}$, $0 = \{00\}$, $1 = \{01\}$.

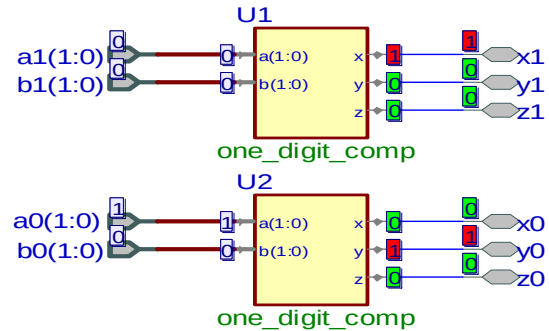


Figure 4 Cascaded Form of First Stage

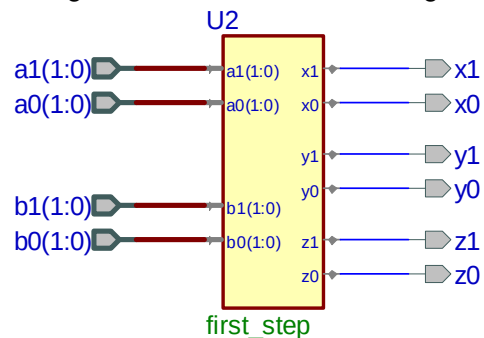


Figure 5 IC Form of First Stage

3.2.2 Design of second stage of RBSD comparator

The second stage of RBSD comparator is shown in Figure 6 and $x0, x1, y0, y1, z0, z1$ are the inputs to this block and e, g, l are the outputs of the block, which stands for *equal*, *greater* and *less* respectively.

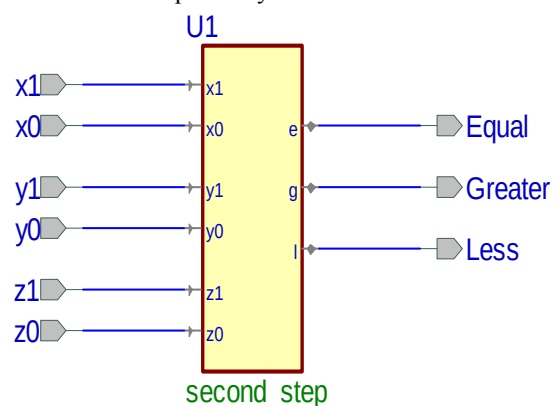


Figure 6 IC Form of Second Stage

3.3 Cascaded stage of two digit RBSD comparator

The first stage of RBSD comparator and the second stage of RBSD comparator are cascaded together to form the two digit RBSD comparator. $[a1, a0]$ and $[b1, b0]$ are the input vectors to this comparator. For checking the status of magnitude of inputs total three numbers of outputs are there, such as e , g and l are shown in Figure 7 and its corresponding simulated results are also shown in Figure 8.

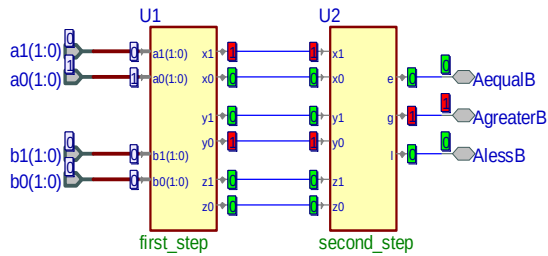


Figure 7 Cascaded Stage of Two Digit RBSD Comparator

Simulation Results:

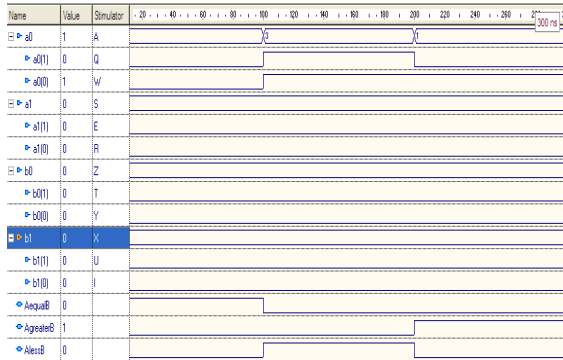


Figure 8 Results of Two Digit RBSD Comparator

The two bit binary comparator is designed by solving its possible combinations by Karnaugh Map using data flow model in VHDL results and are shown in Figure 10.

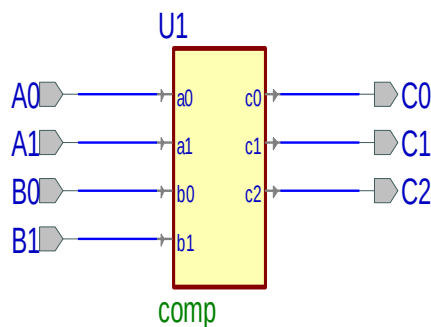


Figure 9 IC of Two Bit Binary Comparator

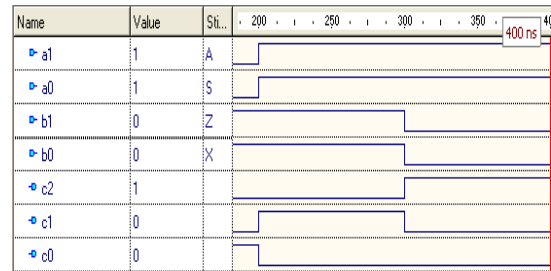


Figure 10 Simulation Results of Two Bit Binary Comparator

3.4 FPGA Implementation

Here the FPGA Implementation is done by Libero IDE v6 environment, which is a product of Actel Inc. The Family is PA, Die used APA150 and the Package is 208 PQFP. The VHDL codes are imported to the new created Actel Project. The Synthesis is done by Synplify of Synplicity Inc., which is integrated in this environment. Finally placement and Routing is done by Designer tool. Netlist Viewer is used to view nets, ports, and instances in the schematic view. The pre-optimized and optimized netlists of one digit RBSD comparator circuits are described in Figure 11 and Figure 12 respectively. In this case the circuit is optimized in all aspects by the Heuristic algorithm. Chip Planner tool i.e the floor planning tool is used to create and edit regions on the FPGA chip and assign logic to these regions, which is shown in Figure 13.

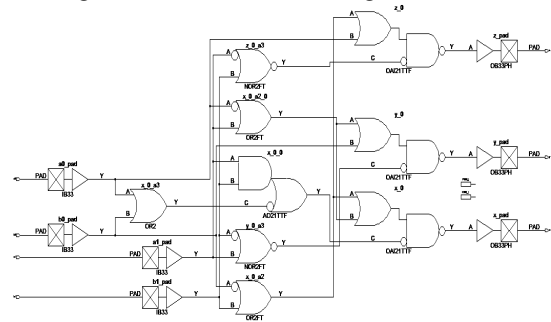


Figure 11 Pre Optimized Netlist of One Digit RBSD Comparator

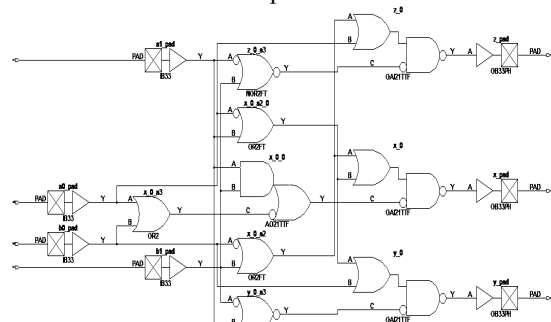


Figure 12 Optimized Netlist of One Digit RBSD Comparator

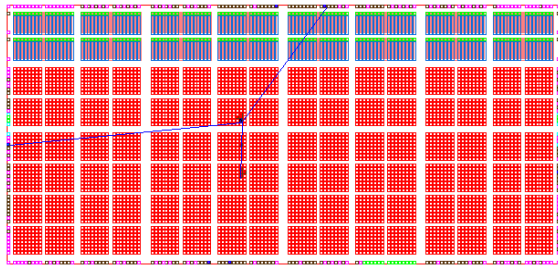


Figure 13 Chip Planner of One Digit RBSD Comparator

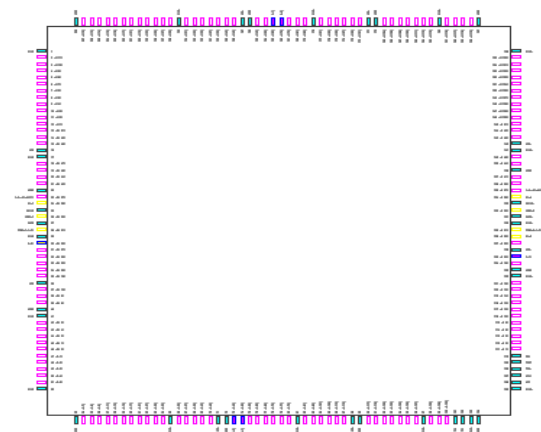


Figure 14 Pin Editor of One Digit RBSD Comparator

Pin Editor which is shown in Figure 14 is the package layout interface used to assign I/O ports to package pins. The I/O Attribute Editor displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format and is shown in Figure 15.

	Port Name	Macro Cell	Pin #	Locked	Output Load
1	y	ADLIB:OB33PH	74	☒	35
2	x	ADLIB:OB33PH	75	☒	35
3	z	ADLIB:OB33PH	125	☒	35
4	b1	ADLIB:IB33	182	☒	
5	a1	ADLIB:IB33	184	☒	
6	b0	ADLIB:IB33	183	☒	
7	a0	ADLIB:IB33	32	☒	

Figure 15. I/O Attribute Editor of One Digit RBSD Comparator

Delays for each path are calculated with the help of Actel's static timing analysis tool and shown in Figure 16.

Path	All Inputs	All Outputs	Actual
1	a1	z	9.17
2	a1	x	8.70
3	a1	y	8.66
4	b1	z	8.58
5	b0	z	8.53
6	b1	y	8.40
7	a0	x	8.35
8	b0	x	8.31
9	b1	x	8.26
10	a0	y	7.97
11	a0	z	7.73
12	b0	y	7.22

Figure 16. Timer Report of One Digit RBSD Comparator

The design-level power summary, at ambient temperature 25°C and junction temperature 25.3°C is described as follows:

Static Power Consumption : 8mW

Dynamic Power Consumption: 1.624mW (Behavioral Model)

Dynamic Power Consumption: 2.384mW (Data Flow Model)

4. Mask Level CMOS Layout Design of Comparator Circuits

The gate level comparator circuit is extracted by its FPGA implementation. To design the mask level layout, its corresponding CMOS circuit [Huang 2003] is required for the low power VLSI design, which can be achieved by writing its Verilog code. The mask level layout design is done by the high end EDA tool i.e. Microwind2, which is a *Layout and Simulation tool for deep submicron CMOS design* and supports Verilog as well as pSpice. The Layout Design tool supports design rule checker (DRC) checking and LVS (Layout Versus Schematic) Report of Full Chip, which scans all the design and verifies that all the minimum design rules are respected.

4.1 Layout Design of One Digit RBSD Comparator

4.1.1 Logic Diagram of One Digit RBSD Comparator

The schematic diagram of one digit RBSD comparator shown in Figure 17 is designed by DSCH2 tool and its corresponding Verilog codes are extracted for the design of its mask level layout diagram [Huang 2003], which are shown in Figure 18 and Figure 19 respectively.

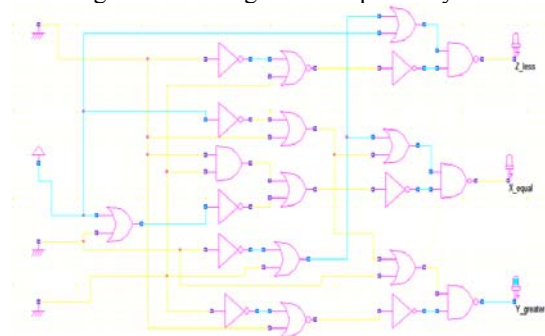


Figure 17 Logic Circuit of One Digit RBSD Comparator

4.2 Simulation on Layout

The simulation is performed directly on the layout. The most interesting layout files to be simulated in this mode are analog blocks such as the DAC and comparators. nMOS and pMOS are the basic building blocks of any CMOS circuit [Huang 2003] design. Here the designed

layout is a direct form of schematic diagram to Layout with the help of verilog code. In Figure 20 the VI characteristics of nMOS which is used for the layout design is shown. The dimension of nMOS is $W = 0.24 \mu\text{m}$ and $L = 0.12 \mu\text{m}$. Both nMOS and pMOS devices are symmetrical for getting sharp VTC (Voltage Transfer Characteristics).

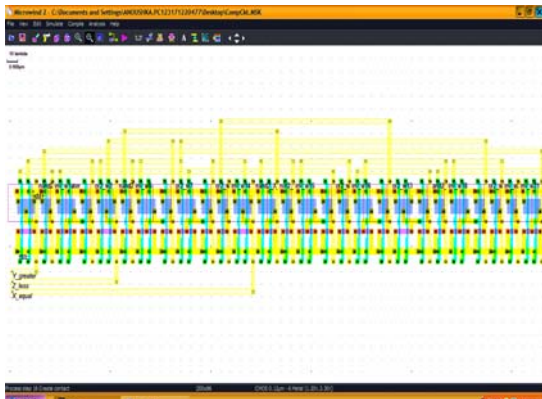


Figure 18 Layout Design of One Digit RBSD Comparator (Close View)



Figure 19 Layout Design of One Digit RBSD Comparator with palette of colors

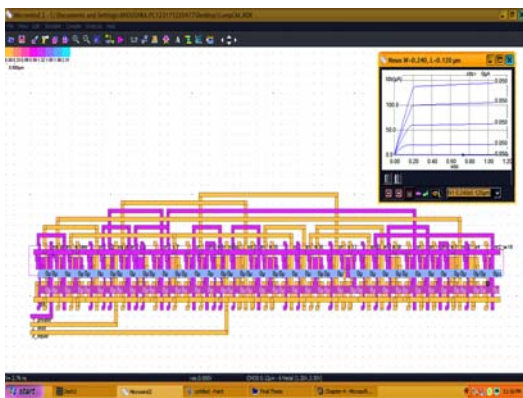


Figure 20 Simulations on Layout Design

The process view in 3 dimensions has been obtained by the Microwind2 tool, which is a *Layout and Simulation tool for deep sub micron CMOS design*. The steps of the CMOS process are illustrated in sequence in Figure 21 keeping in view the low power VLSI design [Lam 2006].

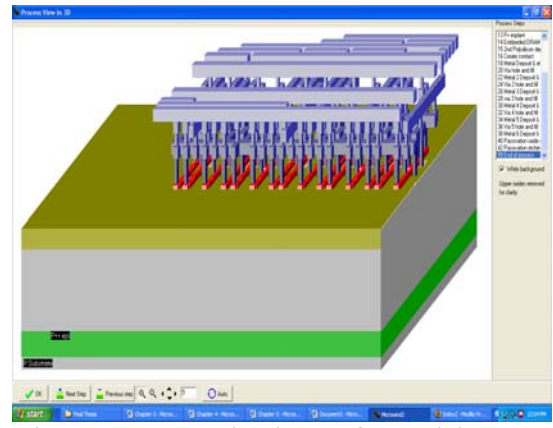


Figure 21 Process View in 3D of One Digit RBSD Comparator

The chip level layout design is done with the help of microwind2 tool. Here the technology used is CMOS $0.12 \mu\text{m} - 6 \text{ Metal}$. The length of channel (L) = $0.12 \mu\text{m}$ and width of the channel (W) = $0.24 \mu\text{m}$. The pad frame layout and the chip layout design are shown in Figure 22 and Figure 23 respectively.



Figure 22 Pad Frame Layout

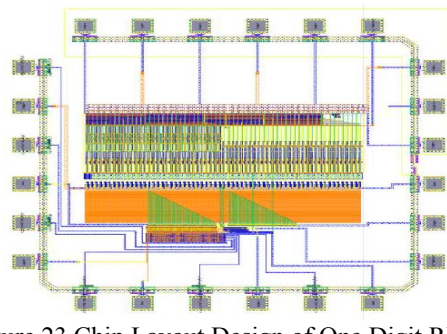


Figure 23 Chip Layout Design of One Digit RBSD Comparator

4.3 Layout Design of Two Bit Binary Comparator

The gate level comparator circuit is extracted by its FPGA implementation and is designed by the high end EDA tool i.e. DSCH2 and it is shown in Figure 4.13. The logic circuit is simulated and verified that it works properly as its RTL behavior. Its corresponding Verilog code is generated and is compiled by the layout generator tool i.e. Microwind2, which is a Layout and Simulation tool for deep sub micron CMOS design

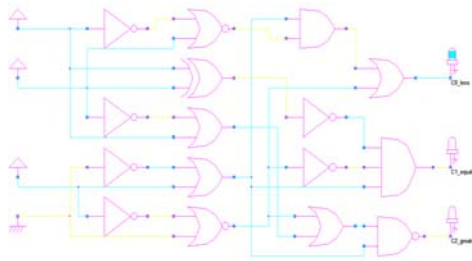


Figure 24 Logic Diagram of Two Bit Binary Comparator

The layout diagrams of two bit binary comparators are designed by Microwind2 and its corresponding CMOS circuit is designed in back end by this back end tool. Microwind supports Verilog for the design of mask level CMOS Layout diagram. The mask level Layouts of two-bit binary comparator in sub micron technologies are shown in Figure 25 and Figure 26, respectively. All the above lambda based CMOS layout design rules are valid and well respected by this tool.

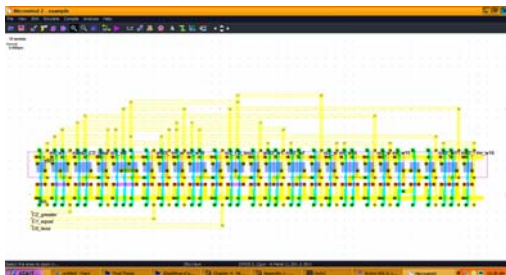


Figure 24 Layout design of Two Bit Binary Comparator (Close View)

4.3.1 Simulation on Layout & Process View in 3D

The simulation on layout is shown in Figure 26. The dimensions of nMOS are $W=0.24\mu\text{m}$ and $L=0.12\mu\text{m}$. Both nMOS and pMOS devices are symmetrical for achieving sharp VTC. The steps of the CMOS process are illustrated in sequence in Figure 27.

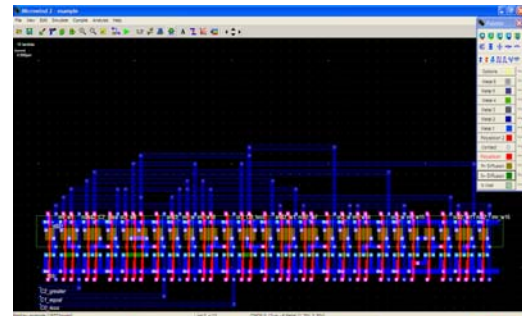


Figure 25 Layout design of Two Bit Binary Comparator with Palette of Colors.

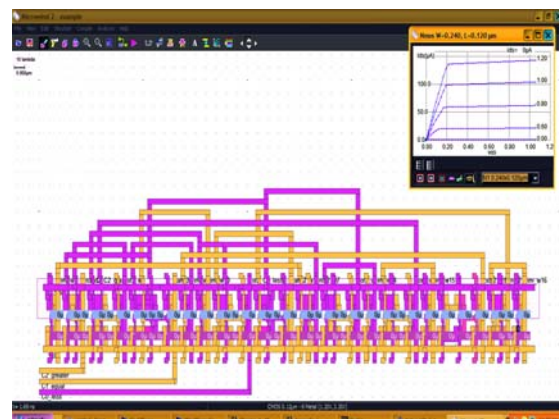


Figure 26 Simulation on Layout design of Two Bit Binary Comparator

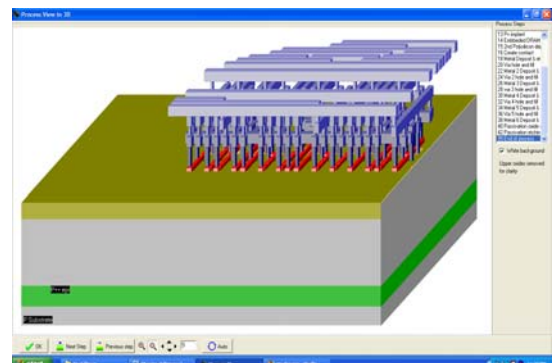


Figure 27 Process View in 3D Dimensions of Two Bit Binary Comparator

4.4 Simulation Results

In Voltage vs Time window the transient analysis of all visible signals are obtained. The delay between the selected start node and selected stop node is computed at $V_{DD}/2$. In Frequency & Voltages Windows so as to make all voltage curves appear in the lower window, and to plot the variation of the switching frequency of one selected signal. The IC Technology is CMOS $0.12\mu\text{m} - 6$ Metal. The

nMOS used in the Layout design is having width of $W=6.000\ \mu\text{m}$ and Length of $L=0.12\ \mu\text{m}$. The threshold voltage of nMOS in Level 3 is $V_{TO}=0.40$, which is used in this Layout design. The pMOS used in the Layout design is having width of $W=6.000\ \mu\text{m}$ and Length of $L=0.12\ \mu\text{m}$. The threshold voltage of pMOS in Level 3 is $V_{TO}=-0.45$, which is used in this Layout design.

5. Conclusion

SUMMARY OF COMPARISON

In this paper one Digit and two Digit Redundant Binary Signed Digit [Aviz 1961] Comparators and two digits Binary comparator have been designed by VHDL and its FPGA implementation has been done followed by its synthesis process. Various parameters such as Delay, Dynamic Power, Cell Count and Area are considered and enumerated in Table 2, for the comparison point of view.

RBSD vs Binary Comparator				
No. of Bits	Delay (ns)	Dynamic Power (mW)	Cell Count	Area*Cell Count
1 Digit RBSD (Beh)	13.72	1.624	17	9
1 Digit RBSD (DF)	9.17	2.384	18	9
2 Digit RBSD (DF)	13.46	2.498	42	21
2 Bit Binary	9.8	2.381	17	8

Table 2 Summary of Comparison

The summary of comparison is also represented in graphical form in Figure 28 and Figure 29 respectively. The various parameters of one digit RBSD comparator are represented in both Dataflow and Behavioral model. Though each digit of RBSD number system is represented by two bits as discussed earlier. So one digit RBSD comparator can be compared with two bit binary comparator.

It is seen from the graph that in case of two-bit binary comparator the cell count is 17 which is equal with RBSD comparator described in Behavioral model. But in case of design described in Dataflow model the cell count is comparable i.e. 18. As far as propagation delay is concerned it is very less i.e. 9.17 ns in case of RBSD comparator described in dataflow model. But it is very high i.e. 13.72 ns in case of behavioral model which is not comparable. But in case of binary comparator the propagation delay is 9.8 ns, which is higher than RBSD

comparator. If the area is taken into consideration then it's concluded that definitely binary comparator require less area rather RBSD, but the area requirement of RBSD is comparable with binary comparator. The last but not the least i.e. the Dynamic power consumption of one digit RBSD comparator are 1.624 mw and 2.384 mw respectively. But in case of binary comparator it is 2.381mw, which is approximately equal with RBSD comparator.

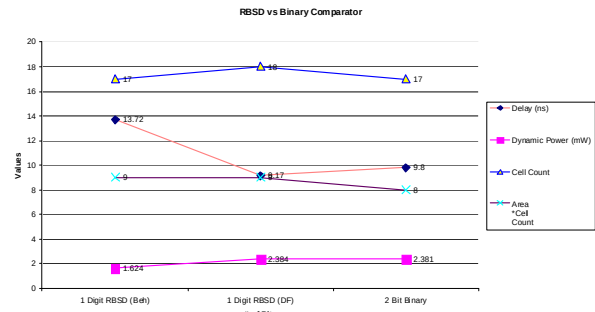


Figure 28 Comparison Graph between (One Digit) RBSD & Binary Comparators

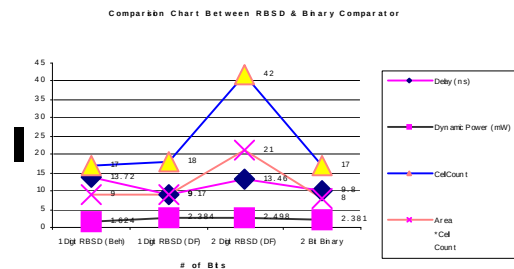


Figure 29 Comparison Graph between RBSD & Binary Comparators

In Figure 5.2 the various typical parameters of one digit and two digit RBSD comparators are shown in graphical manner and its comparative study with binary comparator can be visualized from this graph. As it is seen from the graph that in case of two digit RBSD comparator the complexity increases due to the rising curve of cell count as well as area. But in case of dynamic power requirement and propagation delay obviously the values are higher for two digit RBSD comparator but might be comparable with binary comparator.

This work presents techniques to increase the speed and improve the VLSI suitability in designing Redundant Binary Signed Digit arithmetic logic units (ALU). The regular interconnection structure of this comparator cell results for the VLSI implementation of complex comparator circuits. Here the increased speed is achieved through the technique of elimination of carry propagation

chain. This scheme results in a significant improvement in speed and is very efficient for comparator with larger operand. So this concept might be adopted for developing high-speed processors for computing purposes in all areas for the upcoming GSI (Giant Scale Integration) technology.

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