Architecture for Efficient Energy Meter

Vipan Kakkar
SMVD University, India.

Summary

This paper describes a low-power ARM7TDMI based architecture for use in energy meter. Energy metering device demands low power consumption and portable design. It must be able to calculate the energy consumed by a consumer and communicate this calculated data to the a remote central database. To meet this goal, this work proposes an ARM7TDMI based architecture that can be implemented on a single chip resulting in small size and low power consumption, at an enhanced performance. Various low-power and power management schemes have been used in this design. Furthermore, the design nature of this architecture will allow for scalability for further channel additions.

Keywords *:*
Energy meter, ARM7, AMR, signal processing, low power

1. INTRODUCTION

There is a need to remotely measure voltage and current parameters to calculate power consumed in industry and by the residential users. This power consumed is billed as KWH (Kilo Watt Hour), i.e. 1000 W of power consumed per hour. Currently, there is an urgent need to read this energy consumption by the consumer remotely at the central power station. This can be achieved by having an electronic metering device, which performs energy computations electronically and then communicates these computations with the remote station. The situation is depicted in Fig. 1.

As, very less work in electronic metering as one-chip solution is reported, therefore, this work gives directions in the energy metering devices as following: one-chip solution for the energy metering device, low power consumption of the device itself, remotely reading of the energy consumption. Therefore, work discussed here focuses on low power consumption with increased integration of components into a single SoC (System on Chip) thereby reducing the area. The low power and small area will enable low-cost meters in the near future; which is not possible with traditional approaches.

The system architecture described in this paper is ARM7TDMI based design, which provides an optimal combination of energy efficient microcontroller unit and low power signal processing for speech signals.

Next section will give an overview of the ARM7TDMI based architecture and the results of the system.

2. PROCESSOR SELECTION

Sampling input analog current and voltage signals for metering device at the required sample rate frequencies lead to use DSP (Digital Signal Processor). Unfortunately, there is no easy way to transfer algorithm implementation between two DSP architectures. The instruction sets heavily depend on hardware architecture and may be very different. Using the ARM architecture is a good way to eliminate this problem. The ARM instruction set is the same whatever the manufacturer of the chip is. When the C language is used to implement an algorithm, no problem with instruction set of a CPU arises.

An ARM7TDMI based CPU, is chosen for the sake of good compiler support, low cost and convenient system integration, such as SPI, I2C, Flash and external memory controller etc [4]. The ARM7TDMI processor has a relatively simple data path, and has a few advantageous DSP capabilities [6]. In fact, for many applications the ARM7TDMI is fast enough that the need for a second, dedicated DSP processor disappears. ARM7TDMI-based microcontrollers can perform multiple high-speed communications operations simultaneously. ARM7TDMI has large number of registers, 31 for general purpose compared with traditional programmable digital signal processors. Thus, it helps in reducing the memory accesses and enables good compiler performance. Secondly, most of the instructions can be executed conditionally, which

Manuscript received November 5, 2009
Manuscript revised November 20, 2009

reduces the control overhead significantly. Thirdly, it has a 32-bit barrel shifter that can simultaneously execute shift and rotation with ALU operations. This feature is useful for scaling and multiplication by 2 constant. Fourthly, ARM7TDMI is a pure load/store architecture, which moves 16 registers from or to memory using a single instruction [4].

Since, the ARM7TDMI processor core is usually augmented with cache memories to increase the performance. However, to further enhance the performance, number of accesses from external memory can be reduced by combining different processes wherever possible. This is especially important in portable devices, where the off-chip memories are usually slow because of cost and power consumption limitations.

In this paper it is described that the development of a fully integrated, low-power, ARM7TDMI core to perform filtering and processing of the ADC (Analog to Digital Converter) signal outputs. It also performs the energy calculations, enables the users to customize input/output configurations. It performs the tasks of memory control as well as peripheral control.

For energy computations and communications the timing is less critical, typically the higher level functions, the circuit makes good use of the ARM 7TDMI microprocessor core.

The processor is also used to run DSP algorithms and, at the same time, handles the communication protocol. The communication protocol, in this application, contains the MAC = Medium Access Control Layer. The program running on the microprocessor is stored into an on-board ROM. The working data necessary for the processing is stored in an internal RAM. For the back-end side, the link to the application hardware, a serial interface is provided.

2.1 Analog Front End

The Energy Measurement Front End is made up of the analog front end, which performs the active energy measurement calculations for the processor [1].

The analog front end comprises of programmable gain amplifiers, which give outputs to the three Sigma-Delta modulators for the sampling of the mains voltage, and two current channels, one for the line current, and second for the optional measurement of the Neutral current. These modulators convert the differentially connected analog voltage and current inputs into digital signals to be processed by the ARM processor. Also included in the analog front end is the voltage reference, which provides the temperature stability to the Sigma-Delta modulators.

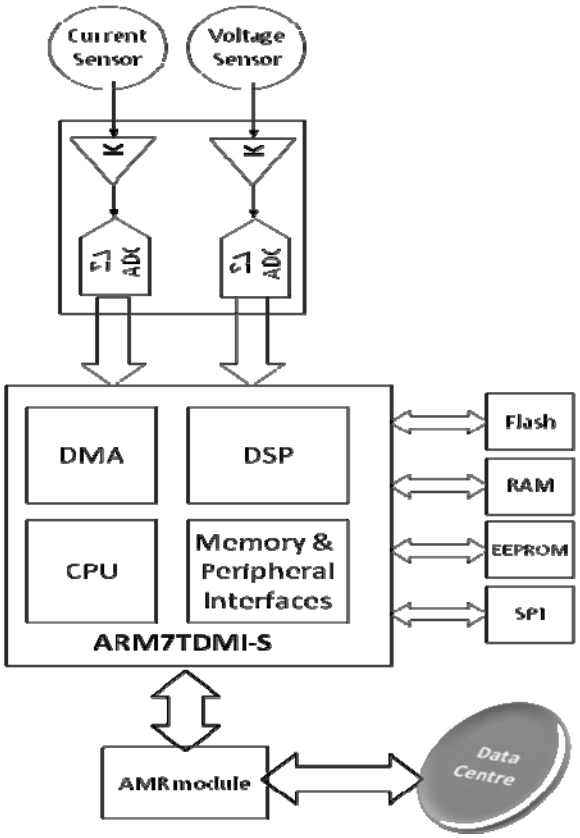

Fig. 1: Overview of the Energy Metering System

3. SYSTEM ARCHITECTURE

3.1 ARM7TDMI Based Subsystem

Fig. 3 shows the complete microsystem architecture consisting of the ARM7TDMI as a Central Processing Unit (CPU) as explained in this section, and the integrated peripherals. This subsystem includes lower compiler bottlenecks, additional communication interfaces, and decreased power consumption. This 32-bit processor contains a pipeline structure, 32kB of on-chip memory, cache, and several peripheral communication interfaces. This makes the microsystem

well suited for other bio-medical or environmental monitoring applications.

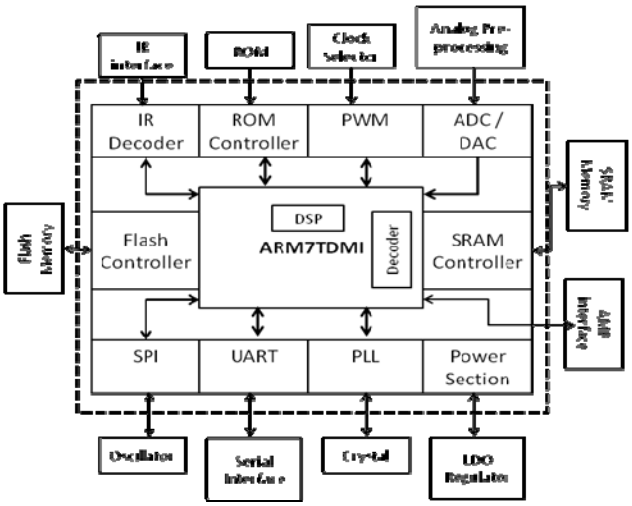

Fig. 2: ARM7TDMI based System Architecture

The communication with the calibration program stored in EEPROM is performed using SPI interface, and is controlled by the ARM processor. Control registers written by the processor software, are read by the processor memory management unit to give control of the read and write data buses for these components to the processor.

Since the dynamic range of the current can be large, a dynamic scaling method employing the block arithmetic is used. In order to further reduce the computation time, software optimization techniques are used, like loop fusion, loop unrolling, loop interchange, and post increment/ decrement conversion [7]. Note that the loop fusion and loop unrolling techniques reduce the computation time by minimizing the overhead of loop control. The performance can be further improved by employing ARM-CPU specific features, such as barrel-shifter, post/pre increment/decrement addressing, multiple register transfers, and conditional execution. Especially, the use of block transfer, LDM and STM, yields a very good result.

3.2 Signal Processing using ARM7TDMI

The output of the sigma-delta modulators are processed by the DSP block of the ARM processor. The DSP block provides the filtering and processing of the output data from the sigma-delta modulators. The DSP offers programming of measurement parameters and provides for fast and efficient meter production calibration procedures. The DSP performs harmonic computations, phase correction, filtering of DC offset, correction of the attenuation, in order to provide the ARM controller with the appropriate data and protocol to perform all the required meter functions. The reception channel filters the incoming serial digital signal, converts it to an analog signal and then amplifies and transmits the signal to AMR (Automatic Meter Reading) module.

3.3 Important Building Blocks

The ARM7TDMI based system architecture as shown in Fig. 2 consists of the following functional blocks:

The *CODEC is* used for receiving and digitizing the pre-processed input data from the current and voltage sensors.

The *ARM7TDMI core* is the core of the chip and is responsible for the processing of the incoming electrical signals. It also takes care of the communication with the outside world and accesses the off-chip flash memory. The core downloads all the processing parameters (patient dependent) from flash memory when the chip starts up. In this way, it also controls all hardware. Since control part of the core is normally in a power-down mode, its contribution to the power consumption of the chip is negligible.

A dedicated *UART* is designed to communicate with the PC and to directly send real-time data over this serial link, SPI is used for communication between CODEC and ARM7TDMI.

PWM is used for clock selection, memory controllers are also mentioned for interface to the memory blocks.

AMR (Automatic Meter Reading) is a remote reading system of reading meters using electronic equipment. Usage data is periodically sent to the central office through a signal being transmitted over the existing power lines or any other communication protocol. The system is reliable, secure, accurate and completely eliminates the need for physically reading the meters. It offers a better financial return due to the inclusion of other applications. See Fig. 1 for AMR module.

3.4 Benefits of Proposed Architecture

Energy savings: The smart metering with AMR can control the usage of energy using different tariffs. At peak times incentives to the end consumer can help control the energy consumption as well as energy generation. This can be achieved by two way communication between the supplier and the consumer, which in-turn comprises of intelligent software, communication media and data management systems. This savings in-turn will help reduce the carbon-footprint in the environment.

Tamper proof: Meter is made tamper proof to reduce thefts. Sofware techniques for metering management are used in order to control the tampering of the meter. Threshold energy monitoring can also be used for minimizing the thefts.

Data security: Remote reading and automatic data collection at stipulated intervals can help increase the data security by reducing manual errors.

4. LOW POWER DESIGN

The nature of the architecture provides for a significant reduction in hardware by pipelining the datapath and allowing all channels to share the same hardware for filters, DSP algorithms, supply harmonics etc. Control circuitry is also simplified by allowing the FSMs in the control unit to reuse states for each channel.

The most effective way of reducing dynamic power is reducing supply voltage, because the power consumption drops quadratically with the supply voltage (Eq. 1). Reducing the supply voltage with a factor of two yields a factor of four decrease in energy. There is, however, a penalty for reducing the supply voltage: circuit delays increase leading to reduced system performance (see Fig. 3).

$$P_{dyn} = \alpha f C_L V_{dd}^2 \qquad (1)$$

The proposed architecture has four operating modes: active, programming, test, and sleep.

For typical operation, the ARM7TDMI core will be in active mode and will process samples and generate stimulation pulses automatically. The controller part can be in standby mode during this time. Input data is received from the ADC through one of the shared SPI interfaces.

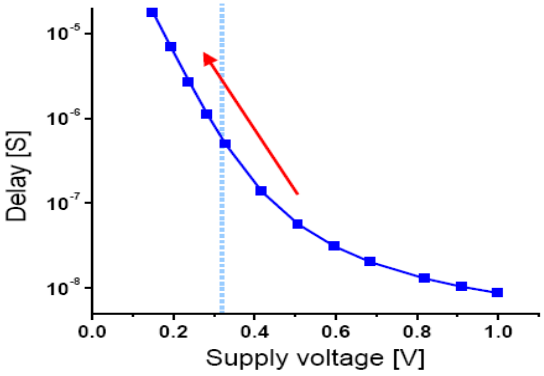

Fig. 3: Delay vs Supply Voltage

Programming mode will allow the processor to set up all filter coefficients, LUT data, and the stimulation profile. Test mode allows for any of the datapath stages to be bypassed via the multiplexors at each output node to provide observability and controllability over each component in the ARM7TDMI. Sleep mode allows all ARM7TDMI components to be shut down in order to conserve power. While in active mode, any unused datapath stages are shut down through the control unit by utilizing the existing sleep mode circuitry.

The proposed architecture has four operating modes: active, programming, test, and sleep.

For typical operation, the ARM7TDMI core will be in active mode and will process samples and generate stimulation pulses automatically. The controller part can be in standby mode during this time. Input data is received from the ADC through one of the shared SPI interfaces.

Programming mode will allow the processor to set up all filter coefficients, LUT data, and the stimulation profile. Test mode allows for any of the datapath stages to be bypassed via the multiplexors at each output node to provide observability and controllability over each component in the ARM7TDMI. Sleep mode allows all ARM7TDMI components to be shut down in order to conserve power. While in active mode, any unused datapath stages are shut down through the control unit by utilizing the existing sleep mode circuitry.

At the technology level, static leakage power has become a bane for low power designs. This leakage power is reduced by using high V_t transistors, thus

leading to low leakage drops, but compromising on performance, but still inside acceptable limits. However, for critical timing blocks, the high V_t cells from the cell libraries were used.

Other techniques, clock gating, DVS (Dynamic Voltage Scaling) and DVFS (Dynamic Voltage and Frequency Scaling) were used for lowering down the dynamic power consumption. DVFS reduces the supply voltage while slowing down the processor's clock frequency, thus yielding a quadratic reduction in power consumption, at the cost of increased run-time. The DVFS scheme used in this work is shown in Table 1.

Table 1: Overview of DVFS scheme

Power State	Control			
	Clock	Supply Voltage	Level Shifter	Regulator
Active	ON	ON	Connected	Normal operation
Standby	OFF	ON		
Powerdown	OFF	OFF	Isolated	Low power operation

5. RESULTS

5.1. Functional Simulation

As this design contains an ARM7TDMI processor and few hardware modules, we have to verify these modules and their integrity as a system. First, the functionality of the major hardware modules with test vectors was verified individually. Then, the integration of the hardware modules with the self-test program was verified.

To verify the function of the system, a testbench and test vectors are needed. Behavioral models were developed to reduce the simulation time. The models are developed in The behavioral model generates a clock and communicates with the system with given communication data in a text file. It provides the system with appropriate data, receives responses from the system, and compares the responses with expected responses stored in the data file. If the response and expected response matches, then the model proceeds to the next communication data. If they do not match, the model reports error messages with a current status. The tools used were ModelSim and Seamless CVE [8] for RTL simulation and software debugging. C-language and instantiated in the testbench with a foreign language interface feature [5].

5.2 Power Simulations

In order to reduce power consumption, timing critical functional-logic use higher supply voltage and low V_T cells, and non-critical logic use lower supply voltage and high V_T cells. DVFS and other techniques as mentioned in section 5 were applied during the system design. Table 1, gives overview of the DVFS scheme implemented in the design.

Synopsys Prime Power was used in cycle-by-cycle power simulation, whose procedure is described in [6] in detail. Low power techniques used in this design enabled power savings as shown in Table 1. The whole design as shown in the dotted area of Figure 3, consumes active power of less than 2 mA at an area of less than 4 mm^2.

Table 2: Summarized Data on Power Savings

Technique	Power savings (%) using multiple Vdd Domains	
	Vdd = 1.0V	Vdd = 0.8V
Dynamic	11	32
Leakage	34	30

6. CONCLUSIONS

Low power architecture for ARM7TDMI based energy metering device was designed and verified. The design is simulated in 130 nm CMOS technology for one-chip solution. Previous energy meters use discrete components and 8051 microcontroller. This architecture is one of the newest and efficient as explained in previous sections of this paper. It also incorporates various low power techniques were implemented, and power savings in leakage power as well as dynamic power were calculated. With the architecture described in this paper almost 40% reduction in leakage power was noticed, and overall 30% reduction in dynamic power was observed.

REFERENCES

[1] Austria Microsystems AG, AS8267 Datasheet, Single Phase 2-current Energy Measurement IC, 2007.
[2] Analog Devices Inc, ADE7116 Single Phase Energy Measurement IC Datasheet, 2008.
[3] Texas Instruments Inc, MSP430F471x6 Datasheet, 2009.
[4] ARM Ltd. ARM Architecture Reference Manual. ARM DDI 0100E. www.arm.com, (2000).
[5] Model Technology Inc., ModelSim Foreign Language Interface, Version 6.4.
[6] Jang, Y., Shin, Y., Hong, M., Wee, J., Lee, S.: Low-Power 32bit x 32bit Multiplier Design with Pipelined Block-Wise Shutdown, Lecture Notes in Computer Science 3769, 398-406 (2005).
[7] V.Zivojnovic, "Compilers for Digital Signal Processors," DSP & Multimedia Technol., vol.4, no.5, pp.27-45, (July 1995).
[8] Mentor Graphics Corp., Seamless CVE User's and Reference Manual: Version 5.0, (2003).

Vipan Kakkar received his B.Tech degree and M.Tech. degrees in Electrical Engineering in 1995 and 1997, respectively. He received his doctorate in Microelectronics from Delft University of Technology, Netherlands in 2002. During 1999-2008, he worked in Netherlands in VLSI design for audio and video applications. He worked in Philips, Netherlands for 10 years at different positions. Presently, he is working as Associate Professor in school of Electronics and Communications Engineering at SMVD University, India.