Perfect Difference Network for Network-on-Chip Architecture

Mahendra Gaikwad† and Rajendra Patrikar††,

†Professor & Head, Department of Computer Engineering, B. D. College of Engineering, Sevagram, 442 102 India
†† Professor & Head, Department of Electronics &Computer Science, VNIT, Nagpur, 440 011 India

Summary

Network-on-Chip (NoC) is a new paradigm for designing core based System-on-Chip. Network-on-Chip has been proposed as a solution for addressing the design challenges of future high performance nanoscale architectures. Innovative system-level performance models are required for designing NoC based architectures. In this paper, we discuss the possibility of achieving the energy-aware NoC architecture based on the mathematical notion of Perfect Difference sets (PDS). We present the analytical energy model for NoC platform using Perfect Difference Network (PDN). The proposed energy model is then validated against the simulation results obtained with Inter-tile link geometry and PDN circular geometry for NoC architecture. Significant energy saving is achieved for Perfect Difference Network with circular geometry in comparison with inter-tile geometry of NoC architecture on the basis of our proposed energy model.

Key words:
Network-on-Chip (NoC), Perfect Difference Network (PDN).

1. Introduction

System-on Chips (SoCs) are designed as a tightly interconnected set of cores, where all components share the same system clock. There is a need to treat SoCs as Network-on-Chip where the interconnections are designed using an adaptation of the protocol stack. Network-on-Chip (NoC) is a new paradigm for designing core based system on chip, where various Intellectual Property (IP) resource nodes are connected to the router-based square network of switches using resource network interface. NoC supports high degree of reusability and is scalable. Energy consumption of a VLSI system became one of the most important factors to optimize in most of the designs due to factors such as the expanding market for mobile products, the increasing cooling cost, etc.

Though the technology in computer network is well developed, a direct adaptation of network protocols to NoCs is impossible, due to different communication requirements, cost considerations and architectural constraints. The design goals for NoCs can be described as

(i) Platform based design.
(ii) Separation between communication and computing resources.
(iii) Minimization in energy and area.

Platform based design is essential for modular network. Network can be made reusable by separating the communication infrastructure from computing resources. A lot of research is going on to develop appropriate network architectures to meet the requirements. This paper summarizes the concept of Perfect Difference Network to minimize the communication energy by proposing the energy model of NoC architecture for Inter-tile geometry in comparison with PDN Circular geometry. Section 2 explains Inter-tile geometry of NoC architecture. Section 3 and section 4 explains Perfect Difference Set and Perfect Difference Network in detail along with theorems & definitions. Perfect Difference Network for Network-on-Chip architecture and energy model for NoC are explored in section 5 and section 6. Simulation results obtained with Inter-tile link geometry and PDN circular geometry for NoC architecture are explained in section 7. Finally paper is concluded in section 8.

2. NoC Architecture

S. Kumar et. al. have proposed 2-D mesh Chip-level Integration of Communicating Heterogeneous Elements (CLICHE) model [5] where each switch is connected to other four neighboring switches through input and output channels. This model is a heterogeneous network of resources where communication between resources is implemented by passing messages over the network. Mesh architecture is built by its dimension d and radix k. The total number of switches is k^d. The k^d switches are organized in an d *-dimensional* grid such that there are k switches located in each dimension and wrap-around connections. Since the number of IPs that can be connected to one switch is d *-1*, the total number of mounted IPs is calculated by

$$N_{Mesh} = k^d (d-1) \quad (1)$$

The total bandwidth of the network is obtained by

$$B_{Mesh} = 2 k^d b \quad (2)$$

Where, b is the unidirectional bandwidth. Moreover, Mesh architecture offers a simple connection scheme and hence

Manuscript received December 5, 2009
Manuscript revised December 20, 2009

the shortest path routing is mostly applied on it. The total number of the mounted IPs is relatively high compared to the total bandwidth hence the performance of Mesh architecture is low.

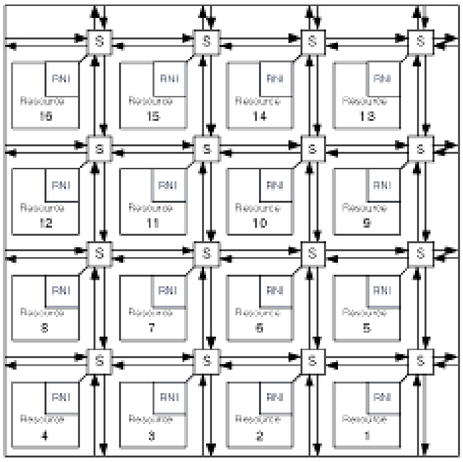

Fig. 1 4 X 4 Mesh Inter-tile based CLICHÉ NoC architecture

3. Perfect Difference Set

Prefect difference set provides the mathematical tool for achieving the optimum number of IP cores or nodes and their interconnections. Perfect difference sets were first discussed by J. Singer in 1938 in terms of points and lines in a finite projective planes [7].The definition and theorems for formulating Perfect Difference sets are stated as under [8].

Theorem 1: A sufficient condition that there exist $\delta + 1$ integers $s_0, s_1, \ldots, s_\delta$ having the property that their $\delta^2 + \delta$ differences $s_i - s_j$, $0 \leq i \neq j \leq \delta$, are congruent, modulo($\delta^2 + \delta + 1$), to the integers $1, 2, \ldots, \delta^2 + \delta$ in some order is that δ be a power of a prime.

Definition 1: Perfect difference set (PDS) – A set { $s_0, s_1, \ldots, s_\delta$ } of $\delta + 1$ integers having the property that their $\delta^2 + \delta$ differences $s_i - s_j$, $0 \leq i \neq j \leq \delta$, are congruent, modulo ($\delta^2 + \delta + 1$), to the integers $1, 2, \ldots, \delta^2 + \delta$ in some order is a *perfect difference set* of order δ. Perfect difference sets are sometimes called simple difference sets. PDS need not contain an integer outside the interval $[0, \delta^2 + \delta]$, because any integer outside the interval can be replaced by another integer in the interval without affecting the defining property of the PDS.

Theorem 2: Given a PDS $\{s_0, s_1, \ldots, s_\delta\}$ of order δ, the set $\{as_0 + b, as_1 + b, \ldots, as_\delta + b\}$, where a is prime to $\delta^2 + \delta + 1$, also forms a perfect difference set. By definition, any perfect difference set contains a pair of integers s_u and s_v such that $s_u - s_v \equiv 1 \bmod (\delta^2 + \delta + 1)$. By Theorem 2 and the observation that preceded it, subtracting s_u from all integers in such a PDS yields another PDS that contain 0 and 1

Definition 2: Normal PDS – A PDS { $s_0, s_1, \ldots, s_\delta$ } is reduced if it contains the integers 0 and 1. A reduced PDS is in normal form if it satisfies $s_i < s_i+1 \leq \delta^2 + \delta$, $0 \leq i < \delta$.

Definition 3: Equivalent PDSs – Two different PDSs are equivalent iff they have the same normal form $\{0, 1, s_2, \ldots, \ldots s_\delta\}$.

Property 1: Multiplicity- For any order δ , there exist more than one PDS.

Perfect Difference sets with order δ as a power of prime number and number of nodes, $n = \delta^2 + \delta + 1$ are stated in the table 1.

Table 1: PDS of order δ in normal form and $n = \delta^2 + \delta + 1$

δ	n	PDS of order δ in normal form
2	7	0, 1, 3
3	13	0, 1, 3, 9
4	21	0,1,4,14,16
5	31	0,1,3,8,12,18
7	57	0,1,3,13,32,36,43,52
8	73	0,1,3,7,15,31,36,54,63
9	91	0,1,3,9,27,49,56,61,77,81
11	133	0,1,3,12,20,34,38,81, 88,94,104,109
13	183	0,1,3,16,23,28,42,76,82, 86,119,137,154,175
16	273	0,1,3,7,15,31,63,90,116,127,136, 181,194,204,233,238,255

4. Perfect Difference Network

We can construct a direct interconnection network with $n=\delta^2 + \delta + 1$ nodes based on the normal form perfect difference set { $s_0, s_1, \ldots, s_\delta$ } with order δ.

Definition 1. Perfect difference network (PDN) based on the PDS { $s_0, s_1, .., s_\delta$ } There are $n= \delta^2 + \delta + 1$ nodes, numbered 0 to n-1. Node *i* is connected via directed links to nodes $i\pm1$ and $i\pm s_j (\text{mod } n)$, for $2 \leq j \leq \delta$. For each link from node i to node j, the reverse link from node j to node i is also exists, hence the network can be drawn as an undirected graph.

Perfect difference networks based on normal form PDSs are special types of chordal rings. In the terminology of chordal rings, the links connecting consecutive nodes i and i+1 are ring links, while those that connect nonconsecutive nodes i and $i\pm s_j (\text{mod } n)$, for $2 \leq j \leq \delta$, are skip links or chords. The link connecting nodes i and $i+s_j (\text{mod } n)$, for $2 \leq j \leq \delta$ is a forward skip link of node i and a backward skip link of node $i+s_j (\text{mod } n)$.

5. Perfect Difference Network for Network-on-Chip Architecture

For better understanding of the network, we consider the chordal ring structure of the PDN for n=13, based on the PDS {0,1,3,9 }, is shown in Figure 2. Any two nodes in a PDN are either connected by a link directly or via a path of length 2 through an intermediate node. There are different possibilities of collective communications among all the pairs of nodes of PDN like One to all, All to all. Maximum message that can be broadcast from any node to all other nodes will be $\delta^2 + \delta$. Routing in PDN is very simple and efficient and message can be routed among the nodes through one or two hopes.

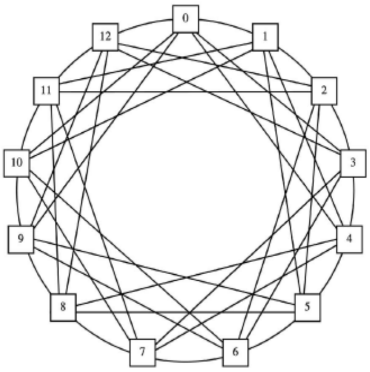

Fig. 2 Chordal Ring structure of PND for n=13.

One to all broadcasting can be obtained from Node'3' to all other nodes as given in the Table 2.

Table 2: Broadcasting of Node '3' to all other Nodes

Source Node	Destination Node	Route	Type of Link	No. of Hops
Node '3'	Node '0'	3-0	Skip Link	1
Node '3'	Node '1'	3-0-1	Skip Link-Ring Link	2
Node '3'	Node '2'	3-2	Ring Link	1
Node '3'	Node '4'	3-4	Ring Link	1
Node '3'	Node '5'	3-6-5	Skip Link-Ring Link	2
Node '3'	Node '6'	3-6	Skip Link	1
Node '3'	Node '7'	3-7	Skip Link	1
Node '3'	Node '8'	3-7-8	Skip Link-Ring Link	2
Node '3'	Node '9'	3-12-9	Skip Link-Skip Link	2
Node '3'	Node '10'	3-0-10	Skip Link-Skip Link	2
Node '3'	Node '11'	3-12-11	Skip Link-Ring Link	2
Node '3'	Node '12'	3-12	Skip Link	1

The parameters of PDN with order δ=3 are summarized as follows

(i) Order = δ=3
(ii) No. of Nodes = n= $\delta^2 + \delta + 1 = 13$ (Node numbered 0 to 12)
(iii) Perfect Difference Sets in normal form are {0,1,3,9} and {0,1,4,6}, According to Multiplicity Property of PDS, more than one PDS may exist for same value of δ.
(iv) Degree of undirected chordal ring = d= 2 δ = 6
(v) Diameter = D=2
(vi) One to all broadcasting messages = $\delta^2 + \delta = 12$

5.1 Shift Permutation Routing

Shift permutation routing is used in PDN for routing the messages among nodes through one or two hops. It is simple & efficient technique of routing either for n-messages or 2n messages. Shift permutation routing for PDN with order δ=3 based on the PDS {0,1,3,9 }is stated in the Table 3

Table 3: Shift Permutation Routing with order 3

n- message		**2n- message**	
Node	**Shift Permutation Routing**	**Node**	**Shift Permutation Routing**
0	3	0	2
1	4	1	3
2	5	2	4
3	6	3	5
4	7	4	6
5	8	5	7
6	9	6	8
7	10	7	9
8	11	8	10
9	12	9	11
10	0	10	12
11	1	11	0
12	2	12	1

6. Energy Model using Perfect Difference Network

We consider the chordal ring structure of the PDN for n=13, based on the PDS {0,1,3,9 }, to obtain average energy consumption of sending one bit of data from one node to another node. Projective geometry gives many mathematical approaches for arranging nodes in graphical manner. All the nodes are arranged in circular fashion forming the chordal ring as shown in figure 2.

We assume the NoC to be composed of chordal ring structure of PDN for n=13, based on the PDS {0,1,3,9}. Let us see how the Node '0' is connected to other nodes of PDN for n=13, based on the PDS {0,1,3,9}. For node '0', ring links are i±1, that is 1 and -1 ≡ 12. Similarly for node

'0', skip links are i±s_j(mod n), for $2 \le j \le \delta$, that is, 0±s_j(mod 13), for $2 \le j \le 3$ which gives 0±s_2(mod 13) and 0±s_3(mod 13), 0±3(mod 13) and 0±9(mod 13), 3(mod 13) & -3(mod 13) and 9(mod 13) & -9(mod 13), 3(mod 13) ≡ 3 & -3(mod 13) ≡ 10 and 9(mod 13) ≡ 9 & -9(mod 13) ≡4, Node '3' & Node '10' and Node '9' & Node '4'

Hence Node '0'forms ring links with Node '1' and Node '12' whereas skip links with Node '3' & Node '10' and Node '9' & Node '4'. Similarly same procedure is applied to all remaining nodes from node '1' to node '12' to get the chordal ring structure of PDN for n=13, based on the PDS {0,1,3,9 }as shown in figure 2.

The length of link from one node to another node is not fixed, hence the average energy consumption of sending one bit of data on the link varies with respect to the length of link. Therefore length of either Skip Link or Ring Link plays key role for minimization of energy consumption for NoC.

Here we are proposing the formula to calculate the length of either skip link or ring link from one node to another node. The length of link 'L' is given by

$$L = 2r\sin\left(\pi\alpha / n\right) \quad (3)$$

$$\alpha = \begin{cases} |n_d - n_s| & \text{If } (n_d - n_s) < 2\delta \\ |n - (n_d - n_s)| & \text{If } (n_d - n_s) > 2\delta \end{cases} \quad (4)$$

Where,

r = Radius of chordal ring

δ = Order of PDS

n = Number of node = $\delta^2 + \delta + 1$

n_d = Destination Node No.

n_s = Source Node No.

In our proposed energy model using perfect difference network, the average energy consumption of sending one bit of data from one node to another node is given by

$$E_{bit}^{ti,tj} = n_{hops}(E_{Rbit}) + E_{Lbit\_ring} + E_{Lbit\_skip} \quad (5)$$

Where,

n_{hops} = Number of router bit passes =Number of hops+1

E_{Lbit_ring} = Average energy consumption for transferring one bit of data through a ring link

E_{Lbit_skip} = Average energy consumption for transferring one bit of data of a skip link

For transferring the data from Node '3' to Node '12', number of router the bit passes and number of links is given by,

Number of hops = 1

Number of router the bit passes = Number of hops + 1 = 2

Number of ring link = 0

Number of skip link = 1

The average energy consumption of sending one bit of data from Node'3' to Node '12' is given by,

$$E_{bit}^{ti,tj} = 2(E_{Rbit}) + E_{Lbit\_skip} \quad (6)$$

Details of PDN for n=13, based on the PDS {0,1,3,9 } for transferring the data from Node '3' to Node '12'are summarized as follows

(i) Number of nodes = n= 13
(ii) Destination node number = n_d = 12
(iii) Source node number = n_s = 3
(iv) Order of PDS = δ =3
(v) $\alpha = n - (n_d - n_s) = 13 - 9 = 4$

Length of skip link E_{Lbit_skip} from node '3' to node '12' is given by,

$$L = 2r\sin\left(\pi\alpha / n\right) \quad (7)$$

7. Simulated Results

Average energy consumption of sending one bit of data through router from one node to another node for PDN with order 'δ'=3 circular geometry in comparison with inter-tile link geometry of NoC architecture on the basis of our proposed energy model are presented in the table shown below

Table 4: Average Energy consumption in (pJ)

Source Node	Destination Node	Average energy consumption (pJ)	
		Inter-tile link Geometry	PDN circular Geometry
Node '3'	Node '4'	2.3088 pJ	0.84270 pJ
Node '3'	Node '5'	1.8201 pJ	1.57009 pJ
Node '3'	Node '6'	1.3314 pJ	1.08139 pJ
Node '3'	Node '7'	0.8427 pJ	1.17140 pJ
Node '3'	Node '8'	2.7975 pJ	1.66010 pJ
Node '3'	Node '9'	2.3088 pJ	1.89879 pJ
Node '3'	Node '10'	1.8200 pJ	1.89879 pJ
Node '3'	Node '11'	1.3314 pJ	1.66010 pJ
Node '3'	Node '12'	3.2862 pJ	1.17140 pJ
Node '3'	Node '0'	1.8200 pJ	1.08139 pJ
Node '3'	Node '1'	1.3314 pJ	1.57009 pJ
Node '3'	Node '2'	0.8427 pJ	0.84270 pJ

9. Conclusion

Significant energy saving is achieved using for transferring random stream of data from one node to another node for Perfect Difference Network with order ‘δ’=3 circular geometry in comparison with Inter-tile link geometry of NoC architecture on the basis of our proposed energy model.

References

[1] P. Guerrier and A. Greiner, “A generic architecture for on-chip packet-switched interconnections”, In Proc. Design Automation and Test in Europe Conf. (DATE), pages 250-256, 2000.

[2] Semiconductor Association, “The International Technology Roadmap for Semicondutors (ITRS)”, 2004.

[3] H. Chang, L. Cooke, M. Hunt, G. Martin, A. McNelly, and T. Todd, “Surviving the SoC revolution”, Kluwer Academic Publisher, 1999.

[4] W. J. Dally and B. Towles, “Route packets, not wires: on-chip interconnection networks”, In Proc. Design Automatin Conf. (DAC), pages 684-689, June 2001.

[5] S. Kumar, A. Jantsch, M. Millberg, J. Oberg, J. Soininen, M. Forsell, K. Tiensyrja, and A. Hemani, “A network on chip architecture and design methodology”, In Proc. Symposium on VLSI, pages 105-112, April 2002.

[6] T. Ye, L. Benini, and G. De Micheli, “Analysis of power consumption on switch fabrics in network routers”,In Proc. Design Automatin Conf. (DAC), June 2002

[7] Singer, J., “A Theorem in Finite Projective Geometry and Some Applications to Number Theory,” *Trans. American Mathematical Society*, Vol. 43, pp. 377-385, 1938.

[8] B. Parhami, M. A. Rakov, “Performance, Algorithmic, and Robustness Attributes of Perfect Difference Networks”, IEEE Transactions on Parallel and distributed systems, Vol. 16., No. 8, August 2005.

[9] J.P. Uyemura “Circuit Design for CMOS VLSI”,Kluwer Academic Publishers,1992

†**Mahendra A. Gaikwad** did his BE in Electronics Engineering in 1991 from Nagpur University. He did his MBA in Marketing Management from Nagpur University and he has completed his MCM from Nagpur University. He did his Master’s Degree in Personal Administration from Nagpur University. He did his M.Tech in Communication Engineering from Indian Institute of Technology, Bombay in 1998. Currently he is doing his PhD on “Power Optimization in Network -on-Chip architecture” at VNIT, Nagpur. Currently he is working as Dean (R&D), Professor & Head, Department of Computer Engineering at Bapurao Deshmukh College of Engineering, Sewagram (Wardha). He is the life member of professional bodies like Indian Society for Technical Education, Institution of Engineers (India), Indian Society for Telecommunication Engineers. He is also invitee member of Institution of Engineers (India), Nagpur local Chapter, Nagpur. He is the member of Computer Society of India

††**Dr.Rajendra Patrikar** did his M.Sc. in Physics from Nagpur University. He did M.Tech in Electrical Engineering from IIT Bombay. He joined as Research engineer in the Microelectronics Project at IIT Bombay. He completed his Ph.D from the same department. He joined as faculty at IIT Bombay after working for a year at Computervision R&D Pune. Later he moved to Singapore to work in TECH Semiconductor in Advance Device Technology. After working there for three years he moved Institute of High Performance Computing Singapore where he carried research work in the area of CAD for VLSI and nano-electronics. He has published about 30 papers International Journals, international conferences and also filed one patent in USA in the area of VLSI Currently he is working as a professor & Head, Electronics and Computer Science Department VNIT Nagpur.