A Wideband Low Jitter Frequency Synthesizer Modeling and Simulation

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Abstract
This paper presents modeling and simulation of a wideband low jitter frequency synthesizer. The proposed system uses two phase-locked loops (PLLs) connected in cascade. The first PLL uses a voltage-controlled crystal oscillator (VCXO) to eliminate the input jitter and the second one is a wideband PLL. One important advantage of using the proposed system is that it uses only one VCXO for multiple carrier frequencies, while reducing the jitter considerably. The MATLAB Simulink simulation results show that the jitter could be minimized while working at different carrier frequencies.

Key words:
Wideband Low Jitter, Synthesizer

I. INTRODUCTION

Jitter is defined as the misalignment of edges in a sequence of data bits from their ideal positions. It occurs when data rates increase in high-speed input and output connections for data communications. Characterizing jitter and its measurement is a challenge. Especially, timing jitter is of great concern in high frequency timing circuits. Its presence can degrade the system performance in many high-speed applications.

Jitter can be expressed in units of time such as picoseconds (ps). It is also specified in other units, such as a percentage of frequency. All jitter measurements are made at a specified voltage, called the threshold voltage.

Jitter measurements can be classified into three categories:

- cycle-to-cycle jitter
- period jitter
- long-term jitter

Jitter is caused by several factors such as:

- Power supply noise passing through a phase locked loop (PLL) produces an output signal with a jitter [1].
- Noise on the PLL's reference frequency signal: a PLL in a frequency synthesizer has a dead-band associated with it, during which the phase and frequency detector does not detect small changes in the input phase. Since these changes are not detected, they do not get corrected and appear on the outputs in the form of jitter [2-3].
- Random thermal noise from the crystal reference, or any other resonating device [4].
- Random mechanical noise from vibrations of the crystal reference [5].
- Optical and electrical connectors and cables [6].
- Internal switching noise [7].
- Cross-talk, which produces phase variations in the transmitted digital signal and arises from magnetic fields generated by nearby signals [8].

Most research focuses primarily on using narrow band PLL systems that support only one communication standard. However, there is a need to build a flexible system that supports multiple communication standards and in the meantime works over a wide range of frequencies and meets all the requirements of the individual standards in a telephone carrier. The objective of this paper is to model and simulate a wideband frequency synthesizer using two PLLs.

The paper is organized as follows: Section II presents the mathematical model of the system. In section III, we present the Simulink model and the simulation results of the proposed system. Some concluding remarks are discussed in section IV.

II. MATHEMATICAL MODEL OF THE SYSTEM

The block diagram shown in figure 1 illustrates the wideband system which uses two cascaded PLLs. The first one uses a voltage-controlled crystal oscillator (VCXO) with a centre frequency f_x, not necessarily equal to f_{in}. The second one is a narrow band PLL with wide sweep range.

The first loop is represented by (1) and the second loop is represented by (2), both equations are derived directly from equations of the basic PLL. It is worth mentioning that the proposed mathematical model is still insufficient because it deals with phase noise and does not deal directly with jitter.

Since all available techniques for measuring jitter are digital, it was necessary to use a Simulink tool to simulate

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the jitter. Details of measuring the simulation results will be discussed in section III. The output phase related to the input is given in (1).

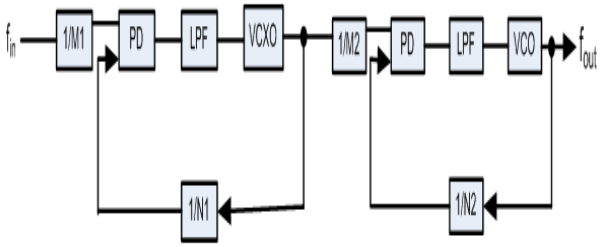

Figure 1. Dual PLLs for wideband frequency synthesizer

$$\theta_{op1}(s) = \theta_{ref}(s)\left(\frac{NK_1^*}{Ns + K_1^*}\right) \tag{1}$$

where, θ_{op1} represents the output phase of the first loop, θ_{ref} represents the input phase, N represents the frequency-divider ratio and K_1* represents the gain of the first loop.

$$\frac{\theta_{op2}(s)}{\theta_{op1}(s)/M} = \frac{K_{p2}K_{F2}(s)K_{V2}}{s + K_{p2}K_{F2}(s)K_{V2}\dfrac{1}{N}} \tag{2}$$

In (2), θ_{op2} represents the output phase of the second loop, and M represents the frequency-divider ratio

$$\frac{\theta_{op2}(s)}{\theta_{op1}(s)} = \frac{1}{M}\left(\frac{NK_2^*}{Ns + K_2^*}\right) \tag{3}$$

where, K_2* represents the gain of the second loop.

$$\theta_{op2}(s) = \frac{\theta_{op1}(s)}{M}\left(\frac{NK_2^*}{Ns + K_2^*}\right) \tag{4}$$

$$\theta_{op2}(s) = \theta_{ref}(s)\left(\frac{NK_1^*}{Ns + K_1^*}\right)\left(\frac{NK_2^*}{Ns + K_2^*}\right)\frac{1}{M} \tag{5}$$

$$\frac{\theta_{op2}(s)}{\theta_{ref}(s)} = \frac{N^2K_1^*K_2^*}{(Ns + K_1^*)(MNs + MK_2^*)} \tag{6}$$

$$\frac{\theta_{op2}(s)}{\theta_{ref}(s)} = \frac{N^2K_{p1}K_{V1}K_{F1}(s)K_{p2}K_{V2}K_{F2}(s)}{(Ns + K_1^*)(MNs + MK_2^*)} \tag{7}$$

It is clear from (7) that the overall output to input phase ratio is directly proportional to the square of the frequency dividing ratio. To simplify the mathematical equations, the values for M_1 and M_2 are set equal to M and the values for N_1 and N_2 are set equal to N. The system is simulated using Simulink.

III. SIMULINK MODEL OF THE PROPOSED SYSTEM

Figure 2 illustrates a technique for generating a jitter signal using MATLAB-Simulink model. It has been used to generate a jitter signal [9] and to measure the jitter in the first and second loop [10]. This circuit uses a sine wave block from Simulink library which generates a pure sine wave without any noise and it is passed through a zero crossing detector with a defined reference, to get a clean square wave output.

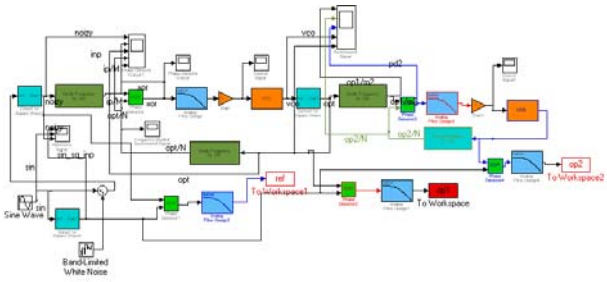

Figure 2. Simulink model of the proposed system

The other signal is the same sine wave with added white noise and it is also passed through a zero crossing detector to obtain the jittered signal. Then, both the jittered signal and the clean signal are passed through a phase detector followed by a low pass filter and finally to the M-file to calculate the jitter as shown in the block diagram of figure 3.

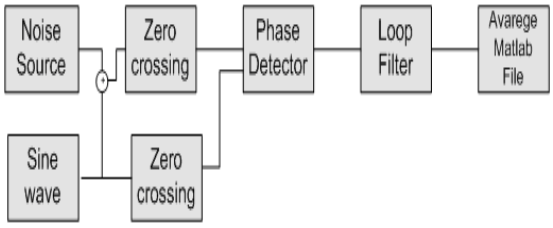

Figure 3. Setup for jitter generation and measurement

The filtering operation of the error voltage (coming out from the phase detector) is performed by a loop filter. The output of the phase detector consists of a dc component superimposed with an ac component. The ac part is undesirable as an input to the VCO; hence a low-pass filter is used to filter out the ac component. The loop filter is one of the most important blocks in determining the performance of the loop. A loop filter introduces poles to the PLL transfer function, which in turn modifies the bandwidth of the PLL. Higher-order loop filters have better noise cancellation than lower-order loop filters. Normally a

second-order loop filter is preferred in PLL for critical applications.

The simulation results of the various blocks are illustrated in figures 4, 5, 6 and 7. Figure 4 depicts three different waveforms, the one shown on top is the input signal, the middle one represents the output of the frequency divider and the last waveform is the phase detector output. Figure 5 shows the response of the two loop filters (LPF1 and LPF2) used in the model. Figure 6 and figure 7 represents the output of the first and second loop respectively.

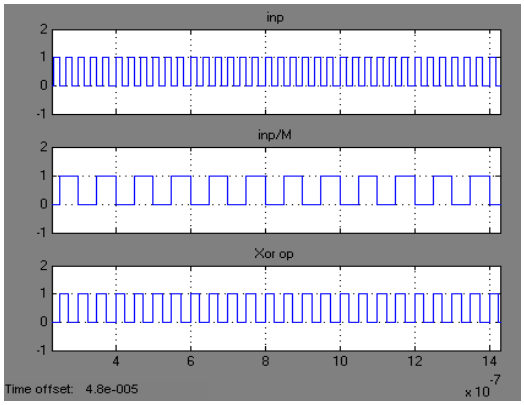

Figure 4. Simulation results for input, frequency divider output and phase detector output

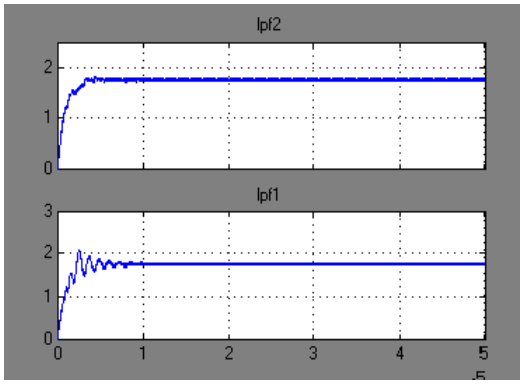

Figure 5. Simulation results for loop filters (LPF1 and LPF2)

Figure 6.

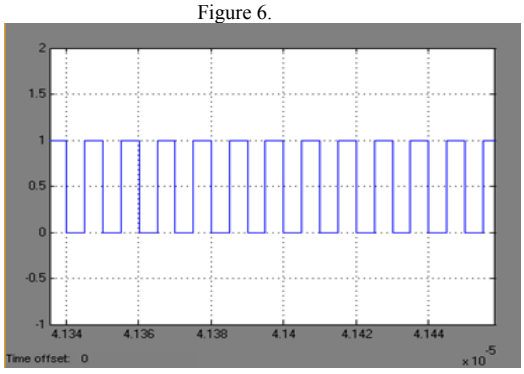

Figure 7. Simulation result for first PLL

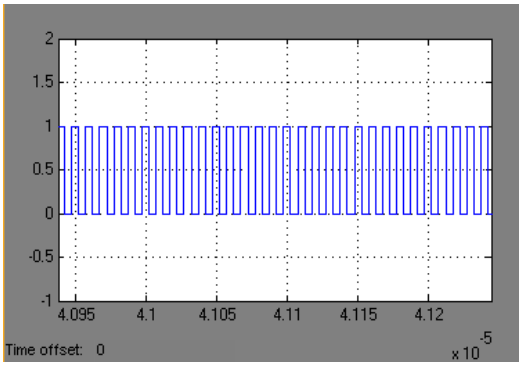

Figure 8. Simulation result for complete system

IV. Conclusion

In this paper we have presented the modeling and simulation of a wideband low jitter frequency synthesizer. MATLAB Simulink was used to model the system which comprises of two PLLs. The first PLL uses a VCXO to eliminate the input jitter and the second one is a wideband PLL. One important advantage of using the proposed system is that it uses only one VCXO for multiple carrier frequencies, while reducing the jitter considerably. The MATLAB Simulink simulation results showed that the jitter could be minimized while working at different carrier frequencies.

V. Acknowledgment

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VI. References

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