Low Jitter and Wide Band frequency Clock Recovery Circuit

Ahmed A. Telba
Department of Electrical Engineering, King Saud University,
P. O. Box-800, Riyadh 11421, Saudi Arabia

Abstract:
Clock recovery circuits are used in data communication systems for the system synchronization. In general a PLL (Phase Locked Loop) circuit is used to extract the clock signal from the input data stream. The recovered clock signal is always jittered and have to be adjusted by using a dejitter circuit. Tracking these errors over an extended period of time determines the system stability. Sources of jitter in PLL circuit itself are due to some ac components at the VCO (Voltage Controlled Oscillator) input which modulate its output frequency. A narrow band PLL may be used after the recovery circuit to minimize the jitter associated with the recovered clock. This second PLL has to be locked at the same frequency as the recovered clock. Other solution is by using a single PLL with Voltage Controlled Crystal Oscillator (VCXO) whose centre frequency is equal to the data bit rate followed by a wide band loop filter. The conversion gain of the VCXO (Hz/V) is very small so a narrow band PLL is resulted without sacrificing the dynamic behaviour. This work presents a proposed system for low jitter clock recovery circuit using two cascaded PLLs which enables to generate several clock frequencies using single VCXO .The proposed described is simulated and verified experimentally. The experimental results confirm the simulation.

Key words:
Low Jitter, Wide Band Frequency Clock

1. Introduction

The heart of any synchronization scheme is the clock recovery circuit. The performance of this circuit is measured by its ability to regenerate a clock signal whose frequency exactly equals the clock frequency of the transmitted data. The Phase-Locked Loop (PLL) is designed to simplify different tasks such as clock recovery, data retiming, frequency translation and clock smoothing applications. The output signal from a given PLL suffers from an associated jitter [1] −[4] especially at high bit rate resulting in bit errors at the receiver side and may cause malfunctioning for all network if this error exceeds a certain threshold level. As the recovered clock signal is always jittered it is needed to be adjusted by using a de-jitter circuit. Jitter is defined as the misalignment of edges in a sequence of data bits from their ideal positions and it can cause data errors. Different types of jitter had been reported such as: Cycle-to-Cycle Jitter [5], period jitter [6] and long term jitter [7] .Fig.1 shows the experimental results of a long term jitter.

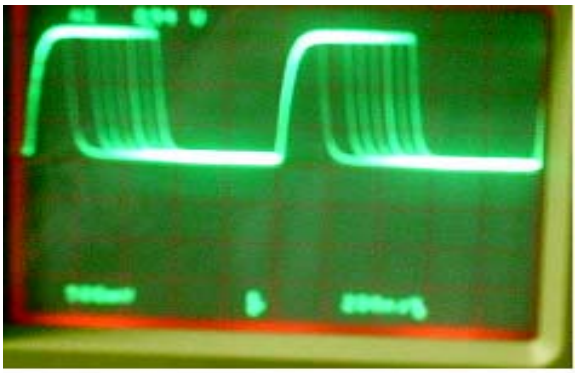

Fig. 1 Typical long term jitter obtained experimentally

2. Jitter Minimization Techniques

Different techniques have been reported for the design and implementation of jitter minimization circuits. This includes modifying the filter design to narrow band the PLL bandwidth and make the phase noise at the VCO input as low as possible [10]. Another technique is by reducing power supply noise [8-9]. Heydari et al proposed a mathematical model for calculating the power supply noise inducing timing jitter in PLLs. This is done by eliminating ground bounce, using additional filter to minimize the effect of the sudden changes of the supply voltage and by having a good grounding to discharge the unexpected charges to ground [11-12]. A technique proposed for high frequency is using dual phase frequency detector [13]. This design uses two phase detectors (PD), the first one is a multiplier (PD) and the second is a phase and frequency detector. Using a modified low power consumption charge pump as phase frequency detector [14], proved useful in improving the jitter characteristics of a Phase-Locked Loop (PLL) by blocking the control voltage leakages. Finally, using PLL with Voltage Controlled Crystal Oscillator (VCXO) [15] as the de-jitter PLL circuit shown in Fig.2, helped in generating a stable, low-jitter clock in the recovered signal.

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An example of a de-jitter PLL circuit is shown in Fig. 2. The design objective of this circuit is to generate a stable, low-jitter clock based on either the recovered receive clock or transmit clock input.

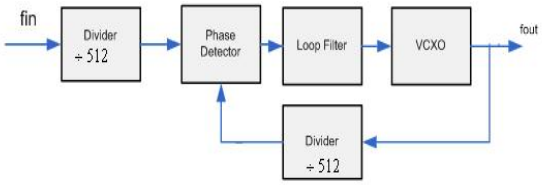

Fig.2 Block Diagram of dejitter circuit

One disadvantage of such technique is that we have to use a VCXO with the same frequency of the input jittered clock. This means that for each carrier system we need to build a VCXO working at the same clock frequency. For example for (E1) telephone carrier system VCXO has to provide exactly 2.048 MHz signal.

3. Dual PLL System

The two main solutions usually used for reducing jitter are those given before [8, 15]. Both techniques work properly and succeeded in reducing the jitter appreciably especially the second one. On the other hand they have one common problem: each of them may be used for only one bit rate (clock frequency). The user has to change the circuit design for each data rate. For example in the second technique we need a VCXO for each bit rate. This work presents a proposed system for low jitter clock recovery circuit with limited jitter. Two cascaded PLL's are used as shown by the block diagram depicted in Fig.3. The recovered clock from the first loop is jitter bounded due to the effect of the VCXO. The second loop is a wide frequency band (wide lock-in range) to cover several standard data rates.

In steady state operation and while the two loops are in locking conditions we may write:

$$\frac{f_{VCXO}}{N_1} = \frac{f_{in}}{M_1} \qquad (1)$$

$$\frac{f_{VCXO}}{N_1 M_2} = \frac{f_{out}}{N_2}$$

and

$$f_{out} = \frac{N_1 N_2}{M_1 M_2} f_{in} \qquad (2)$$

and

$$\frac{f_{VCXO}}{N_1 M_2} = \frac{f_{out}}{N_2} \qquad (3)$$

Combining the above two equations results in

$$f_{out} = \frac{N_1 N_2}{M_1 M_2} f_{in} \qquad (4)$$

The above equation shows that the output frequency f_{out} may be programmed through selecting (N_1, N_2, M_1 and M_2) to be equal to f_{in} independent of f_{VCXO} when $N_1 N_2 = M_1 M_2$. This means that we can generate several clock frequencies using single VCXO .The system described by Fig. 3 is tested by simulation and experimentally. The experimental results confirm the simulation.

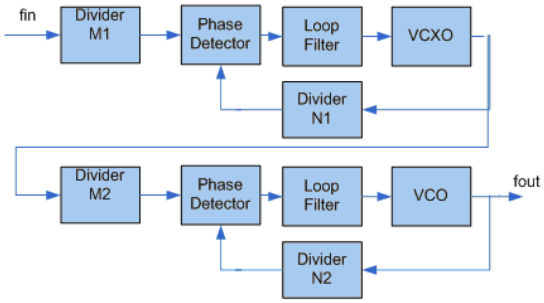

Fig.3 Dual loop PLL clock recovery circuit

4. Simulation and Experimental results

4.1 System structure

The experimental work done using two phase locked loop the first PLL is built using TRU 050 IC chip, from Vectron Semiconductor devices, Inc. It is used as a low jitter clock recovery circuit. The Basic building block of TRU-50 (VCXO_PLL-1) is shown in Fig.4.

The second PLL uses wide range Voltage Control Oscillator and is built around the 74HC4046 integrated circuit that contains all parts necessary to make a PLL except for the loop filter components. The programmable frequency dividers needed to complete the dual loop structure are built using the FPGA prototype board type (SPARTAN_XC10TM^{TM}).

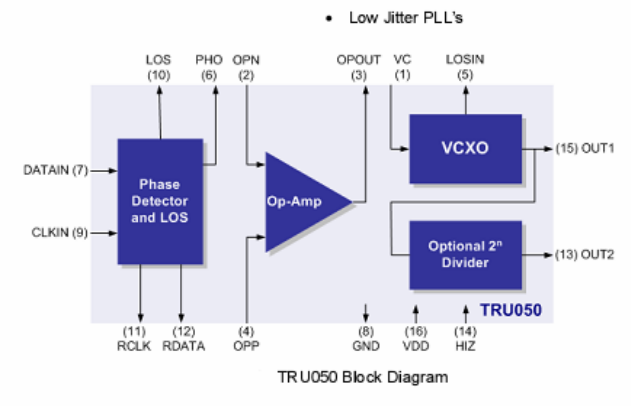

Fig.4 Basic building block of TRU-50 (VCXO)

4.2 Simulation results

For different values of N, we chose N=130,150,170,193 as shown in fig. 5 and 6, the RMS jitter was measured at the output from the first and second loops respectively. The relationships between the RMS jitter and noise power are plotted for different values of N for both outputs and is shown in fig.5 and fig.6 respectively. We can notice that the final output jitter is almost constant irrespective of the input phase noise.

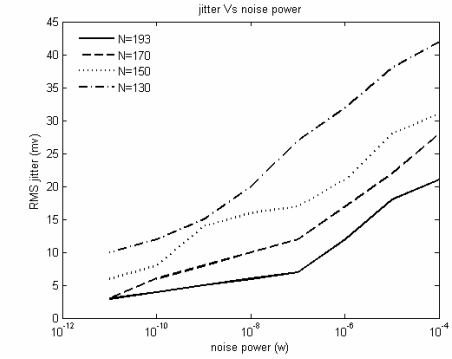

Fig. 5 Jitter at PLL-1 output

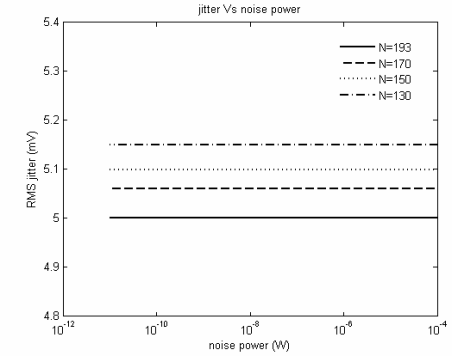

Fig. 6 Jitter at PLL-2 output

4.3 Experimental results

The dual loop system described above was built and tested using Lecroy Oscilloscope "Wave Runner" model 6100 "1GHz Sampling Oscilloscope". The JTA2 software package for LeCroy Oscilloscopes provides advanced jitter and timing analysis capabilities. It uses LeCroy's long memory and zoom architecture to capture and precisely measure thousands of cycles of timing information and then present the results with three different views. By applying a high jittered signal to the system and measuring the output jitter at frequency 1.544 MHz (T1 Carrier), we can deduce the jitter behaviour of the system .The output from the oscilloscope is as shown in Fig.7, where the upper part represents the carrier frequency. The middle portion of the figure shows the Jitter track. The lower portion is the Jitter histogram. The Jitter statistics were taken mainly as cycle to cycle jitter, RMS jitter and accumulated jitter. The TIE has also been measured. It is clear from the figure that the value of the jitter was reduced dramatically from 5.6 ns in input to 37.5 ps in output. The test is repeated for different carrier frequencies and the output RMS is plotted versus the carrier frequency in fig.8.

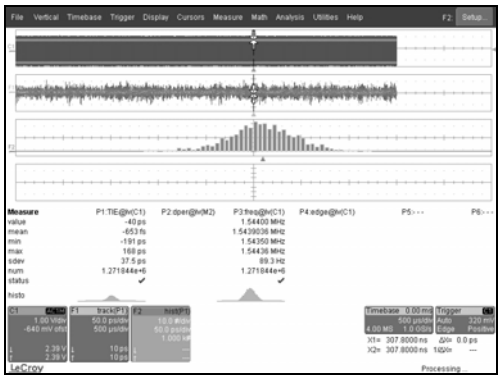

Fig.7 Jitter measurements of T1carrier frequency

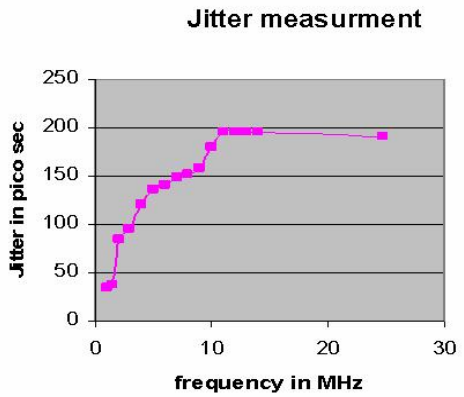

Fig.8 Output Jitter for different carrier frequencies

5. Conclusions

Jitter is almost non useful noise that exists in both digital and analogue signals. Most telephone carriers nowadays use digital signals, and such carriers are meeting different standards (European, American and Japanese). This work presents a proposed system for low jitter clock recovery circuit with limited jitter. Two cascaded PLL's are used where, the recovered clock from the first loop is jitter bounded due to the effect of the VCXO. The second loop is a wide frequency band (wide Lock-in range) to cover several standard data rates. Simulation and experimental results shows that the jitter behaviour is almost directly proportional to the carrier frequencies from 1.54 MHz up to almost 10MHz, and then it remains almost constant for values of frequency beyond 10 MHz up to 24.77 MHz. The experimental results confirm the simulation results and proves the validity of the proposed system in increasing the operating frequency range of a given low jitter circuit.

Acknowledgment

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Biography:

Dr. Ahmed Telba received his PhD from School of Engineering, Design and Technology, University of Bradford UK Electronics and Telecommunications. Currently he is a postdoctoral research assistant with the Electronics and Communications, collage of Engineering, King Saud University Saudi Arabia. His research interests include analogue circuit design, phase locked loop, jitter in digital telecommunication networks, FPGA and VLSI Design.