Static Performance Analysis of Low Power SRAM

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Summary
Low power SRAMs are essential in embedded systems as they are preferred as on chip memories. This paper examines the read stability, write ability and leakage power of various dual-Vt configurations, of an asymmetric SRAM cell (Pass cell) in an array considering the process-induced intra-die threshold voltage variations using N-curve metrics. The effects of process induced Vt variations in 22 different dual-Vt cell combinations are evaluated and compared using Monte Carlo simulations. The comparisons are made with the help of power noise margins and leakage power. The variances and percentage variances from the mean of margins for all combinations are estimated and compared. Comparisons are also made based on four different yield values of the metrics. Thus given a range of a metric and the yield value one can choose the type of configuration of Pass cell. The results help in process variation tolerant design of Pass cell. In addition to this sub threshold operation of C0 configuration of Pass cell is examined under various conditions.

Key words:
SRAM, read stability, write ability leakage variation.

1. Introduction

With the scaling down of CMOS feature size into nanometer regime, the effect of leakage power on the circuits, especially memory is increasing. Therefore SRAM design for low power and low leakage is the main concern in memory design. In asymmetric SRAM cell (Pass Cell) an NMOS pass transistor is inserted between the right storage node and the gate of PDN1 when compared to the 6T SRAM cell, to decouple the storage node from the gate of the pull-down transistor. This reduces the gate leakage current by reducing the voltage on the gate of the leakage transistor PDN1 assuming the cell is storing "0" [6].It has been found that dual threshold voltage assignment method is one of the solutions available to reduce sub threshold leakage power, without any area overhead. However this method is also prone for process induced transistor parameter variations. Analysis of SRAM cell under process variations has been carried out earlier in [1, 11, 12 and 15]. The need for statistical method of design was stressed in [11] and [13] considering the effects of process variations. Also, deterministic and statistical optimization of the standby leakage power of an SRAM cell has been provided [13]. The optimization is based on an algorithm using constraints and dual-Vt strategy. Ref. [7] compares cell stability, noise margin, performance and power of different dual Vt design choices for large on-chip cache with single ended, full swing sensing in a 0.13um technology. In [8] various dual Vt configurations of an SRAM cell considering inter-die Vt variations have been studied. The authors in [9] discuss dual Vt SRAM array design considering inter die variations in Vt. The scaling of MOSFET dimensions, introduces microscopic variations in number and location of dopant atoms in the channel region of the device. This induces increasingly limiting electrical deviations in device characteristics [5]. Intrinsic fluctuations are independent of transistors location on a chip. The threshold mismatch between neighboring cell transistors due to intrinsic fluctuations typically contributes to larger reductions in static noise margins than the threshold voltage mismatch due to macroscopic manufacturing related variations in scaled CMOS SRAM cells [17].

In this paper, the authors consider intra-die random Vt variations and their influence on the read stability, write ability and leakage power of different configurations of a Pass Cell that is part of an array and compares them. Each of the 22 different dual-Vt configurations is evaluated based on the statistical parameters like mean, standard deviation, average deviation of N-curve metrics like static voltage noise margin (SVNM), static current noise margin (SINM),write-trip voltage(WTV) and write-trip current (WTI) in both the cases using Monte Carlo simulations. We have neglected behavior wise repetitive configurations. Section 2 briefly describes the N-curve metrics. Section 3 discusses various dual Vt configurations. Section 4 and 5 compares configurations based on N-curve power metrics and variances respectively. Section 6 is a brief report of leakage power dissipation of the configurations. Section 7 compares them based on confidence levels. Section 8 gives a report of sub threshold operation of Pass cell.

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2. N-Curve Metrics

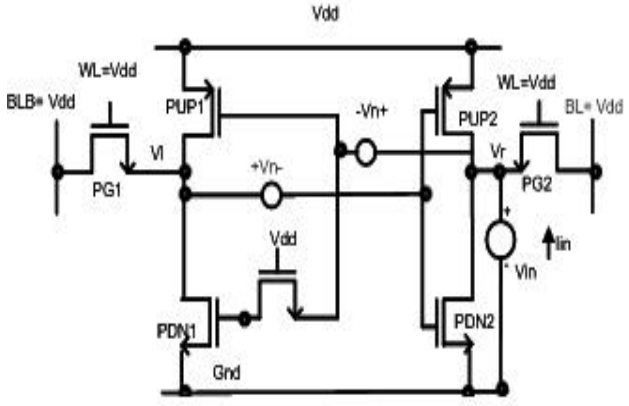

Fig. 1(a). Experimental set up to measure n-curve metrics of a Pass cell

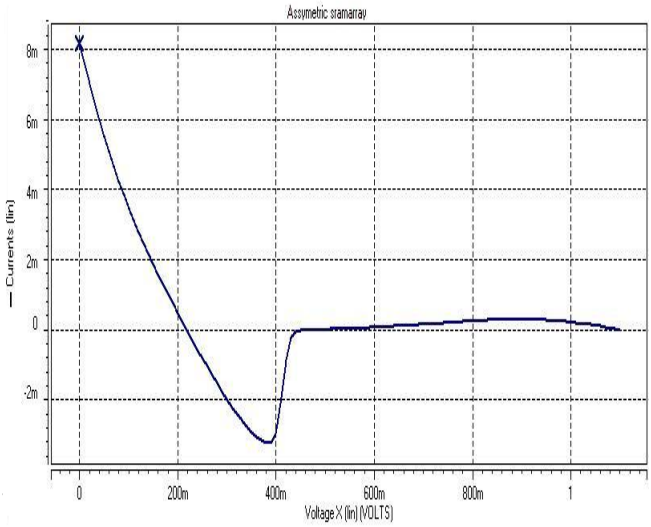

Fig. 1(b) N-curve of C1 Pass cell

As N-curve provides information to find both read stability as well as write ability we have considered this method. The experimental set up used to measure N-curve metrics is shown in the Fig. 1(a).The voltage level of voltage source Vin is varied linearly and the output current –Iin is noted and plotted to obtain the required N-curve.

2.1 Static Voltage Noise Margin (SVNM)

Static voltage noise margin is the voltage differences between first two zero crossing points in Fig. 1(b). It indicates the maximum tolerable DC noise voltage at the input of the inverter of the SRAM cell before its content changes [1].

2.2 Static Current Noise margin (SINM)

Static current noise margin is defined as the maximum value of DC current that can be injected into the SRAM cell before its content changes [1]. It is given by the peak value of Iin during read operation that is between the first and second zero crossing points in Fig. 1(b).

2.3 Write Trip Voltage (WTV)

The difference between the voltages at the second and the last zero crossing points in Fig. 1(b). is the write-trip voltage (WTV) that is the voltage needed to flip the internal node ”1” of the cell with both the bit lines clamped at Vdd [1].

2.4 Write –Trip current (WTI)

It is the amount of current needed to write the cell when both bit lines are clamped at supply voltage equal to Vdd [1].The peak value of Iin after the second zero crossing of N-curve gives WTI.

2.5 Static Power Noise Margin (SPNM)

It indicates the maximum tolerable DC noise power at the input of the inverter of the SRAM cell before its content changes [2].It is given by the product of SVNM and SINM.

2.6 Write Trip Power

It is the amount of power needed to write the cell when both the bit lines are clamped at supply voltage equal to Vdd [2].It is given by the product of WTV and WTI.

Table 1: Dual Vt allotment

Configuration	***High Vt MOSFETs***	***MOSFETs***
C0B	None	All
C1B	PUP1,PUP2, P DN1,PDN2, PG1,PG2	P
C2B	PUP1,PUP2,PG1,PG2,	PDN1,PDN2, P
C3B	PDN1,PDN2,PG1,PG2	PUP1,PUP2, P
C4B	PUP1,PUP2,P DN1,PDN2	PG1,PG2,P
C5B	PG1,PG2,	PUP1,PUP2,P DN1,PDN2, P
C6B	PUP1,PUP2	PDN1,PDN2,P G1,PG2,P
C7B	PDN1,PDN2	PUP1,PUP2,P G1,PG2,P
C8B	PDN2, PUP1, PG1	PDN1, PUP2, PG2, P
C9B	PUP1,PUP2, P DN1,PDN2 PG1	PG2, P
C10B	PUP1, PDN1, PUP2, PG1	PDN2,PG2, P

Configuration	*High Vt MOSFETs*	*Low Vt MOSFETs*
C0	P	PUP1,PUP2,PDN 1,PDN2 PG1,PG2
C1	All	None
C2	PUP1,PUP2,PG1, PG2,P	PDN1,PDN2
C3	PDN1,PDN2,PG1 ,PG2,P	PUP1,PUP2
C4	PUP1,PUP2,P DN1,PDN2, ,P	PG1,PG2,
C5	PG1,PG2,P	PUP1,PUP2,PDN 1,PDN2
C6	PUP1,PUP2,P	PDN1,PDN2,PG1 ,PG2
C7	PDN1,PDN2,P	PUP1,PUP2,PG1, PG2
C8	PDN2, PUP1, PG1,P	PDN1, PUP2, PG2
C9	PUP1,PUP2, P DN1,PDN2 PG1,P	PG2
C10	PUP1, PDN1, PUP2, PG1,P	PDN2,PG2,

3. Dual Vt configurations

Table 1 shows various combinations of dual Vt assignment that we have considered for Pass Cell that belongs to an array of hundred cells as shown in Fig.1 (a). Dual Vt technique is used to reduce the sub-threshold leakage power without any area overhead. It is known that there are two sub-threshold leakage paths in a 6T SRAM cell, one from the power supply to ground (either through PUP1 to PDN1 or PUP2 toPDN2) and the other path is through bit line (BL or BLB) to ground through the access transistors PG1 or PG2. Although leakage power is due to sub-threshold current, it can be reduced to a minimum by employing high Vt transistors in these paths. In practice however it is not done as it leads to high access time.

The cell has cell ratio and pull up ratios to be 1.5. Predictive technology models (PTM) at nominal process corner in 65nm technology were considered. The low threshold voltages of 0.516V and -0.471V and high threshold voltages of 0.652Vand -0.589V were chosen. As threshold voltage variations capture some of the other sources of process-induced variations the threshold voltage variations of 3σ at 20% from the mean μ was considered. We also assume the variations in Vt of any of the transistors to follow Gaussian distribution. Monte Carlo simulations were used to get different combinations of uncorrelated threshold voltage Vt values for the analysis.

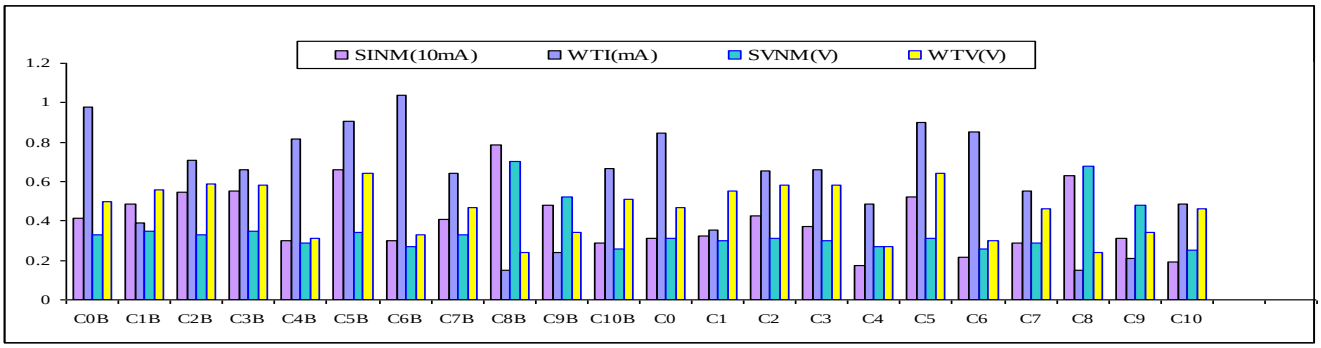

Fig. 2 (a) Read and write N-curve metrics for all 22 configurations

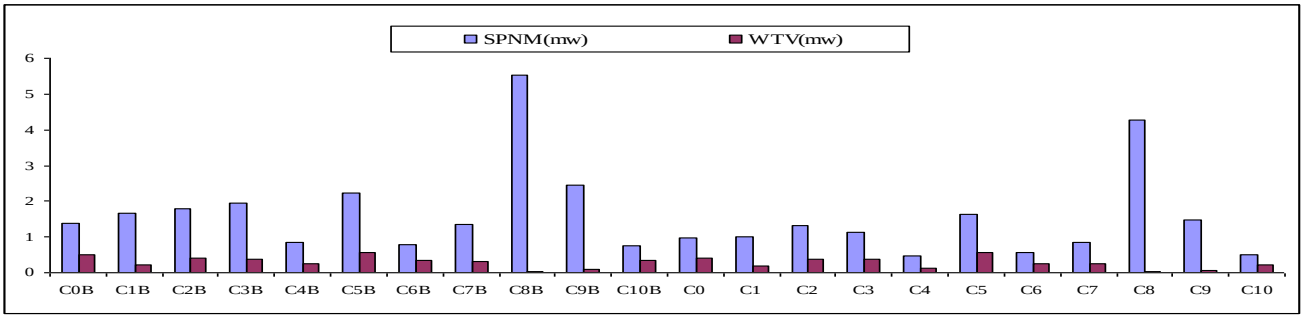

Fig. 2 (b) Read and write N-curve power metrics for all 22 configurations

4. Comparison based on power metrics

For better read stability, the product of mean of SVNM and mean of SINM called Static Power Noise Margin should be larger. For better write ability, the product of mean of WTV and mean of WTI called Write Trip Power must be smaller. Fig. 2(a) provides the plot of read and write margins for all configurations from which power margins can be estimated. Fig. 2(b) shows the power margins for read stability and write ability for all the configurations. C8B has the highest value of read stability of SPNM equal to 5.543mw and C8 is next with 4.281mw.The configuration C8B and C8 have lowest values for WTP equal to 0.0363 mw and thus it can be easily written compared to others.

5. Comparison based on variances

Table II shows variances of all n curve metrics due to threshold voltage variation within a die. The configuration C3 has highest variance of 30.45μA and C10B has least variance of 1.81 μA followed closely by C4B with 1.84 μA for SINM. The configuration C6B has highest variance of 0.705 μA whereas C6 has least variance of 1.074pA for WTI. In case of static voltage noise margin C6B has highest variance of 0.061V followed by C6 with 0.0607V. The configuration C8 has least variance of 0.0104V.C10 has highest variance of 0.08259V and C3B has lowest variance of 0.00635V for write trip voltage.

Table2: Variances and Percentage Variances

	SINM		***WTI***		***SVNM***		***WTV***	
	σ^2 μA	$(\sigma^2/\mu)100$	σ^2 nA	$(\sigma^2/\mu)100$	σ^2 mV	$(\sigma^2/\mu)100$	σ^2 mV	$(\sigma^2/\mu)100$
C0B	2.99	0.071864	450.47	0.04594	45.44	13.62698	57.93	11.65354
C1B	2.52	0.051731	64.27	0.016586	27.99	8.111885	29.04	5.189282
C2B	3.68	0.067556	345.96	0.048853	35.25	10.75465	54.21	9.264761
C3B	2.60	0.047196	43.51	0.006583	12.92	3.662705	6.36	1.098481
C4B	1.84	0.061456	300.81	0.036955	52.55	18.38364	35.67	11.55234
C5B	3.92	0.059311	140.58	0.015516	17.51	5.215782	15.37	2.405737
C6B	2.33	0.078225	705.26	0.068029	61.31	23.12274	52.14	15.637
C7B	2.61	0.064016	166.89	0.025907	34.64	10.47783	34.12	7.236985
C8B	2.36	0.02997	9.66	0.006507	11.80	1.673813	11.30	4.623234
C9B	2.40	0.050281	35.29	0.014838	39.74	7.693487	24.54	7.134195
C10B	1.81	0.062291	170.62	0.025615	40.81	15.80621	70.90	13.94993
C0	3.82	0.122406	693.48	0.082254	44.22	14.1417	61.41	12.96266
C1	3.25	0.099553	100.40	0.02835	26.29	8.649972	29.61	5.365016
C2	4.52	0.106656	447.19	0.068674	33.77	10.807	55.06	9.552197
C3	30.45	0.812773	43.62	0.006609	10.59	3.513127	6.41	1.107937
C4	2.92	0.166391	667.22	0.137244	56.83	21.10055	55.02	20.22601
C5	4.30	0.082689	146.21	0.016211	15.54	4.97294	15.45	2.420934
C6	3.05	0.142703	0.00	1.26E-07	60.78	23.21732	68.81	22.87418
C7	3.40	0.117441	301.13	0.054473	35.44	12.04181	35.85	7.86665
C8	2.26	0.035877	9.66	0.006507	10.49	1.541817	11.30	4.623223
C9	2.98	0.095794	65.48	0.031535	41.21	8.647964	28.34	8.344736
C10	8.43	0.433695	335.02	0.069178	40.23	16.0335	82.57	17.94856

6. Comparison based on leakage power

The threshold voltage of a MOSFET affects the leakage current that flows through the device. Low Vt MOSFET produces more leakage current than high Vt MOSFET. Fig. 3 shows the mean value of the leakage power for all 22 configurations. Hence we can observe variation in leakage power for various configurations and their changes due to variation in Vt. C0 has maximum leakage with mean leakage power over a specified time of 6.9ns equal to 6.8117μwatts. C9B produces least leakage power mean of which is equal to 0.199μwatts over the same duration.

7. Comparison based on confidence level

Confidence is a range of population means. We considered the highest value of the mean for the analysis for static voltage and current noise margins. For voltage and current noise margins we have considered the confidence levels, 0.9, 0.8, 0.7, and 0.6 as larger values are preferred. The confidence levels 0.1, 0.2, 0.3, 0.4 were considered for both the write trip voltage as well as write trip current margins as least values are preferred for better write ability. We considered the lowest value of the mean for analysis of write trip margins. The confidence range of ±26mv is obtained for SVNM at confidence level 0.9 for C1 configuration means that for any population mean μ0 in this interval μ±26mv the probability of obtaining a sample mean further from μ0 than μ is more than 0.1. Likewise for any population mean μ0 outside this interval, the probability of obtaining a sample mean further from μ0 than μ is less than 0.1. Similar analysis can be done for other metrics. The configuration C0B provides maximum ange of ±41.77μA for WTI at confidence interval 0.4 and C6B has minimum range of ±0.0123μA at confidence level 0.1. Fig. 4(a) and Fig. 4 (b) show intervals (μ-confidence range) for SINM and SVNM respectively. Fig. 4(c) and Fig. 4 (d) show intervals (μ-confidence range) for WTI and WTV respectively.

8. Analysis of N-curve metrics of pass cell for sub threshold operation

In pursuit of low power Pass cell the analysis was carried out for a bigger Pass cell in 65nm technology by using Predictive Technology Models derived in [18], for C0 configuration in sub threshold region assuming threshold voltage of devices to be process variation independent.

8.1 Power supply voltage

The ratio of SVNM to VDD increases with VDD and drops down to 0.325 at VDD equal to 0.42V.The ratio of WTV to VDD increases gradually from 0.5793 to 0.621 as we increase VDD from 0.3V to 0.42V.The static noise margin current SINM increases by 13 times with increase in VDD and the WTI increases by 31 times. The increase is due to the exponential dependence of sub threshold current on VDD. The noise tolerance improves with VDD along with write ability as the value of on current increases. Fig. 5(a) and Fig.5 (b) show the variations of current voltage metrics with respect to supply voltage VDD respectively.

8.2 Temperature

The increase of temperature from -40^{o}C to 100^{o}C increases SINM by 10 times and further increase in temperature gradually reduces the SINM. Thus above 100 ^{o}C the noise tolerance of the circuit reduces. The WTI remains almost constant with only 0.6μA change in the value over 180^{o}C raise in the temperature. The value of WTV almost remains constant with rise in temperature but the curve of SVNM shows noise intolerance above 100^{o}C as the threshold voltage of the devices gets affected more. The write ability is not affected by the changes in temperature. Fig. 5(c) and Fig. 5(d) show the variations of current and voltage metrics with respect to supply temperature respectively.

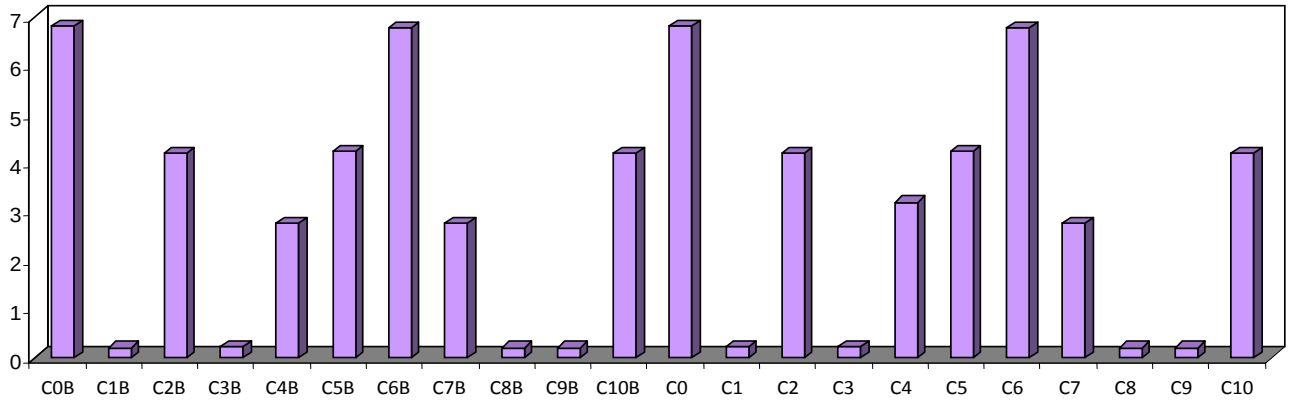

Fig. 3 Leakage power for all 22 configurations

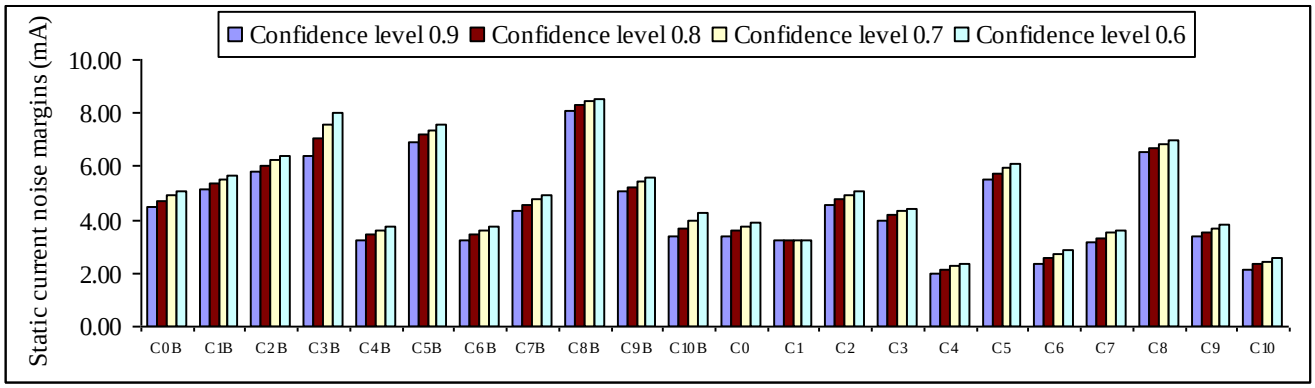

Fig. 4. (a). Confidence intervals of static current noise Margin for all 22 configurations

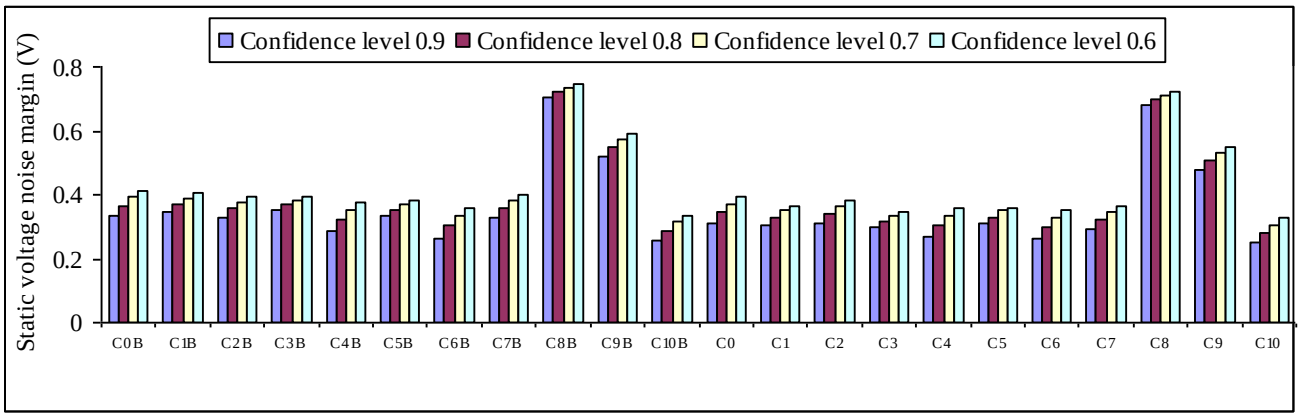

Fig. 4. (b). Confidence intervals of static voltage noise margin for all 22 configurations

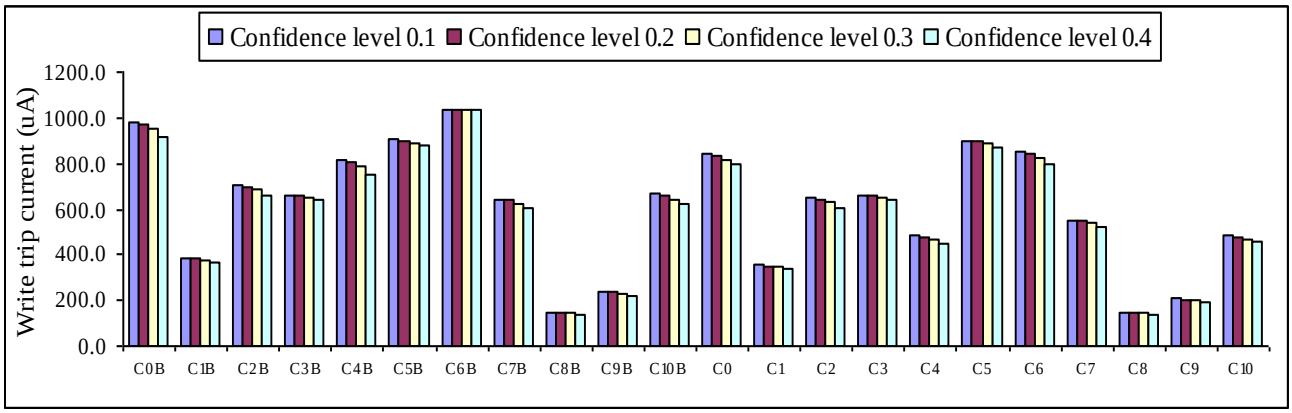

Fig. 4. (c). Confidence intervals of write trip current for all 22 configurations

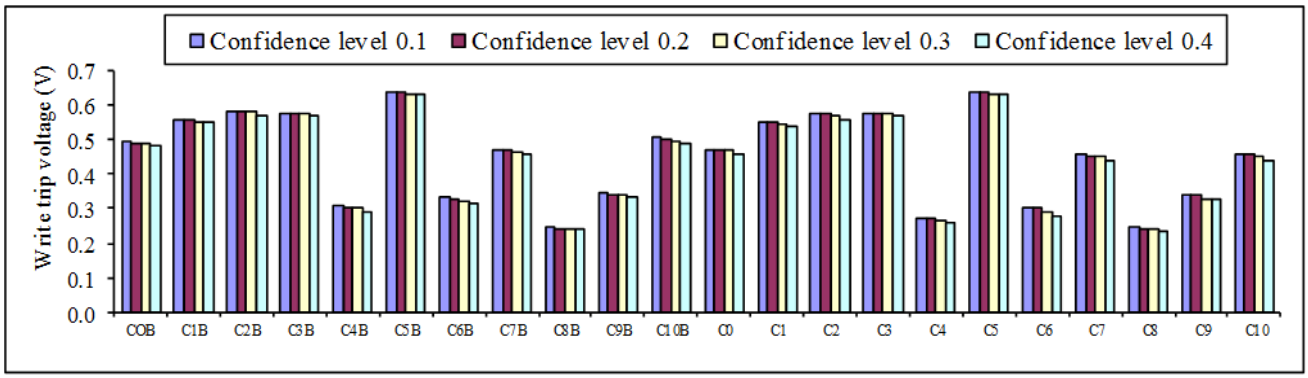

Fig. 4. (d). Confidence intervals of write trip voltage for all 22 configurations

8.3 Oxide thickness

The effect of gate oxide is studied by considering high Vt devices. The higher the gate oxide, the lower is the SINM value. The SINM decreases by 4.86 times for a change in t_{OX} from 2nm to 3 nm. The change in WTI is gradual. WTI decreases by 5 times for a change in 1nm change in thickness. The SVNM decreases at a rate of 0.02V per 1nm variation in gate oxide thickness. WTV increases at a rate of 0.004V per nm change in gate oxide thickness. The noise withstanding capability decreases with increase in gate oxide thickness although write ability is not much affected. This is due to the fact that the potential needed to change the surface potential and overcome the depletion layer charge decreases. Fig. 5(e) and Fig. 5(f) show the variations of current and voltage metrics with respect to gate oxide thickness respectively.

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Conclusion

In this paper we studied various dual Vt configurations of a Pass cell considering intra-die Vt variations due to process variations. Due to process variations, the read stability write ability and leakage power of each of the configurations is examined based on the N-curve power metrics. Monte Carlo simulations for 65nm PTM technology was done to study the effect of intra die variations on Vt due to process variations using HSPICE. Comparisons based on N-curve power metrics, variances of metrics, leakage power have been done. Also comparisons of different cell configurations, based on evaluating the mean values of various metrics at points corresponding to desired confidence level have been carried out. The configurations C8 and C8B show better performance with respect to write ability, read stability, leakage and variances of metrics when compared to other configurations. The results obtained help in the statistical design of Pass cell with constraints, using dual-Vt technique to reduce the leakage power. In sub threshold region of operation the noise tolerance improves with VDD along with write ability. The noise tolerance decreases above 100 ^{o} C although the write ability is not much affected by the changes in temperature. The noise withstanding capability decreases with increase in gate oxide thickness although write ability is not much affected.

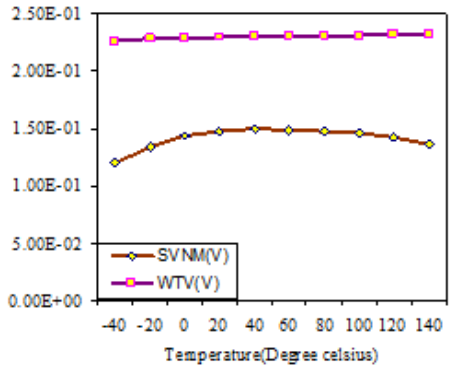

Fig. 5 (d). Variation of voltage metrics with temperature

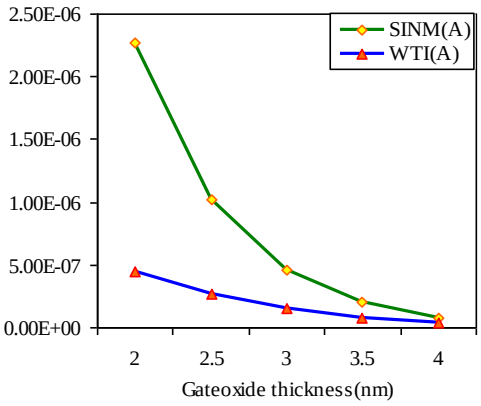

Fig. 5(e). Variation of current metrics with gate oxide thickness

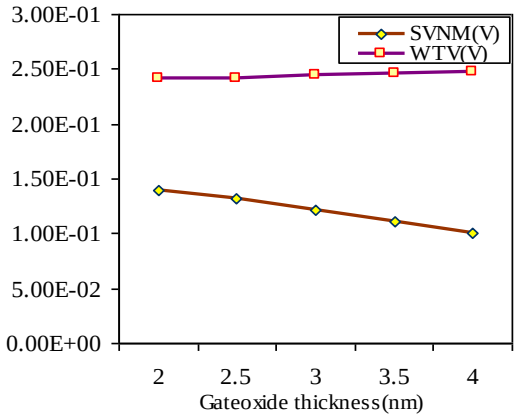

Fig. 5(f) Variation of voltage metrics with gate oxide thickness

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