Quaternary Sequential Circuits

Vasundara Patel K S[1], K S Gurumurthy[2]
[1]Department of ECE,BMSCE,Bangalore,

[2]Department of E & C, UVCE, Bangalore,

Abstract
Application of multiple-valued logic(MVL) in the design of digital devices opens additional opportunities. D flip-flop is a basic sequential circuit in any logic. A 4-bit counter using Multiple-valued D flip-flops is presented in this paper. D flip-flop is built by 3 input NMIN gates and has both preset and clear inputs. Quaternary multiplexer and D flip-flops are used to design the quaternary counter. The circuits being studied are optimized for power and delay at 0.18-µm CMOS process technology. The new D flip-flop designed here shows 64.33% improvement in dynamic power dissipation when compared to DLC based flip-flop and Q-IDEN D flip-flop. The proposed Counter circuit also exhibits less dynamic power dissipation.

Key words
Multi-valued logic, Quaternary logic, multiple-valued sequential circuits, MVL counter

1. Introduction

MULTIPLE-VALUED Logic (MVL) has been the subject of research for many years [1, 2, 3]. Besides reduction in chip area, it could become the future logic for high speed image processing [4] and speech recognition [5] applications. Until late 1960s, theoretical nature of computing techniques had been established using binary valued digital systems. Even today, the latest computing systems are designed and developed using binary logic only. Alternatively, people have also been working on the possibilities of using multi-valued logic for developing faster computing techniques. It is but natural to assume the 10-valued logic (decimal) systems as an alternative to binary systems, since decimal machines would gain rapid acceptance if they could be produced reliably and inexpensively. Unfortunately, the present state of technology is more amenable to implementing lower radix systems. In real life situations, there is no clear cut binary yes/no requirement; situations such as yes/no not defined, or up/down/stop, or left/right/straight ahead bound in the real world scenario. This amounts to saying that multi valued logical systems, for instance, a three-valued (radix 3) digital realization would be more appropriate than binary [6]. The significance of using higher radix is the possibility to reduce the number of interconnections per system or subsystem. As the value of radix increases, the information carrying capacity of each connection also increases [7].

In this paper, we explore the possibilities of realizing sequential circuits using multi valued logic or more precisely using what we call as quaternary logic.

In view of describing the notion of multi-valued logic (MVL), we first consider the primary logic levels 0 and 1 and the associated Boolean logic in our discussion [2]. In 1938, Shannon proved that a two-valued Boolean algebra (whose members are most commonly denoted by 0 and 1, or false and true) can describe the operation of two-valued electrical switching circuits. In modern times, Boolean algebra and Boolean functions are indispensable in the design of computer chips and integrated circuits [8]. Boolean algebra has recursive structures apparent in the Hasse diagrams shown in figure 1, which illustrate Boolean algebra of orders n = 2, 3, 4 and 5. These figures illustrate the partition between left and right halves of the lattice, each of which is the Boolean algebra on (n-1) elements. The complexity of Hasse diagrams increases as the order increases, which, of course, could be easily solved by implementing these logics into a semiconductor chip.

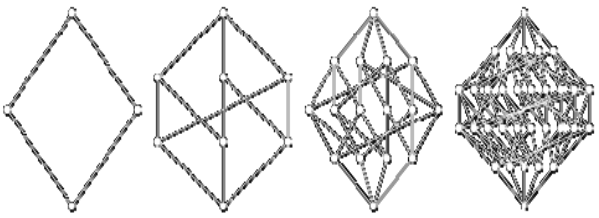

Figure 1: Hasse diagrams illustrating Boolean algebra

The binary logic levels can also be represented using Venn diagrams which originated in Venn (1894). Figure 2(a) represents a two variable example and 2(b) represents a three variable example which are self explanatory [9]. A three variable Boolean algebra yields 256 Linear Boolean Functions (LBF). In general, an n-variable Boolean algebra deals with Linear Boolean Functions.

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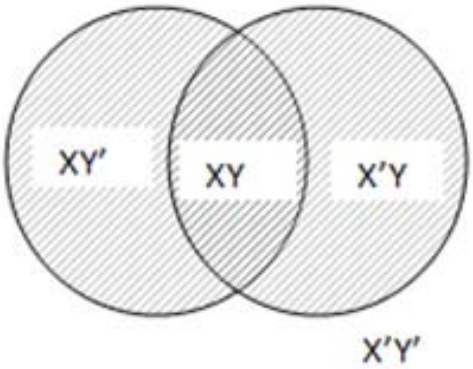


Figure 2 (a): Venn diagrams representing for a two variable map, $n = 2$.

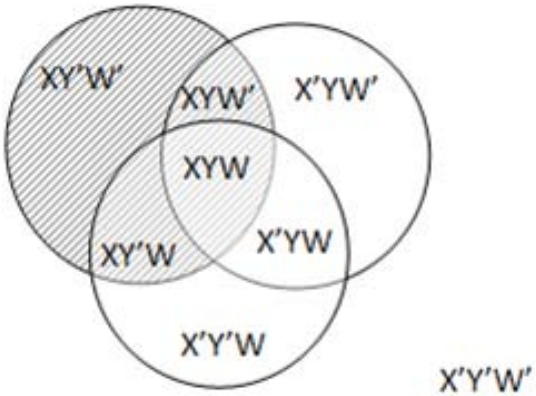


Figure 2 (b): Venn diagrams representing for a two variable map, $n=3$

Model theory is basically understood as a union of algebra and logic. Boolean algebra is a model of Boolean logic. Any algebraic system, for that matter, is a model of classical logic that works on truth values T and F. However, in a real life situation, one would admit to the fact that decision made on observations do not precisely comply with 'True', 'False' values. On the other hand, there is always an uncertainty in deciding these values, rather, one would come across situations wherein one has to accept multiple decision values like to what extent the decision may be true and to what extent the decision may be false [8]. This argument is sufficient enough to support for the truth value model shown in figure 3.

2. Multi-valued Logic

Traditional calculi are only two valued for any proposition. Multi-valued logics are logical calculi in which there are more than two truth values. Multi-valued system has several important advantages over existing binary system. Expanding the existing logic levels to ternary and penta levels, higher processing rates could be achieved in various applications like memory management, communication throughput and domain

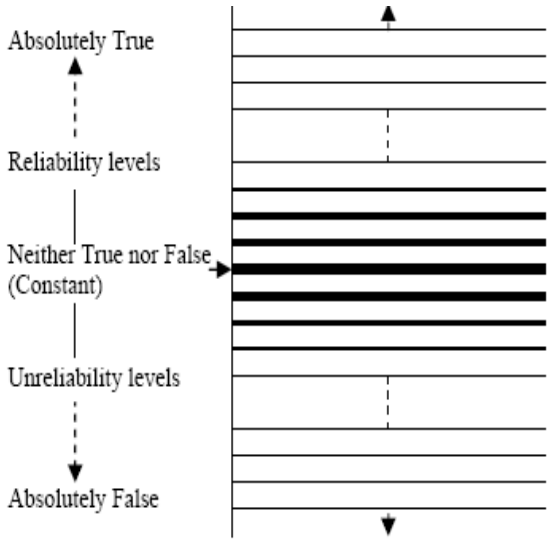


Figure 3: Truth values Reliability-Unreliability model.

Specific computation. An evident advantage of a ternary representation over binary is economy of digits. To represent a number in binary system, one needs 58% more digits than that of ternary [7]. For example, to represent a 15-digit decimal number, one requires 34 ternary digits instead of 54 binary digits. Ternary representation admits sign convention also. The most significant advantage is that there is reduction in the interconnection required to implement a logic function. This in turn causes reduction in the chip area while fabricating devices [8].

In addition to the design it is also necessary to assess the cost of manufacturing of these types of multiple valued logic circuits. Let R be the radix, 'd' be the number of digits to express a range of N numbers such that $N = R^d$. Assume that the number and/or cost of the basic hardware components C is proportional to the "digit capacity" R x d, then we have

$$C = k(R \times d) = k\left[R\frac{\log N}{\log R}\right]$$

where k is some constant. Differentiating this cost equation with respect to the radix R and equating to zero gives that R should equal e (2.718) for minimum cost. From this analysis R=3 should be more economical than the binary radix R=2. If we consider that devices or circuits are available which provide two, three, four or more stable digital signals without any increase in individual costs for the higher-valued radices, then in such ideal circumstances total cost C would be proportional to d. Hence,

$$C = kd = k\left\lceil \frac{\log N}{\log R} \right\rceil$$

which is a gradually decreasing total cost C with increasing R [10, 11, 12].

Table 1 shows representation of decimal numbers using ternary symbols. The decimal number D in terms of ternary symbol is given by

$$D = \{T_n 3^n + T_{n-1} 3^{n-1} + \ldots + T_1 3^1 + T_0 3^0\}$$

where T = ternary digit -1, 0, +1
n = significance of the ternary digit,
T_0 = least significant
T_n = most significant.

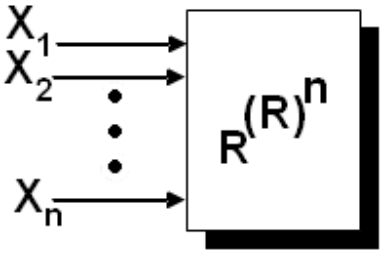
However, the -1, 0, +1 numbering system has a unique advantage that any number can be changed from a positive value to the corresponding negative value by merely changing all -1s to +1s and vice versa, leaving all zeros unchanged [12]. As an example table 2 shows the natural representation of quaternary logic. For a system with n multi-valued inputs X_1 to X_n and one multi-valued output f (x), (Refer to figure 4(a)) , the different number of signal input combinations is R_n and the number of different functions f(x) of the n inputs is R^{R^n}. For example, a ternary system of three variables (Refer to figure 4(b)) has 3^n input combinations and 3^{3^n} possible ternary valued functions.

Table 1: Representation of decimal numbers using ternary symbols.

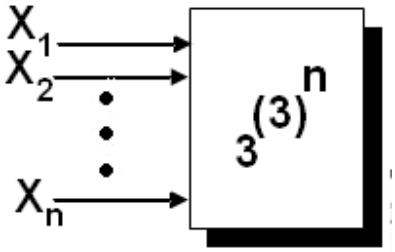
Decimal number D	Ternary notation using the number -1, 0, +1
0	0000
1	0001
2	000-1
3	0010
4	0011
5	01-1-1
6	01-10

Table 2: Natural representations of quaternary numbers.

Quaternary logic representation	Natural Representation
0	00
1	01
2	10
3	11



a) R-Valued system



b) Three-valued (ternary) system.

Figure 4: Multi-valued systems

Organization of the paper is as follows: Discussion regarding previous work is illustrated in section 3. Sequential circuit design is done in section 4. In the same section quaternary D flip-flop and quaternary counters are explained. Results are discussed in section 5. Finally conclusion is given in section 6.

3. Review of related work

3.1. Flip-flops

A family of multiple-valued (MV) electronic memory elements, referred to as flip-flops, was presented in paper [13] by Thurman A Irving along, with a system of MV algebra upon which they are based. These MV flip-flops were compared to binary flip-flops. MV asynchronous set-clear flip-flops and synchronous set-clear, D-type, JK, and modulo N counter flip-flops were presented, their next-state equations were derived, and they were shown to have desirable properties for use in MV sequential circuits. Experimental results and schematic diagrams were presented for a level restoring three-valued logic gate, the clocked set-clear flip-flop, and an example synchronous sequential circuit [13].

The implementation of the multi-valued flip-flop presented in paper [14] by L. Sintonen, was independent of N (number of logic levels).The output of the flip-flop was stable during clock transitions. [14]

By using the theory of clipping voltage-switches, two kinds of master/slave NMOS quaternary flip-flops were

designed by Xia Yinshui [15]. These flip-flops have the capability of two-input presetting and double-rail complementary outputs. It was shown that these flip-flops were effectively suitable to design NMOS quaternary sequential circuits by designing two examples of hexadecimal up counter and decimal up-counter [15].
The implementation and verification of the fundamental flip-flops for the voltage mode multi-valued logic circuits on a conventional CMOS VLSI chip were presented in paper [16]. By Inaba. In verification through HSPICE simulation the proposed flip-flops perform good results such as high noise margins and low power consumption [16].
A new CMOS quaternary D flip-flop was presented employing a multiple valued clock by In Shui Xia in paper [17]. Pspice simulation shows that the proposed flip-flop has correct operation compared to traditional multiple valued flip-flops, The proposed multiple valued CMOS flip-flops was characterized by improved storage capacity, flexible logic structure and reduced power dissipation[17].
A NMAX-TG D flip-flop and a NMIN D flip-flop presented by Sangmi Shim in paper [18] were composed of the components such as NMAX D flip-flops, NMIN D flip-flops and T-gate circuits. In the simulations, sampling frequencies of NMAX-TG D flip-flop and NMIN-TG D flip-flop were measured around 500 MHz and 1 MHz, respectively [18].
Q-IDEN D flip-flop circuit was designed by Sangmi Shim in paper [19] using thermometer code output circuit, EXOR gate, bias inverter, transmission gate, and binary D flip-flop circuit. Using thermometer code output circuit, EXOR gate, and bias inverter multi-valued identity logic circuit was designed and with multi-valued identity logic circuit and binary D flip-flop Q-IDEN D flip-flop was designed [19].
D. Venkat Reddy in Paper [20] was concerned with the formulation of a novel paradigm called (2n+1)-ary logics and their ultimate use in the development of multiple valued logic based processor. Apart from a preliminary introduction to the binary valued logic systems, this paper introduces the notion of Truth values Reliability-Unreliability model and a brief exposition of multiple valued logic in the framework of switching algebra. Finally the paper discusses the simulation results of implementing primarily ternary and penta logic switching functions using traditional binary logic circuits [20].
The D flip- flop circuit was designed by Vasundara Patel K S in paper [21] using Down Literal Circuit, EXOR gate, bias inverter, pass transistor, transmission gate, binary D flip flop. Proposed circuit dissipates less power and uses same fabrication steps as that of conventional CMOS circuits. [21]

3.2 Counters

Tai haur kuo in Paper [22] describes the use of resonant tunneling diodes for multi-valued counters, In order to achieve this implementation, a unique state-dependent current source was used to successively trigger RTD-based counter [22].
J. G. Lomsdalen in Paper [23] introduces a Multiple Valued Counter, based on recharged semi floating gate structures. The counter starts at a sampled voltage, and counts from there, using an input clock signal as an input. Depending on the sampled value and the phase of the input clock signal – the counter can count both up and down. The counting steps can be varied adjusting the input clock amplitude, which in combination with different output resetting values allows a set of different counting radixes. Recharged semi floating structures may suffer from an offset at the output due to mismatch in the inverter structures. This counter minimizes this problem with a build in offset cancellation, which is an advantage for non capacitive readouts [23].

4. Sequential circuit design

4.1 Quaternary D-flip flop

D-flip flop means data flip flop. A quaternary D-flip flop has four stable states, namely 0, 1, 2 and 3.
We have designed a positive edge triggered quaternary D-flip flop. It has a synchronous input ‘Din’ and two asynchronous inputs clear and preset. The term synchronous or asynchronous is with reference to clock. ‘Din’ being synchronous can change the output only at positive edge of clock. It means when a low (0V) to high (3V) transition occurs. Since preset and clear are asynchronous, any change in them affects the output immediately, irrespective of positive edge of clock. Preset and clear are both active low inputs. Hence logic 0 on preset input line causes the output to enter into logic 3 state and logic 0 on clear input line causes the output to enter into logic 0 state.
If both preset and clear are active simultaneously then the output is unpredictable. Hence this condition must be avoided. The truth table and circuit diagram for D-flip flop are as shown in table 3 and figure 5 respectively. This circuit consists of six, three input NMIN gates [24]. The block diagram for D-flip flop is shown in figure 6.
If preset and clear are both logic 3 then din appears at the output at positive edge. If preset = 0 and clear = 3 then output = 3. At this stage flip flop is in set state. If preset = 3 and clear = 0 then the output = 0. Now the flip flop is in clear or reset state.

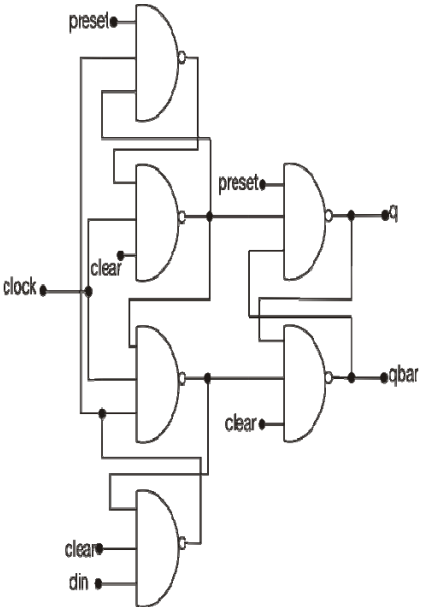


Figure 5: Circuit Diagram of Quaternary D-flip flop

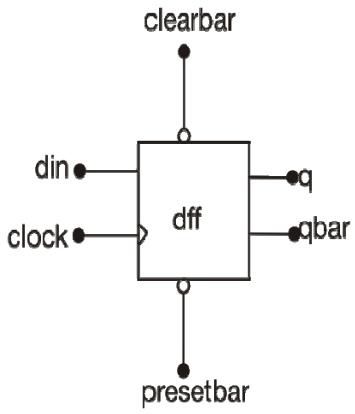


Figure 6: Block Diagram of Quaternary D-flip flop

Table 4: D-flip flop truth table.

Inputs				Outputs	
Preset	Clear	Din	Clock	Q+	Qbar+
0	3	X	X	3	0
3	0	X	X	0	3
0	0	X	X	unpredictable	
3	3	0	↑	0	3
3	3	1	↑	1	2
3	3	2	↑	2	1
3	3	3	↑	3	0

4.2 Two digit synchronous quaternary up-counter

The circuits for producing the least significant digit and most significant digit of the counter output are as shown in figures 7 and 8 respectively. They make use of quaternary multiplexers [24] and D-flip flops. The D-flip flop designed above has been used.

This counter has sixteen states as shown in table 4. Q1 is the most significant digit and Q0 is the least significant digit. The outputs of the flip flops are fed back to the multiplexers [24] to get the next count (next state). Initially the D-flip flops are reset using the clear input to get the initial count (initial state) 00. Once reset, the next count sequences are obtained one after the other at subsequent positive clock edges provided clear and preset are inactive. Counts occur only at positive edge of the clock since the flip flops are positive edge triggered. It must be noted that the counter can be brought to reset state at any instant using the clear input.

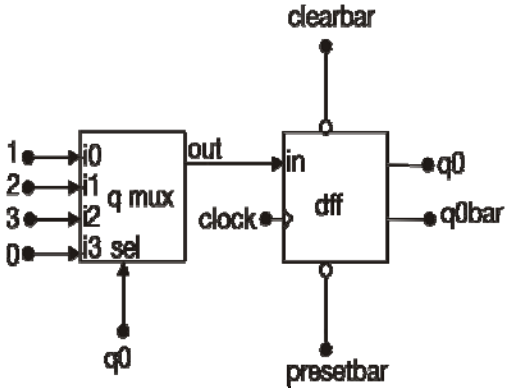


Figure 7: Circuit for generating least significant digit of counter output

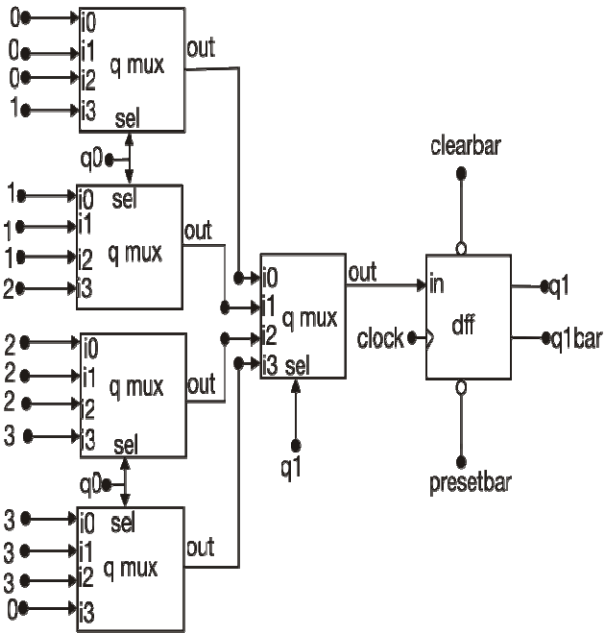


Figure 8: Circuit for generating most significant digit of counter output.

Table 5:.State table of Quaternary Up-counter

Present state		Next state	
Q1	Q0	Q1+	Q0+
0	0	0	1
0	1	0	2
0	2	0	3
0	3	1	0
1	0	1	1
1	1	1	2
1	2	1	3
1	3	2	0
2	0	2	1
2	1	2	2
2	2	2	3
2	3	3	0
3	0	3	1
3	1	3	2
3	2	3	3
3	3	0	0

5. Results and discussion

The simulation results for the quaternary D-flip flop and the quaternary up-counter are shown in figure 9 and 10 respectively. Simulation is carried out using Synopsys Hspice Tool and results are observed on COSMOS SCOPE.

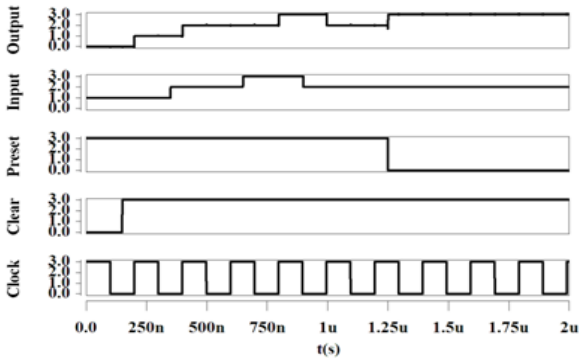


Figure 9: Simulation result of quaternary D-flip flop.

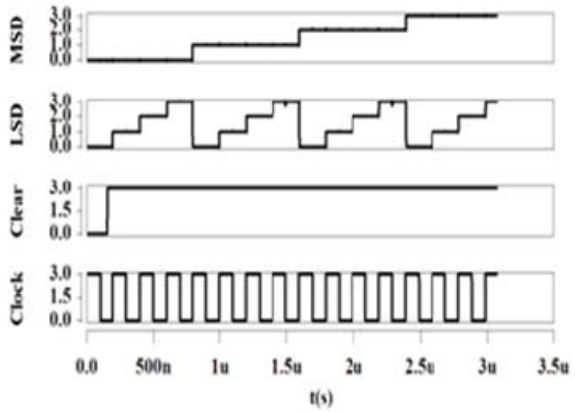


Figure 10: Simulation result of quaternary counter

Table 6: Performance parameters comparison of different D-flip flops

Flip-Flop	Author	Foundry	Max supply voltage	Dynamic power dissipation µW	Delay ns
Binary Flip-Flop	Elgamel[25]	0.18 µm	3.3V	19.84	0.224
	Do[26]	0.18 µm	1.8V	4.7	0.138
	Sung[27]	0.18 µm	1.5V	47.8	0.402
	Shin[28]	0.35 µm	3.3V	540	0.427
Multi-valued flip-flop	Current[29]	2µm	5V	354.8	2.8
	Inaba(I)[30]	600nm	3.5V	80	420
	Inaba(II)[30]	600nm	3.5V	155	130
	Q-IDEN D_FF[19]	350nm	3.5V	138	0.43
	NMAX-TG D-FF[18]	350nm	3.5V	890	32.2
	NMIN-TG D_FF[18]	350nm	3.5V	880	29.0
	DLC based D-FF [21]	180nm	3.0V	157	0.57
	Proposed work	180nm	3.0V	56.19	1.187

The average power dissipation and propagation delay of the quaternary D-flip flop are compared with Q-IDEN D flip flop [19] and DLC based flip-flop [21].The comparison results are as shown in table 6. The average power dissipation and propagation delay of the counter is shown in table 7.

Table 7.Power and delay of counter

Average power dissipation (μW)	24.805
Propagation delay (ns)	1.1963

The D-flip flop proposed in this paper has both preset and clear inputs. These inputs are useful in the implementation of counters. This D-flip flop has less average power dissipation (56.19 μW) than Q-IDEN D flip flop [19]. But the propagation delay (1.187ns) is found to be slightly higher compared to Q-IDEN D flip flop. The increase in propagation delay can be neglected when compared to its functional advantages. It must be noted that the Q-IDEN D-flip flop has no preset and clear input and hence cannot be used for designing counters.

The counter designed using Quaternary D-flip flop has a propagation delay of 1.1963 ns and average power dissipation of 24.805 μW.

6. Conclusion

Multiple-valued flip-flops are necessary storage elements in design of multiple-valued sequential circuits. In this paper, quaternary D flip-flop with preset and clear is designed on the basis 3 input NMIN circuit. This quaternary D flip-flop is compared to previously designed binary and multi-valued D flip-flops. Proposed D flip-flop is better than all other flip-flops reported so far except propagation delay. Propagation delay is slightly higher in our flip-flop. But power dissipation is 64.33% less than that of DLC based D flip-flop and Q-IDEN D flip-flop. 2 bit binary counter can count only up to 4 counts, where as 2 bit quaternary counter can count up to 16. Multiple-valued counters are simple dividers that are basic components in most digital systems and can generate a multiple-valued output. 2 bit quaternary counter dissipates 24.805 μW of dynamic power. D flip-flop reported in this paper is useful for designing many low power sequential circuits such as counters, shift registers and state machines.

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Vasundara Patel K S is currently working at Dept of ECE, BMS College of Engg, Bangalore. She is pursuing Ph.D from, Bangalore University, she has industrial experience of 3 years and teaching experience of 11 years, Member of IMAPS INDIA, ISTE and IACSIT. She has published 10 conference papers and 2 Journal papers. Her areas of interest are Low power VLSI, Operation Research, Analog and mixed signal VLSI design, Multi-valued logic.

Dr K S Gurumurthy is currently working as professor and chairman, Dept. of E&C UVC College of Engg, Bangalore University, Bangalore. He has 33 years of teaching experience, Ph.D. (1990) from I I Sc and gold medal in ME, recipient of KHOSLA AWARD for the best Technical Paper, Member of IMAPS INDIA, MISTE and MIEEE. He has published more than 75 research papers. His areas of interest are Low power VLSI, Analog and mixed signal VLSI design, Analog and digital communication, DSP etc.