Design of AMBA Based AHB2APB Bridge

Vani.R.M [†] and M.Roopa [††],

[†]Reader and Head University Science Instrumentation Center, Gulbarga University, Gulbarga, INDIA
[††] Assistant Professor in the Department of Electronics and communication, Dayananda sagar college of engineering, Bangalore, INDIA

Summary
The Advanced Microcontroller Bus Architecture (AMBA) is an on-chip bus architecture used to strengthen the reusability of IP core and widely used interconnection standard for system on chip (SOC). The analysis of AMBA-based embedded systems a challenging proposition. The aim of this paper is to synthesize and simulate a complex interface bridge between Advanced High performance Bus (AHB) and Advanced Peripheral Bus (APB) known as AHB2APB Bridge. Here in this Paper Synthesized Net list of Bridge module is generated. To perform Functional and Timing Simulation using Xilinx and Modelsim.

Key words:
Bus Architecture, Peripheral Bus, synthesize, system on chip.

1. Introduction

AMBA's taget is to help designer of embedded system to meet challenges like design for low power consumption, to facilitate the right-first-time development of Embedded Microcontroller Products with one or more CPUs or signal processors, to be technology-independent and to encourage modular system [1]. To minimize the silicon infrastructure required supporting efficient on-chip and off-chip communication for both operation and manufacturing test.

This paper mainly concentrates on synthesis and simulation of AMBA based AHB2APB Bridge [2]. AHB2APB Bridge interfaces AHB and APB buses. It is required to bridge the communication gap between low bandwidth peripherals on APB with the high bandwidth ARM Processors and/or other high-speed devices on AHB. This is to ensure that there is no data loss between AHB to APB or APB to AHB data transfers.

Here we used Verilog HDL (Hardware Description Language) for designing the RTL (Register Transfer Level) code. Synthesis and Simulation is done using Xilinx and Modelsim[3].

.

2. Typical AMBA based microcontroller

An AMBA-based microcontroller typically consists of a high-performance system backbone bus (AMBA AHB or AMBA ASB), able to sustain the external memory bandwidth, on which the CPU, on-chip memory and other Direct Memory Access (DMA) devices reside. This bus provides a high-bandwidth interface between the elements that are involved in the majority of transfers. Also located on the high performance bus is a bridge to the lower bandwidth APB, where most of the peripheral devices in the system are located.

AMBA APB provides the basic peripheral macro cell communications infrastructure as a secondary bus from the higher bandwidth pipelined main system bus [4].Such peripherals typically:
(i)Have interfaces which are memory-mapped registers
(ii)Have no high-bandwidth interfaces
(iii) Are accessed under programmed control.

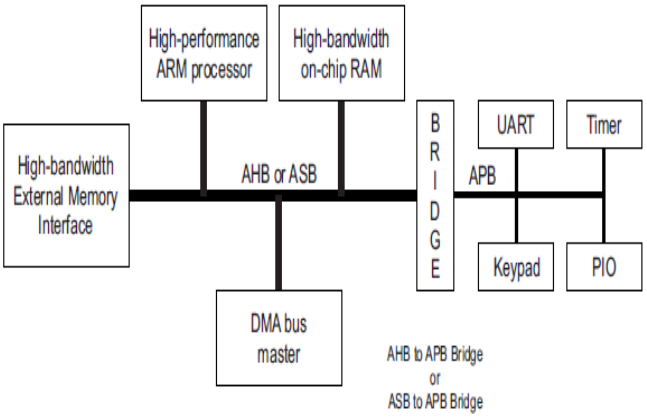

Figure 1. AMBA based Simple Microcontroller

3. Features of AHB2APB Bridge

The AHB2APB interfaces AHB and APB. It buffers address, controls and data from the AHB, drives the APB peripherals and return data along with response signal to the AHB [4]. The AHB2APB interface is designed to operate when AHB and APB clocks have the any combination of frequency and phase TheAHB2APB performs transfer of data from AHB to APB for write cycle and APB to AHB for Read cycle.

Interface between AMBA high performance bus (AHB) and AMBA peripheral bus (APB)[2].Provides latching of address, controls and data signals for APB peripherals.
Supports for the following

- APB compliant slaves and peripherals.
- Peripherals which require additional wait states

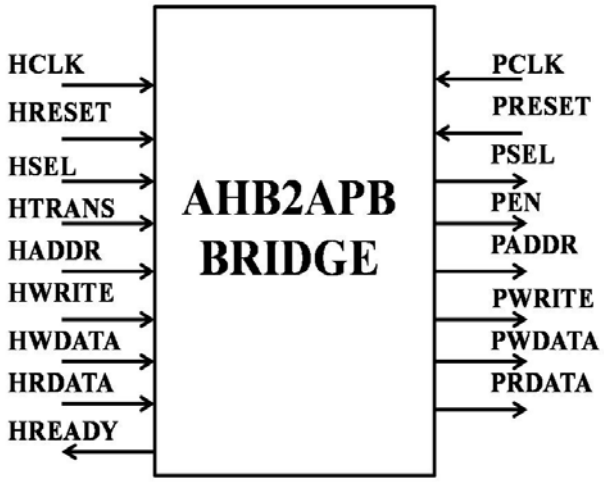

Figure 2. Pin details of AHB2APB Bridge

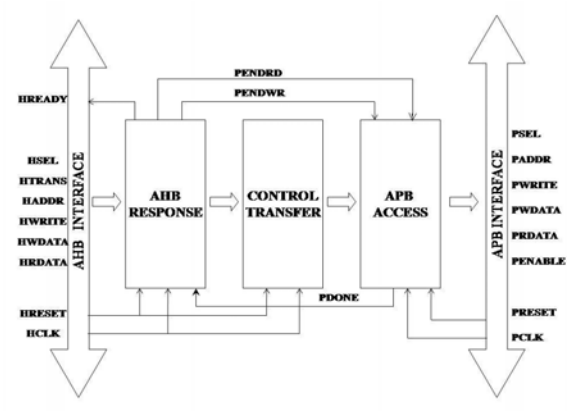

Figure 3. Internal architecture of the bridge

4. Implementation

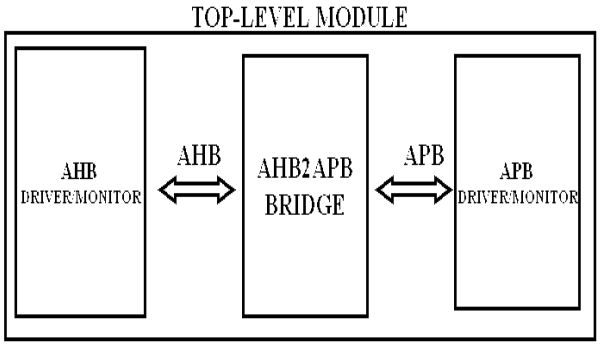

Figure 4. Design of AHB2APB Bridge

4.1. Design of AHB2APB Bridge

AHB2APB Bridge operates on HCLK and APB access sub module operates on PCLK. AHB response and Control transfer is together termed as AHB interface and APB access is termed as APB interface [7]. To ensure the correct generation of suitable control signals and address we use three internal signals in the bridge module namely: PENDWR (Pending Write), PENDRD (Pending Read), PDONE (Peripheral operation done).The capture of address & control, for Write or Read operation is done when HREADY, HTRANS and HSEL are valid.

The sub modules operate on different clock domains namely HCLK and PCLK, there is a need for interfacing these clock domains. The design becomes asynchronous at the boundary of interface, which results in setup and hold time violation, metastability and unreliable data transfers. So we need to go out for special design and interfacing techniques. In such a case if we need to do data transfer, there are very few methods to achieve this namely:

- Handshake signaling method
- Asynchronous FIFO

Both have its own advantages and disadvantages. In our paper we used Handshake signaling Method. In Handshake signaling method the AHB interface sends data to APB interface based on the handshake signals PENDWR (or PENDRD) and PDONE signals. The protocol for this uses the same method that is found with 8155 chip used with 8085 based on handshake signals Request and Acknowledge.

AHB interface asserts the PENDWR (or PENDRD) signal, asking the APB interface to accept or to send the data on the data bus.APB interface asserts the PDONE signal, asserting that it has accepted or sent the data. This method is straightforward, but it has got loop holes: when APB interface samples the AHB interface‘s PENDWR (or

PENDRD) line and AHB interface samples APB interface's PDONE line, they are done with respect to their internal clock, so there will be setup and hold time violation. To avoid this we use double stage synchronizers, which are immune to metastability to a good extent. The figure 5 below shows how this is done

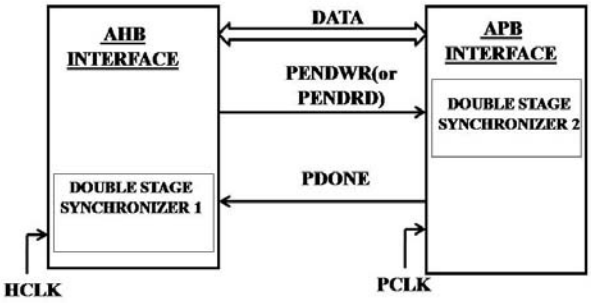

Figure 5. Handshake signaling method

The figure below shows the internal blocks of double stage synchronizer for PENDWR

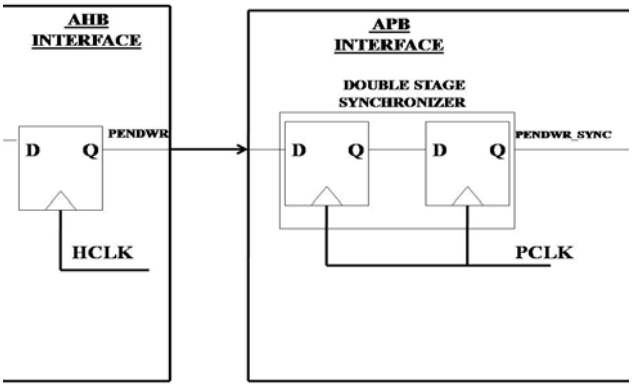

Figure 6. Double Stage Synchronizer

The double synchronizers for PENDRD and PDONE will be same as double synchronizers for PENDWR with the only difference that synchronizer for PDONE is made to operate on HCLK unlike PENDWR and PENRD which operate on PCLK.If we do the double synchronizing, then the transfer rate comes down, due to the fact that a lot of clock cycles are wasted just handshaking.

4.2. Design of AHB driver/monitor

The AHB Driver/Monitor is the module that drives the AHB2APB Bridge with suitable control signals, address and data [5]. Also monitors the input data that is received from the bridge, so that AHB master environment is created.

This module also contains the block for HCLK generation distributed to module AHB2APB Bridge and RESET generation distributed to the two other modules namely AHB2APB Bridge and APB Driver/Monitor and these two signals generated are obviously used in this module also.

4.3. Design of APB driver/monitor

The APB Driver/Monitor is the module that drives the AHB2APB Bridge with suitable data and also monitors the control signals, address and data that is received from the bridge, so as to create the environment of the APB Slave [6]. The control signals, address and data that is received from the bridge is suitably used for the data transaction from bridge to this module or vice versa depending whether it is a write or a read operation. This module contains block for PCLK generation, which is distributed to AHB2APB bridge module, and the PCLK generated is obviously used in this module also.

4.4 Design of top module

Out of all the modules present, this module is simplest and also very prominent. All the signals are taken as wire to interconnect various modules present under this top module. In this module all the three modules namely:

- AHB Driver/Monitor
- AHB2APB bridge
- APB Driver/Monitor

These modules are all instantiated using Positional assignments which is again simple compared to naming assignment which is little tedious.

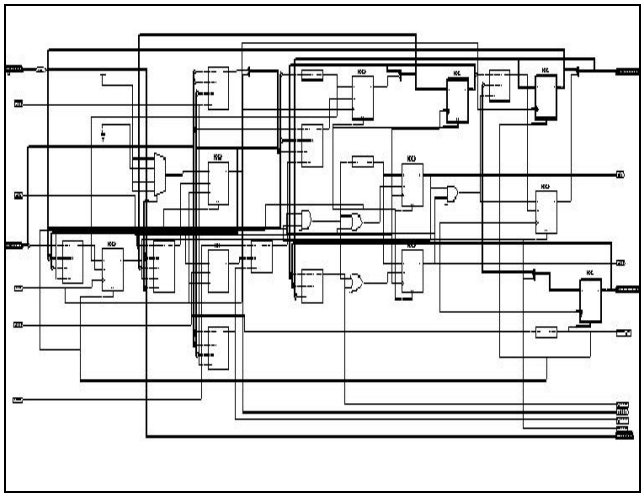

Figure 7. Synthesized Netlist of Bridge Module

5. Simulation results

Back annotation is the translation of a routed or fitted design to a timing simulation Netlist.Back annotation was performed on the Xilinx generated synthesis file for the AHB2APB Bridge module. In our paper only Bridge module is the synthesized module and AHB driver and APB monitor were test bench modules.

(1) With HCLK and PCLK having a ratio of 1:2.

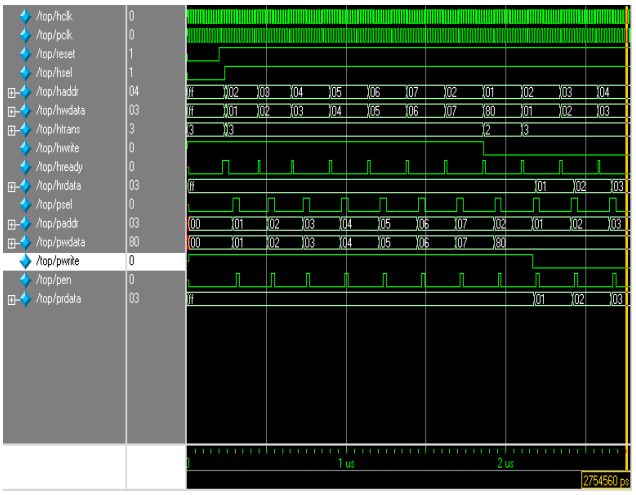

Figure 8. Burst of Write & Read Transfers

(2) With HCLK and PCLK having a phase difference of 90^0 and same frequency

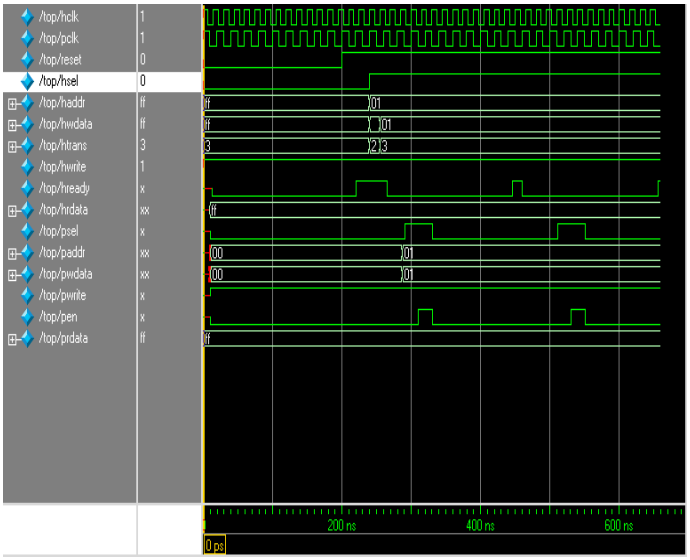

Figure 9. Single Write Transfer

6. Conclusion

The RTL Simulation of AHB2APB Bridge has been verified and validated by using suitable test benches namely AHB Driver/Monitor and APB Driver/Monitor.

The Synthesis of AHB2APB Bridge has been successfully completed by the extraction of Synthesized Netlist with unit delays & verified by comparing the Gate level Simulation with RTL Simulation results. The Back Annotation of AHB2APB Bridge has also been successfully completed by the extraction of Synthesized Netlist with suitable delays & verified by the comparison of Gate level simulation with RTL simulation results.

Thus AHB2APB Bridge is a standalone solution to extract the advantages of newly developed ARM based AMBA AHB bus by bridging the common gap between AHB and the existing APB bus.

References

[1] Jaehoon Song, Student member, IEEE, Hyunbean Yi, Member,IEEE, Juhee Han, and Sungju Park, Member, IEEE,"An Efficient SOC Test Technique by Reusing On/Off-Chip Bus Bridge"IEEE Transcactions on Circuits and Systems-I: Regular Papers, Vol,56,No.3,March2009.

[2] AMBA Specification (Rev 2.0).

[3] Xilinx ISE Synthesis and Verification Design Guide

[4] Sangik Choi and Shinwook Kang, Mobile SamsungElectronics Co.,Ltd, "Implementation of an On-Chip Bus Bridge between Heterogeneous Buses with

Different Clock Frequencies".IEEE, IDEAS'05,1098-8068/2005.
[5] AHB Example AMBA system; Technical Manual ARM1999.
[6] Flynn, D. Adv. RISC Machines Ltd., Cambridge, "AMBA: enabling reusable on-chip designs", IEEE Micro, Publication Date: Jul/Aug 1997.
[7] Wang Zhonghai,Ye Yizheng,Wang Jinxing, and Yu Mingyan, "Designing AHB/PCI Bridge,"in Proceedings of 4th International Conference on ASIC, Oct 2001,pp.578-580.

VANI. R.M. received her B.E. in Electrical and Electronics from the B.I.ET., Davanagere, Karnataka, and M.Tech in Industrial Electronics from S.J.C.E., Mysore. She has received her Ph.D in Applied Electronics from Gulbarga University, Gulbarga, India, in year 2005. She is working as Reader & Head, University Science Instrumentation Center, Gulbarga, since 1995. She has more than 85 research publications in national and international reputed journals and Conference proceedings. She presented many research papers in India & abroad. She has conducted several courses, workshops for the benefit of faculties and field engineers. Her areas of interest are microwave antennas, PC based Instrumentation, Embedded controllers and wireless communication. She has one UGC major research project to her credit.

Roopa. M. received B.E, Degree from U.V.C.E Bangalore University, Bangalore In 1990, M.E, Degree from U.V.C.E, Bangalore University, Bangalore, India in 1994, pursuing Ph.D in the Department of Applied Electronics, Gulbarga University, Gulbarga, INDIA, currently she is working as Assistant Professor in the Department of Electronics and communication, Dayananda sagar college of engineering, Bangalore, INDIA, her research interests include Design of Digital circuits, VLSI Design and Embedded systems.