

Delay Study of Virtex-2, Virtex-4 and Spartan-3E Based Truncated Multipliers

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Summary

Medical imaging technology requires real time efficient algorithms. The aim of this paper is to present the Field Programmable Gate Array (FPGA) based truncated multipliers delay study; implemented on Spartan-3E, Virtex-2 and Virtex-4 FPGAs using Very high speed integrated circuit Hardware Description Language (VHDL). The delay study was analyzed using analysis of variance (ANOVA) method using the software Statistical Package for Social Science (SPSS). The one way ANOVA method followed by post hoc Tukey's test using the software SPSS with a .05 significance level was used to compare the FPGA devices. Multiple comparison tests revealed that the differences between the FPGA devices are significant with a 95% confidence level. In all three FPGA devices as the size of truncated multipliers increases their mean latency value is also increases.

Key words:

Digital Signal Processing (DSP), Field Programmable Gate Array (FPGA), Spartan-3E, Truncated Multiplier, Virtex-2, Virtex-4, VHDL.

1. Introduction

The accomplishment of efficient realization of multiplication using Field Programmable Gate Arrays (FPGAs) can ascribe digital signal processing (DSP) blocks including small embedded multipliers to specific application in terms of speed, power dissipation and area.

A full width digital $n \times n$ multiplier computes the $2n$ output as a weighted sum of partial products [1]. The contribution of the least-significant columns of the product matrix to the final result becomes negligible if the product is truncated to n -bit. The truncated multipliers do not form all of the least-significant columns in the partial-product matrix. The area and power consumption of the arithmetic unit are significantly reduced as more columns are eliminated which also decreases the delay.

The only disadvantage is that using truncated multipliers also introduces errors into the computation due to the unformed columns of partial product bits [2-14].

This also reduces the area and power consumption of the multiplier [15].

A study by Al Mijalli [16] on latency has shown that truncated multipliers based on Spartan-3AN FPGA clearly

indicate as the size of truncated multiplier increases the mean delay time also increases.

The purpose of this study is to present the statistical evaluation effect of the truncated multipliers delays in Spartan-3E, Virtex-2 and Virtex-4 FPGA devices using one way ANOVA (analysis of variance) and post hoc Tukey's test using the SPSS (statistical Package for Social Science) software .

2. Architecture platform

FPGAs work as an ideal platform for the realization of highly computational and extremely parallel architecture. Here brief introduction about Spartan-3, Virtex-2 and Virtex-4 FPGAs from Xilinx are presented.

2.1. Spartan-3 FPGAs

The Spartan-3 FPGA [17] family is specifically designed to meet the needs of high volume, low unit cost electronic systems. The Spartan-3 consists of eight member offering densities ranging from 50,000 to five million system gates. The Spartan-3 consists of five fundamental programmable functional elements: CLBs, IOBs, Block RAMs, dedicated multipliers (18×18) and digital clock managers (DCMs), Spartan-3 FPGA family includes Spartan-3L, Spartan-3E, Spartan-3A, Spartan-3A DSP, Spartan-3AN and the extended Spartan-3A FPGAs. Particularly, the Spartan-3E is used as a target technology in this paper.

2.2. Virtex-2 FPGAs

The Virtex-2 FPGA family [18] is a platform developed for high performance from low-density to high-density designs that are based on IP cores and customized modules. Combining a wide variety of flexible features and a large range of densities up to 10 million system gates, the Virtex-2 family enhances programmable logic design capabilities. The Virtex-2 family comprises 11 members, ranging from 40K to 8M system gates.

The Virtex-2 FPGA family consists of four major elements such as Configurable Logic Blocks (CLBs), Block SelectRAM, 18×18 -bit dedicated multipliers and Digital

Clock Manager (DCM). The Virtex-2 architecture is optimized for high speed with low power consumption.

2.3. Virtex-4 FPGAs

Virtex-4 FPGA [19] consists of three platform families i.e., LX, SX and FX. Virtex-4 hard-IP core blocks include the IBM power PC (PPC) 405 32-bit reduced instruction set computer (RISC) processor; tri-mode Ethernet media access controls (MACs) 622 Mbps to 6.5 Gbps serial transceivers, dedicated DSP slices and high speed clock management circuitry. Virtex-4 devices consumes approximately 50% the power of respective Virtex-2 Pro devices due to static and dynamic power reduction enabled by triple-oxide technology and reduced core voltage and capacitance respectively. The Virtex-4 FPGA family comprises of CLBs, Block RAMs, Xtreme DSP Slices and DCMs.

3. FPGA design and implementation results

The design of truncated 4×4, 6×6, 8×8, and 12×12-bit multipliers are done using VHDL and implemented in a Xilinx Spartan-3E XC3S100E (package: vq100, speed grade: -5), Virtex-2 XC2V40 (package: fg256, speed grade: -6) and Virtex-4 XC4VLX40 (package: ff668, speed grade: -12) FPGAs using the Xilinx ISE 9.2i design tool [20].

A one-way ANOVA is applied to find out the effect of different multipliers on the mean delay time for Spartan-3E, Virtex-2 and Virtex-4 FPGAs.

Table 1 summarizes the statistics of latency in truncated multipliers for Spartan-3E, Virtex-2 and Virtex-4 FPGAs. The mean value for 4×4, 6×6, 8×8 and 12×12 multipliers in Virtex-2 and Virtex-4 are almost similar, as compared to Spartan-3E FPGA.

In all three FPGA devices as the size of truncated multipliers increases their mean latency value are also increases, similar result is obtained in [16] that as the size of multiplier increases the mean delay time also increases. Figure 1 shows the average value of mean delay time for 4×4, 6×6, 8×8 and 12×12 truncated multipliers for three devices. The average value of mean delay time for Virtex-2 is much lower in value than Spartan-3E and Virtex-4 FPGAs. Table 2 shows the ANOVA results on Spartan-3E, Virtex-2, and Virtex-4 FPGAs. ANOVA is applied to compare the mean delay time for three devices including Spartan-3E, Virtex-2 and Virtex-4 FPGAs; using four multipliers 4×4, 6×6, 8×8, and 12×12. There is a statistically significant difference at the 0.05 level in delay time for the three devices [$F(2, 57) = 7.302$, $p = .002$] compared by using ANOVA and post-hoc Tukey HSD multiple comparison tests at the 0.05 significance level. The test indicates that the mean of delay time for Spartan-3E (Mean = 13.2, Standard Deviation = 3.5) is significantly different from the other two devices; Virtex-4

(Mean = 10.76, Standard Deviation = 1.78) and Virtex-2 (Mean = 10.29, Standard Deviation = 2.26). However, there is no statistically significant difference in mean delay times of the devices Virtex-2 and Virtex-4 FPGAs.

Table 1: Statistics of latency in truncated multipliers for FPGAs

FPGA Devices	Bit Width	Mean (ns)	Std. Deviation (ns)	Std. Error of Mean (ns)
Spartan-3E	4×4	8.84	0.1140	0.0510
	6×6	11.76	1.0877	0.4864
	8×8	14.08	0.5541	0.2478
	12×12	18.12	0.4764	0.2131
Virtex-2	4×4	8.12	0.4764	0.2131
	6×6	8.92	0.3899	0.1744
	8×8	10.04	1.4029	0.6274
	12×12	13.42	0.4550	0.2035
Virtex-4	4×4	8.62	0.4604	0.2059
	6×6	10.36	0.4393	0.1965
	8×8	10.76	0.5899	0.2638
	12×12	13.3	0.5568	0.2490

4. Conclusion

In this paper we have presented a comparative study of latency in Spartan-3E, Virtex-2 and Virtex-4 FPGA devices using Statistical Analysis. The design of truncated 4×4, 6×6, 8×8, and 12×12-bit multipliers are done using VHDL and implemented in Xilinx FPGAs devices.

The one way ANOVA method followed by post hoc Tukey's test using the software SPSS with a .05 significance level was used to compare the FPGA devices. Multiple comparison tests revealed that the differences between the FPGA devices are significant with a 95% confidence level. In all three FPGA devices as the size of truncated multipliers increases their mean latency value is also increases.

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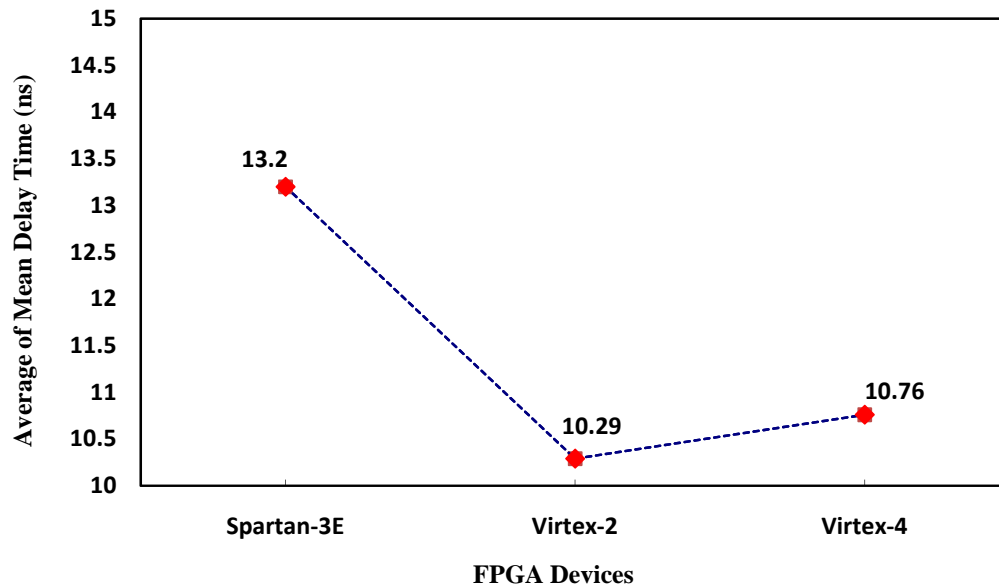


Fig. 1: The average of mean delay time for 4×4, 6×6, 8×8 and 12×12 truncated multipliers for Spartan-3E, Virtex-2 and Virtex-4 FPGA devices

Table 2: The results of multiple comparisons of delay time (ns) for four multipliers using the Tukey's HSD post-hoc test

(I) Devices	(J) Devices	Mean Difference (I-J)	Std. Error	Sig.	95% Confidence Interval	
					Lower Bound	Upper Bound
Spartan-3E	Virtex-2	2.90500*	.83216	.003	.9025	4.9075
	Virtex-4	2.44000*	.83216	.013	.4375	4.4425
Virtex-2	Spartan-3E	-2.90500*	.83216	.003	-4.9075	-.9025
	Virtex-4	-.46500	.83216	.842	-2.4675	1.5375
Virtex-4	Spartan-3E	-2.44000*	.83216	.013	-4.4425	-.4375
	Virtex-2	.46500	.83216	.842	-1.5375	2.4675

* The mean difference is significant at the 0.05 level.

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