Iterative Memory Shared Processor Array (MSPA) Architecture Design for Channel Estimation of Downlink OFDM IEEE 802.16a System

Savitri Galih[1], Trio Adiono[#2], Adit Kurniawan[#3], Iskandar[#4]

[1]Department of Informatics Widyatama University Jl Cikutra 204 Bandung, Indonesia
[1,2,3,4]School of Electronics and Informatics, Bandung Institute of Technology Jl Ganesha 10 Bandung, Indonesia

Abstract
WiMAX communication system has spectrum alocation that enable wireless service operator to operate throughout the world including the rural area. WiMAX is suitable for development country condition, where wiring infrastructures are limited. This advantages make WiMAX become a desirable future wireless technology that can be implemented in an developed archipelago country like Indonesia.
WiMAX Communication System needs accurate channel estimation process to predict fluctuative channel condition in order to equalize received signal with the transmitted signal. Channel Estimation recent studies, mostly analyzed the algorithm side without considering implementation issue. The hardware implementation of complex signal processing algorithm such as MMSE(Minimum Mean Square Error) channel estimation with high computational complexity, are required to achieve robust trasmission, whereas mobile wireless aplication require low power dissipation. Therefore we need an algorithm mapping method to the corresponding hardware architecture that practically fits with overall system hardware. The proposed architecture aims to achieve low power and efficient resource utilization by using iterative memory shared architecture.

Keywords
channel estimation; OFDM; fixed WiMAX; Hardware Architecture

1. Introduction

Fourth generation (4G) wireless system nowadays, gain a lot attention among science community. The implementation of complex signal processing algorithms are required to achieve robust transmission, whereas mobile wireless application require low power dissipation. Therefore, eficient transmission plays important role to achieve high datarate. One of the method that gain alot of attention is OFDM (Orthogonal Frequency Division Multiplexing). OFDM as developed and has implemented in wireless communication system due to its highspeed transmission, and high bandwidth efficient. OFDM also implemented in broadband wireless standard, such as IEEE 802.16a (WiMAX) and become core technique for 4 G wireless mobile communication.

WiMAX system is vulnerable to high fading channel condition. Complex baseband signal, will experience some impairment due to selective frequency and time-varying channel. The system will need channel estimation modul to estimate and compensate these impairment, and resulting receiver baseband signal which similar with transmitted baseband signal. Channel estimation is required to correct the filtering process suffered by transmitted signal during its trip at the channel. MMSE channel estimation has been known as a superior performance channel estimation especially in low SNR . However, this algorithm has high computational complexity which prohibits its direct real-time implementation low complexity partial-sampled MMSE[1,3,7,8] (Minimum Mean Square Error) channel estimation for IEEE 802.16a (fixed WiMAX) Orthogonal Frequency Division Multiplexing (OFDM) downlink system. The hardware implementation of the MMSE OFDM channel estimation basically employs large matrix vector multiplication corresponds to the number of OFDMA subcarriers. The most area efficient architecture for matrix vector multiplication is sequential architecture which consist of only one processor element. However this minimum-area solution can not meet the low latency requirement of mobile WiMAX OFDMA system. Fast but large matrix vector multiplication architecture, i.e Systolic array architecture [10, 11, 12, 13] has advantages in regularity and high throughput but still suffers the overlapping data storages, idle processing and high area requirement. MSPA (Memory Sharing Processor Array) [9] overcomes these problems by minimize the data storage by sharing memory units to several processor array and achieve better efficiency than conventional systolic architecture, but the data throughput is not suitable and far beyond the clock alocation compute based on standard parameter i.e sample period is much larger than the computational delay of MSPA hardware unit. In this paper we will present methodes that jointly optimize algorithm and hardware performance and improve the parallel efficiency of MSPA architecture for MMSE channel estimation architecture by fold the processor array and reducing the number of

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processing element through time multiplexing, the proposed architecture is called Folding MSPA.

2. System Model

The OFDM/OFDMA system with pilot based channel estimation is given in figure 1.

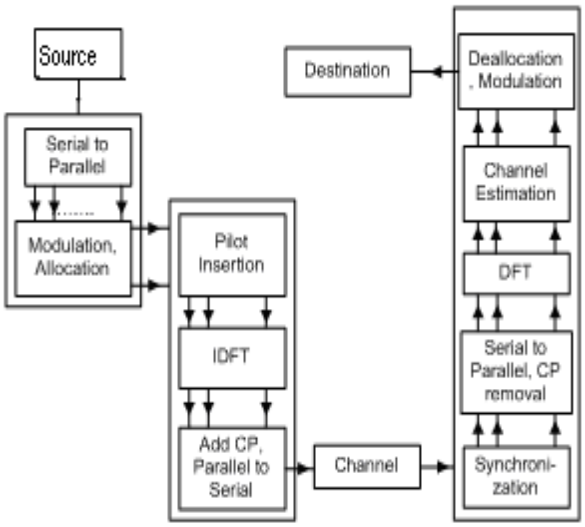


Fig. 1 Block Diagram of The Pilot Based OFDM System

The data bits provided from the source are converted from serial to parallel to form parallel data of some subchannels[5].

Each parallel subchannel modulated to complex QAM symbols of Nu active subcarriers. The modulated data with other null carrier as guardband and DC form N subcarriers. This data sequence of length N {Xk} are then fed into IDFT block symbol by symbol to transform them into time domain and generate an OFDM signal {xn} with the following equation :

$$x_n = IDFT\{X_k\} = \sum_{k=0}^{N-1} X_k e^{j2\pi kn/N}, \quad n = 0,1,\ldots, N-1 \qquad (1)$$

Where N is the DFT length or the number of subcarriers. To prevent inter-symbol interference (ISI), a cyclic prefix of Ng samples is inserted at the beginning of every symbol. After D/A conversion, the signal is transmitted through the frequency selective time varying fading channel with additive noise.

$$h(t,\tau) = \sum_r h_r(t)\delta(\tau - \tau_r), \qquad (2)$$

Assumed that the impulse response of the multipath fading channel is given by [18]:

Where hr(t) and r are the gain and delay of the r-th path, respectively. The received signal, which has been corrupted by the multipath fading channel and contaminated by the additive white Gaussian noise can be formulated as

$$y(\tau) = \sum_r h_r(t)x(\tau - \tau_r) + w(\tau), \qquad (3)$$

Where x( ) is the continuous-time representation of the transmitted discrete-time signal, xn. The received continuous-time signal then convert back to a discrete –time signal yn, the receiver do synchronization, downsampling, and removes the cyclic prefix. The simplified baseband model of the received samples takes the form of :

$$y_n = \sum_{l=0}^{L-1} h(l)x(n-l) + w(n) \qquad (4)$$

Where L is the number of sample-spaced channel taps, w(n) is additive white Gaussian noise (AWGN) sample with zero mean and variance of w, and h(l) is the time domain channel impulse response (CIR) for the current OFDM symbol. It is assumed that time and frequency synchronization is perfect.

FFT transforms yn to the frequency domain received base band data :

$$Y_k = FFT(y_n) = X_k H_k + W_k \qquad (5)$$

Where H and W are FFT of h and w repectively. Following FFT block, the pilot signals are extracted and the Channel Estimation is carried out to obtain estimated channel response $\hat{H}_k$ for the data sub-channels. Then the transmitted data is estimated by equalization process :

$$\hat{X}_k = \frac{Y_k}{\hat{H}_k} \qquad (6)$$

After signal demapping, the sourece binary information data are re-constructed at the receiver output.

3. Channel Estimation

In this section, the different types of channel estimators considered in this paper are explained. After channel estimation process at pilot subcarrier position, the channel responses at the rest of data subcarrier are estimated by interpolation. First is interpolation at time domain which has 2 symbols time spacing. In this paper we use linear interpolation for time domain interpolation because it is sufficient for small time spacing. H is estimated by

vertically 1D linear interpolation, after vertical time interpolation, tile structure is described at figure 3.a.
The MMSE channel estimator employs the second order statistics of the channel condition to minimize the mean-square error. The major disadvantage of the MMSE estimator is its high complexity, which grow exponentially with the observation sample. The frequency domain MMSE estimate of channel response is given by[4]:

$$\hat{H}_{P,MMSE} = R_{H_P H_P}\left(R_{H_P H_P} + \sigma_n^2\left(X_P X_P^H\right)^{-1}\right)^{-1}\hat{H}_{P,LS} \quad (7)$$

Where HP,LS is the LS estimate of channel condition at pilot position, n2 is the variance of noise , XP is a matrix containing the transmitted pilot on its diagonal, $R_{H_P H_P}$ is the channel autocorrelation matrix defined by

$$R_{H_P H_P} = E\left\{H_P H_P^H\right\} \quad (8)$$

For this case, the correlation function between the channel frequency response value is given by[5] :

$$E\left\{H_m H_n^*\right\} = \begin{cases} 1, & m = n \\ \dfrac{1 - e^{-j2\pi\left(N_g(m-n)/N\right)}}{j2\pi\left(N_g(m-n)/N\right)}, & m \neq n \end{cases} \quad (9)$$

From equation (9) we can get $R_{H_P H_P}$.
MMSE interpolation for all subcarrier can be perform by modifying the MMSE estimator at equation (7) to obtain all data subcarrier's channel responses, with this equation[1] :

$$\hat{H}_{MMSE} = R_{HH_P}\left(R_{HH_P} + \sigma_n^2\left(X_P X_P^H\right)^{-1}\right)^{-1}\hat{H}_{P,LS} \quad (10)$$
$$= Q.\hat{H}_{P,LS}$$

The MMSE estimator (7 and 10) uses a priori knowledge of n2 (or SNR) and RHH , and is optimal when these statistics of the channel are known. As will become clear from the further discussion, SNR value can be predefined: higher target SNRs are preferable to obtain more accurate estimates. Also the robust estimator design necessitates account for the worst correlation of the multipath channel, namely when the channel power-delay profile (PDP) is uniform [14].

4. Hardware Implementation

There are some hardware architecture that can be implemented in Matrix Vector Multiplication which is the main process in MMSE Channel Estimation. Milovanovic et.al proposed linear systolic array to process matrix vector multiplication, as describe at figure 4 below
Kunieda et.al designed MSPA (Memory Sharing Processor Array to process Matrix Vector Multiplication. The architecture is descriped at figure 5 below.

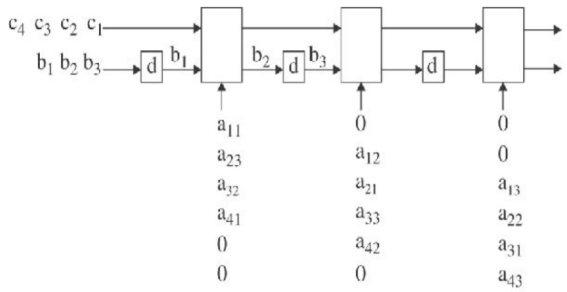


Fig. 4. Linear Systolic Architecture propsed by Mlovanovic

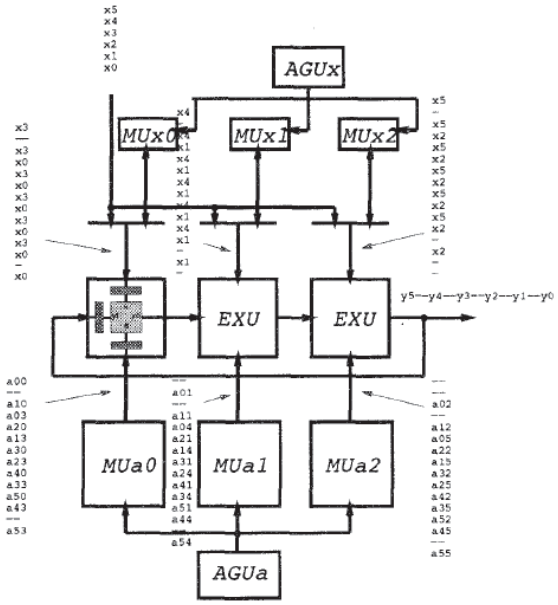


Fig. 5 . MSPA Architecture

The architecture of the Menory Sharing Processor Array (MSPA) consists of a processor array with direct links and buses connected with memory units and their address generation unit (AGU). The memory units can supply the multiple data stream into the processor arrays. The memory units store and load input data to processor array according to the control signal generated by the AGU.[9].

5. Folding MSPA Architechture

The proposed Folding MSPA architecture is the modification of original MSPA architecture by Kunieda, and has been adjust to match OFDM IEEE 802.16a standard parameters below

From the table above, we derive clock allocation that match with the standard and system specification. MSPA architecture implementation to the system, resulting lower computation time than the clock allocation stated above.

Therefore we need folding process to the MSPA architecture. This modified architecture has less processor elements than MSPA architecture. To finish all matrix vector multiplication computation, iteration is carried out with the number of iteration is adjusted as the stated clock allocation.

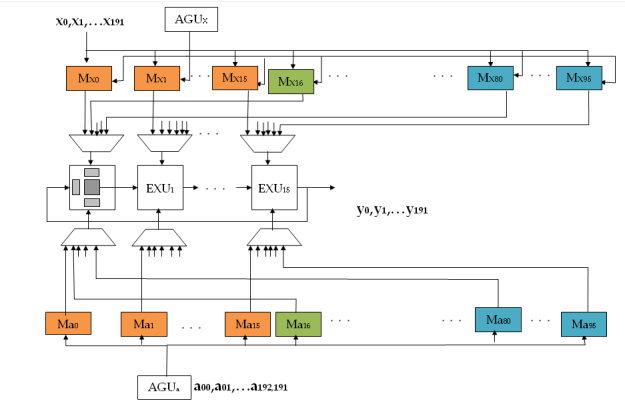
Table I Parameter Used In The Paper

Primitive Parameters	Parameter Name	Value	Value
BW(MHz)	Nominal Channel Bandwidth (MHz)	10	5
N_{used}	number of used subcarriers	192	192
n	sampling factor	1.142857143	1.142857143
G	rasio CP	0.125	0.125

Derived Parameters	Parameter Name	Value	Value
N_{FFT}		256	256
F_S= floor(n.BW/ 8000)x8000	sampling freq (Hz)	11424000	5712000
$\Delta f = F_S/N_{FFT}$	subcarrier spacing (Hz)	44625	22312.5
$T_b = 1/\Delta f$	Useful symbol time (s)	2.2409E-05	4.48179E-05
Tg= G.Tb	CP Time (s)	2.80112E-06	5.60224E-06
TS =Tg + Tb	OFDM Symbol time (s)	2.52101E-05	5.04202E-05
freq clock (MHz)		56	56
Clock Allocation = frek.clock x useful symbol time (clockcycle)	1255	2510	

In the processor element input, the multiplexer is added to choose which memory to supply input to PE, correspond to the iteration sequence. This architecture is called as Folding MSPA and descriped by the figure below

The selection of PE's number is fitted with the clock allocation for channel estimation modul in system hardware. This clock allocation is calculate under assumption of low power specification and IEEE 802.16a primitive and derived parameters. The clock allocation is defined by frequency clock times useful symbol time in clock cycle. In this research we use 56 MHz frequency clock for low power consideration.



6. Implementation Result

In this section, we compare the folding MSPA architecture with oher architectures from the reference. The table 3 below, shows the hardware performance comparation. The sequential architecture has higher computation time than the computed clock allocation for the OFDMA mobile WiMAX channel estimation calculated as shown from table 2. The other two architectures (systolic array and MSPA) have much lower computation time than the clock allocation, as a result, the architectures have more iddle time during computation process of channel estimation system. Folding MSPA architecture is more suitable with the considered system, since the architecture has equivalent computation time with the stated allocation clock.

In addition, the proposed architecture has higher processor utility than the three other architectures, showed by its highest parallel efficiency. The parallel efficiency is defined as sequential computation time divide by processor number times the parallel computation time.

Table II Hardware Design Performance Comparation

Architectue Type	Number of Processor Elements	Iteration Number	Total Operation Time	Architecture Efficiency
Sequential	1	192	36.684	1
Systolic Array (Milovanovic et.al)	192	1	386	0.492
MSPA (Kunieda)	96	1	480	0.800
Folding MSPA (Proposed)	16	1	2450	0.940

7. Conclusion

In this paper we introduce Folding MSPA Architecture for downlink OFDM IEEE 802.16a (fixed WiMAX) system. This architecture is suitable for MMSE channel estimation which require large matrix vector multiplication, since its computation time is equal with clock allocation computed from IEEE 802.16a standard parameter. Moreover, this architecture has higher parallel efficiency than systolic array and original MSPA architecture.

References

[1] T.Yucek, M. Kemal Ozdemir, H. Arslan, F. E. Retnasothie, "A Comparative Study of Initial Downlink Channel Estimation Algorithms for Mobile WiMAX", IEEE Mobile WiMAX Symposium, March 2007 .

[2] S. Coleri, M. Ergen, A. Puri, A. Bahai, "Channel Estimation Techniques Based on Pilot Arrangement in OFDM System", IEEE Trans. On Broadcasting Vol. 48, No. 3, September 2002.

[3] R. Alihemmati and M. E. Kalantari, "On Channel Estimation & Equalization in OFDM based Broadband Fixed Wireless MAN Networks", The 7th International Conference on Advanced Communication Technology ICACT, Vol. 1, pp 224-229, 2005.

[4] M. H. Hsieh and C. H. Wei, "Channel Estimation for OFDM System Based on Comb-Type Pilot Arrangement in Frequency Selective Fading Channels", IEEE Transactions on Consumer Electronics, Vol. 44, No. 1, February 1998.

[5] L. Hanzo, M. Munster, B. J. Choi, T. Keller, "OFDM and MC-CDMA for Broadband and Multiuser Communications, WLANs and Broadcasting", IEEE Press, John Wiley & Son, 2003.

[6] J. G. Proakis, " Digital Communications", Mc Graw Hill , 3rd edition, 1995.

[7] O. Edfors, M. Sandell, J van de Beek, S. K Wilson, P. O Borjesson, "OFDM Channel Estimation by Singular Value Decomposition" in Proc IEEE 46th Vehicular Technology Conference, Atlanta, GA, USA, Apr. 1996, pp 923-927

[8] J. J. van Beek, O. Edfors, M. Sandell, S.K. Wilson, and P. O. Borjesson, "On Channel Estimation in OFDM systems", in Proc. IEEE Vehicular Technology Conf., vol. 2, Chicago,II,July 1995, pp.815-819.

[9] H. Kunieda, K. Hagiwara, "Effective Processor Array Architecture with Shared Memory", Proceedings of APCCAS'94 - 1994 Asia Pacific Conference on Circuits and Systems. 1994

[10] [Ho09] H.Ho, V.Szwarc, T. Kwasniewski, "A Reconfigurable Systolic Array Architecture for Multicarrier Wireless and Multirate Applications", International Journal of Reconfigurable Computing, 2009

[11] E.I. Milovanovic, M.K. Stojev, N.M. Novakovic, IZ Milovanovic, TI Tokic, "Matrix-Vector Multiplication on a Fixed-SizeLinear Systolic Array", An International Journal of computers and Mathematics with Application, elsevier, 2000.

[12] I.Z. Milovanovic, E.I. Milovanovic, MP Bekakos,, " Synthesis of a Unidirectional Systolic Array for Matrix Vector Multiplication", M2006athematical and Computer Modelling, Elsevier, 2006

[13] Radhika S. Grover, Weijia Shang, Qiang Li, "Bit –level two's complement matrix multiplication", Elsevier Integration, the VLSI Journal 33, 2002

[14] [Sito08]Miyoshi Sito, Masahiro Yoshida, Makoto Mori, "Digital Baseband SoC for Mobile WiMAX Terminal Equipment", Fujitsu Sci. Tech Journal vol 44, July 2008

[15] Savitri Galih, Riafeni Karlina, Ade Irawan, Trio Adiono, Adit Kurniawan, Iskandar, "Low Complexity Partial Sampling MMSE Channel Estimation for Downlink OFDMA IEEE 802.16e System", ISPACS 2009 proceeding, November 2009.

[16] D. Markovic, B. Nikolic, RW Brodersen, "Power and Area Efficient VLSI Architectures for Communication Signal Processing", IEEE ICC 2006 Proceeding, 2006

[17] K.K. Parhi, VLSI Digital Signal Processing Systems, New York: NY, John Wiley & Sons, 1999.

[18] T. D. Chiueh and P. Y. Tsai, "OFDM Baseband Receiver Design for Wireless Communications,Assisted Microtechnology", John Wiley & Sons (Asia) Pte Ltd, 2007.

[19] N Weste, D Harris, Principles of CMOS VLSI Design., 3rd Edition, 2005. Addison-Wesley