A Novel implementation of OFDM using FPGA

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Summary
Summery-Orthogonal Frequency Division Multiplexing (OFDM) is a multi-carrier modulation technique which divides the available spectrum into many carriers. The actual and next communication schemes tend to use OFDM systems in order to provide high baud rates and less inter symbol interference. Some examples are IEEE802.11 standard, IEEE802.16 standard, MC-CDMA, Digital Video Broadcasting, Wireless USB. FPGAs could support many of its operations. The main advantage of OFDM is their robustness to channel fading in wireless environment. The objective of this paper is to design and implement a base band OFDM transmitter and receiver on FPGA hardware. All modules are designed using VHDL programming language. Input and output data is displayed to computer and the results is compared using Matlab software.

Keywords
Orthogonal frequency division multiplexing (OFDM); Field programmable gate array (FPGA); Hardware description language (HDL); bet error rate (BER); signal to noise ratio (SNR);Frequency Division Multiple Access (FDMA).

1. Introduction

Orthogonal Frequency Division Multiplexing (OFDM) could be tracked to 1950's but it had become very popular at these days, allowing high speeds at wireless communications [1]. OFDM could be considered either a modulation or multiplexing technique; its hierarchy corresponds to the physical and medium access layer. A basic OFDM system consists of a QAM or PSK modulator/demodulator, a serial to parallel / parallel to serial converter, and an IFFT/FFT module. The iterative nature of the FFT and its computational order makes OFDM ideal for a dedicated architecture outside or parallel to the main processor. Using FPGA instead of an ASIC gives also flexibility for reconfiguration, which is a need for the Software Defined Radio (SDR) concept.

OFDM is a multicarrier modulation technique, which provides high bandwidth efficiency because the carriers are orthogonal to each other and multiple carriers share the data among themselves. The main advantage of this transmission technique is their robustness to channel fading in wireless communication environment [2].

This paper aims to give an idea of what is an OFDM system, its implementation and the analysis of the obtained results of the simulations testing. This OFDM system is able to support different M-QAM modulation schemes. The M-QAM modulation schemes used for the multicarrier OFDM transmitter/receiver subsystem are basically BPSK, 4-QAM, 8-QAM, 16-QAM and 64-QAM modulations. Simulation results are provided within this paper. Simulation results have been obtained through the System Generator and Matlab/Simulink tools.

OFDM uses the spectrum efficiently compared to FDMA by spacing the channels much closer together and making all carriers orthogonal to one another to prevent interference between the closely spaced carriers.

The next of this paper is organized as follows. Section-2 provides an OFDM overview; section-3 introduces a VHDL overview; section-4 presents an OFDM uplink; section-5 gives an OFDM downlink; section-6 introduces software simulation of OFDM systems; section-7 presents the VHDL emulation of the OFDM components; finally, section-8 provides the simulation results and conclusions.

2. OFDM overview

OFDM is an attractive modulation scheme used in broadband wireless systems that encounter large delay spreads. OFDM avoids temporal equalization altogether, using a cyclic prefix technique with a small penalty in channel capacity. Where Line-of-Sight (LoS) cannot be achieved, there is likely to be significant multipath dispersion, which could limit the maximum data rate. Technologies like OFDM are probably best placed to overcome these, allowing nearly arbitrary data rates on dispersive channels. The difference between single carrier transmission and multicarrier transmission (OFDM) shown in Fig.1 [3].

For each subcarrier a rectangular pulse shaping is applied. The guard interval or cyclic extension is added to the subcarrier signal in order to avoid intersymbol interference (ISI), which occurs in multipath channels. At each receiver the cyclic prefix is removed and only the time interval [0, Ts] is evaluated. The total OFDM block duration is [T=Ts

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+ Tg]. Each subcarrier can be modulated independently as shown in Fig.2. The spectra of the subcarriers overlap, but the subcarrier signals are mutually orthogonal, and the modulation symbol can be recovered by a simple correlation as shown in Fig.3 [3].

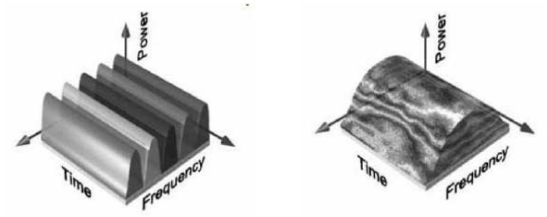

Fig.1 Single carrier versus multicarrier transmission

A. Advantages of OFDM

In general, OFDM systems have the following advantages: (i) makes efficient use of the spectrum by allowing overlap; (ii) By dividing the channel into narrowband flat fading subchannels, OFDM is more resistant to frequency selective fading than single carrier systems are; (iii) Eliminates ISI and IFI through use of a cyclic prefix; (iv) using adequate channel coding and interleaving one can recover symbols lost due to the frequency selectivity of the channel; (v) channel equalization becomes simpler than by using adaptive equalization techniques with single carrier systems; (vi) It is possible to use maximum likelihood decoding with reasonable complexity; (vii) OFDM is computationally efficient by using FFT techniques to implement the modulation and demodulation functions; (viii) Is less sensitive to sample timing offsets than single carrier systems are, and (ix) provides good protection against cochannel interference and impulsive parasitic noise [3].

B. Disadvantages of OFDM

OFDM systems have the following disadvantages: (i) High synchronism accuracy; (ii) Multipath propagation must be avoided in other orthogonality not be affected, and (iii) Large peak-to-mean power ratio due to the superposition of all subcarrier signals, this can become a distortion problem.

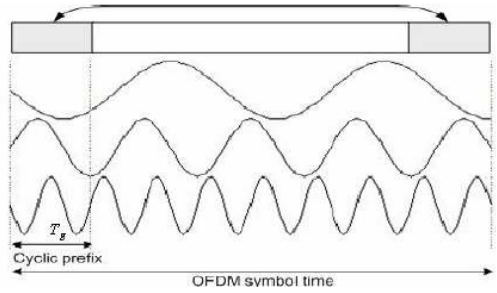

Fig.2 Cyclic Extension

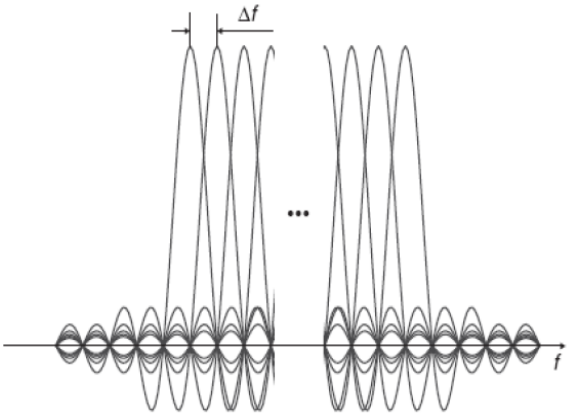

Fig. 3 OFDM subcarriers representation

C. OFDM Transmitter

As shown in Fig.4, OFDM transmitter basically consists of: (i) serial-to-parallel converter; (ii) constellation modulator; (iii) the IFFT block; (iv) parallel-to-serial converter, and (v) digital-to-analog converter [3]. The serial to parallel converter receive the M serial bits to be transmitted, and those bits are divided into N subblocks of m×n bits each subblock. Those N subblocks will be mapped by the constellation modulator using Gray codification, this way an + jbn values are obtained in the constellation of the modulator. The M-QAM encoder converts input data into complex valued constellation points, according to a given constellation, BPSK, 4QAM, 8-QAM, 16-QAM, 64-QAM and so on [4]. The amount of data transmitted on each subcarrier depends on the constellation; 4QAM and 16QAM transmit two and four data bits per subcarrier, respectively. Which constellation to use depends on the quality of the communications channel? In a channel with high interference a small modulation scheme like BPSK is favorable, since the required signal to noise ratio (SNR) in the receiver is low, whereas in a interference free channel a larger constellation is more beneficial due to the higher bit rate.[3, 4]. It is important to notice that in that mapping block, bits are converted into complex symbols (phasors) having the information of the constellation in its I, Q components.[3, 4].

The Inverse Fast Fourier Transform (IFFT) transforms the signals from the frequency domain to the time domain; an IFFT converts a number of complex data points, of length that is power of 2, into the same number of points but in the time domain. The number of subcarriers determines how many sub-bands the available spectrum is split into.[3, 4]. The Cyclic Prefix(CP) is a copy of the last N samples from the IFFT, which are placed at the beginning of the OFDM frame. There are two reasons to insert a CP.

Assuming that the CP is longer than the channels impulse response, the convolution between the data and the channel impulse response will act like a circular convolution and interference from the previous symbol will only affect the CP [4]. The CP is then discarded in the receiver and the circular convolution makes equalization in the receiver easier. However, if the number of samples in the CP is large, the data transmission rate will decrease significantly, since the CP does not carry any useful data. Thus, it is important to choose the minimum necessary CP to maximize the efficiency of the system.[11].

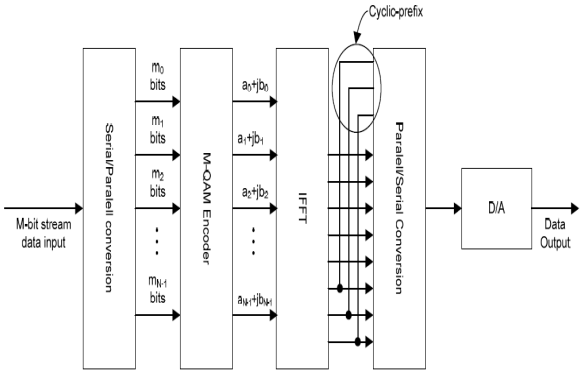

Fig.4 OFDM transmitter

D. OFDM Receiver

As shown in Fig.5, OFDM receiver basically consists of: (i) Analog to digital converter; (ii) Serial to parallel converter; (iii) Cyclic prefix removal; (iv) The FFT block; (iv) M-QAM decoder, and (v) Parallel to serial converter. The received symbol is in time domain and it can be distorted due to the effect of the channel. The received signal goes through a serial to parallel converter and cyclic prefix removal [3]. After the cyclic prefix removal, the signals are passed through an N-point fast Fourier transform to convert the signal to frequency domain.

The output of the FFT is formed from the first M samples of the output. The demodulation can be made by DFT, or better, by FFT, that is it efficient implementation that can be used reducing the time of processing and the used hardware [6]. FFT calculates DFT with a great reduction in the amount of operations, leaving several existent redundancies in the direct calculation of DFT [5, 6, 9]. At the decoder, a mapped symbol (point) of the transmitted constellation may have changed due to the additive noise in the communications channel, a miss-adjustment in the sampling time at the receiver, or several other unwanted causes. Therefore, it is necessary to define a threshold to facilitate the decision making in the receiver constellation. That is the function of the M-QAM decoder [3, 5].

E. Experimental Results

The discussed OFDM system presented in the above few sections will be simulated using MATLAB-2009a on a personal computer of the following specifications: (i) Intel processor 3.2 GHZ Pentium-four; (ii) 1MB cache RAM; (iii) 512 MB RAM; (iv) SATA hard disk 160GB. In this part the simulation of OFDM system using MATLAB Simulink tools will be obtained. This OFDM system consists of 8-point FFT/IFFT, 3-bit cyclic prefix, 8-bit serial to parallel converter, and the mapper can be BPSK, QPSK, 8-PSK, 16-PSK, or 64-PSK.

The block diagram of the system using MATLAB Simulink tools is obtained in fig. 6. In this part we will show the relation between BER and SNR for OFDM systems that are mentioned previously as shown in fig. 7, and we get the following: (i) The more complex modulation scheme, the larger value of BER will be evaluated and (ii) The SNR is inversely proportional to BER.

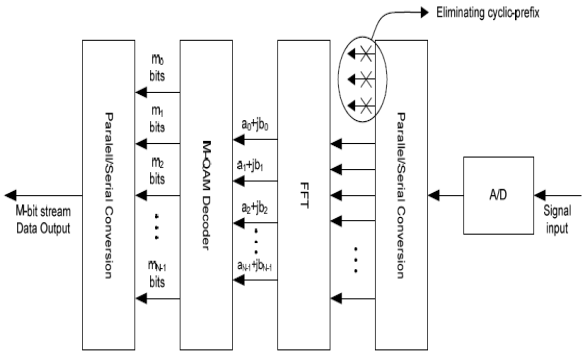

Fig.5 OFDM receiver

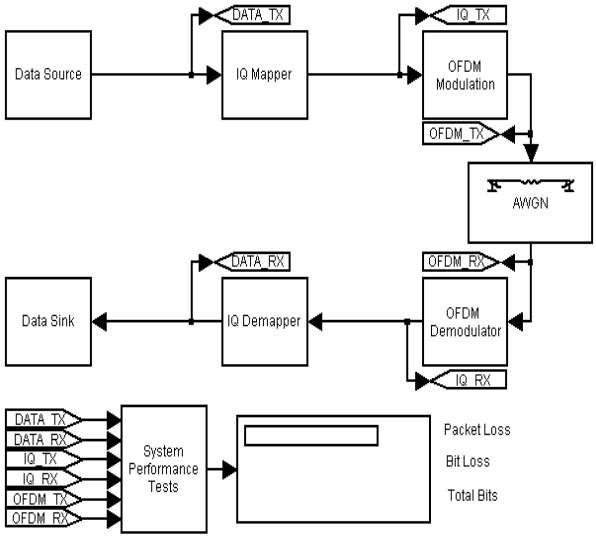

Fig.6 OFDM block diagram using MATLAB Simulink tools

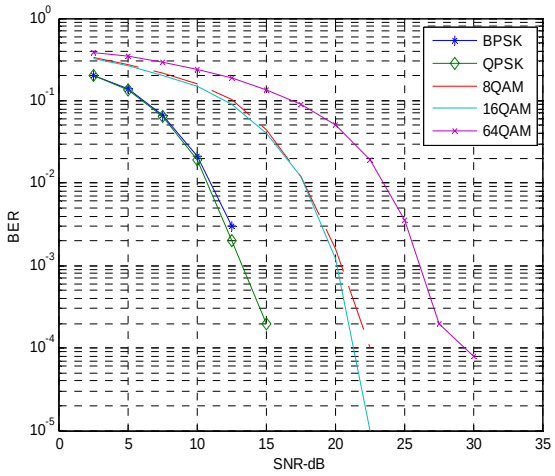

Fig. 7 The relation between BER and SNR for different OFDM

3. VHDL EMULATION

A .VHDL Overview

VHDL is an acronym for VHSIC (Very High Speed Integrated Circuit) Hardware Description Language. It is intended for documenting and modeling digital systems ranging from a small chip to a large system. It can be used to model a digital system at any level of abstraction ranging from the architectural level down to the gate level [3]. Due to the increase of the amount of resources needed for the PLD's and the FPGA's, it became difficult to program this devices, to solve this issue, method to plan the desired logic functions was created. VHDL language can be regarded as an integration of the following languages: Sequential language, Concurrent language, Net list language, Timing specifications, and Waveform generation. It allows the user to model the system as an interconnection of components. Test waveforms can be generated using the same constructs. All the above constructs may be combined to provide a comprehensive description of the system in a single model. The models written in VHDL can be verified using a VHDL simulator. It inherits extensive range of modeling capabilities that are difficult to understand [3].

B. VHDL Emulation of OFDM Elements

In this part the emulation of OFDM elements will be implemented. The implementation process will be carried out using the Mentor Graphics tool FPGA-Advantage 7.2 on the same personal computer presented in the simulated part. The mapping module used is BPSK type of modulation. BPSK is used because module is much easier to design compared to QPSK or other modulation method. If the input is '1' then the value is mapped with '1' while if the input is '0' the value is mapped with '0'. This type of modulation is monopodal type. The input passed through this module actually does not get any changes to the value, but it can be assumed that the input is modulated after pass through it. The serial-to-parallel converter can convert the 8-bit serial data input to parallel form and vice versa for parallel-to-serial converter. As shown in Fig.8, the FFT computation is accomplished in three stages. The X(0) until X(7) variable is denoted as the input value for FFT computation and Y(0) until Y(7) is denoted as the output. There are two operations to complete the computation in each stage. The upward arrow will execute addition operation while downward arrow will execute subtraction operation. The subtracted value is multiplied with twiddle factor value before being processed into the nest stage. This operation is done concurrently and is known as butterfly process. For second stage, there are two butterfly process with each process get reduced input variable. In the first stage the butterfly process get eight input variable while in the second stage, each butterfly process get four input variable that is from first stage computation. This process is continued until third stage. In third stage, there are four butterfly processes. Noted that each of the butterfly process is performed concurrently enable it to execute FFT computation process in a very fast technique. FFT module

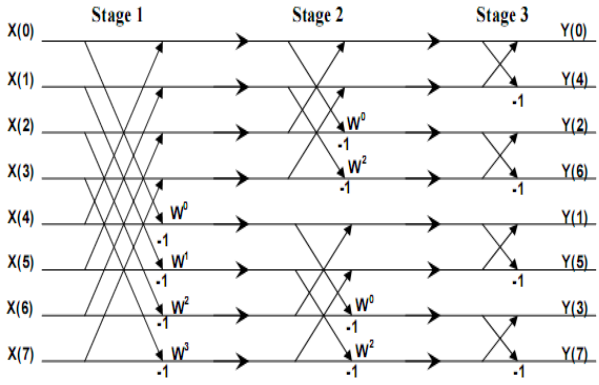

Fig. 8 8-point FFT flow graph using decimation-in-frequency

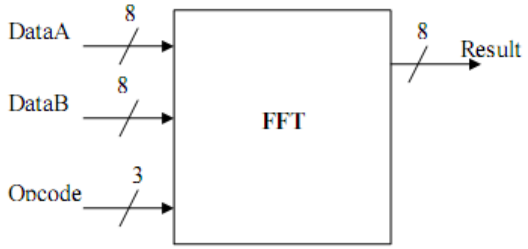

Fig.9 FFT module

The same block diagram as 8-point FFT is used to develop 8-point IFFT module. Input port such as DataA, DataB and Opcode is also used as well as Result for output port. The different between FFT and IFFT is that the IFFT module needs to divide with eight at the end of the result. Additional operation to handle this process is inserted at this module. The CP is a copy of the last N samples from the IFFT, which are placed at the beginning of the OFDM frame.

C. VHDL EMULATION RESULTS

In this part the emulation results for each component in an OFDM uplink/downlink system will be shown using VHDL simulator and then it can be implemented using FPGA.

Firstly the serial to parallel converter is used to convert the data from the serial form to the parallel form to introduce it to IFFT and it can be programmed using VHDL language as shown in fig.10.

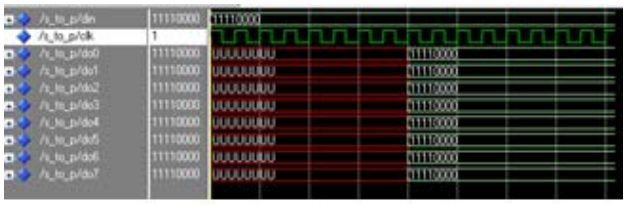

Fig. 10 serial-to-parallel converter emulation

The next block is the Binary Phase Shift Keying (BPSK) that is used as a simple type of complex digital modulation and as illustrated in fig.11 the bit(0) can be represented by a symbol (01) and the bit(1) is represented by a symbol(11).

Fig. 11 BPSK modulator emulation

As shown in fig.12 the emulation results for IFFT which is the inverse process of FFT which is actually explained.

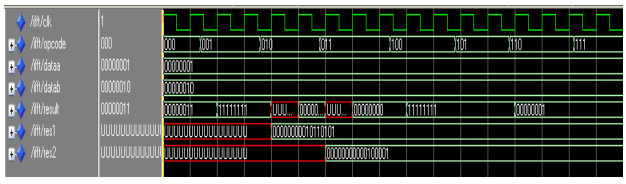

Fig. 12 IFFT emulation

Theoretically the cyclic prefix is a copy of the last N samples from the IFFT, which are placed at the beginning of the OFDM frame and this concept of cyclic prefix can be programmed using VHDL language as shown in fig.13

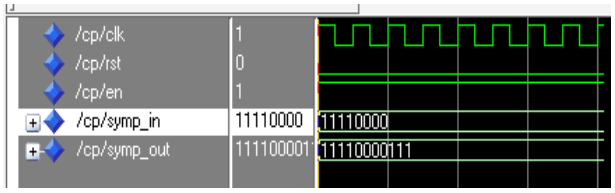

Fig. 13 Adding cyclic prefix emulation

In the receiver the inverse blocks for those of the transmitter will be obtained in the following figures. In fig.14 we can remove the cyclic prefix that is be added in the transmitter and it is clear that it is possible using VHDL code and the simulation result is matched with the theoretical concept.

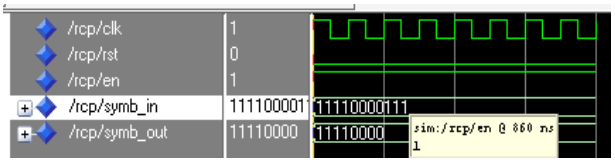

Fig. 14 Removing cyclic prefix emulation

The next block in the OFDM receiver is the FFT block and the emulation results can be illustrated in fig.15.

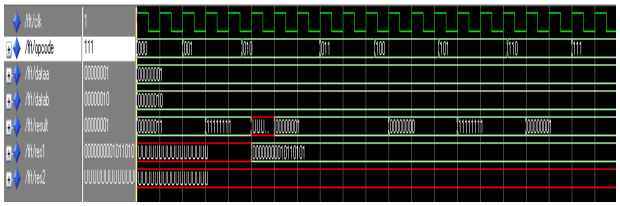

Fig. 15 FFT emulation

The inverse of BPSK block is the BPSK demodulator
In which that the bit (0) is reconstructed again from the symbol (01) and the bit(1) from the symbol(11) and the emulation result for this block is shown in fig.16.

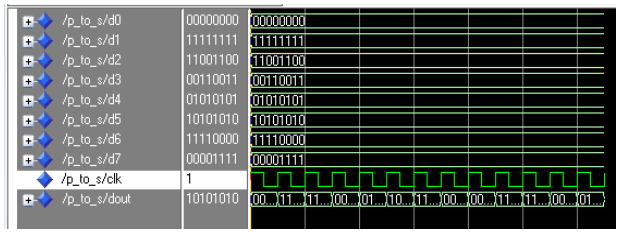

Fig.17 parallel-to-serial converter emulation

4. Conclusions

As mentioned in the objectives, a base band OFDM transmitter and receiver were successfully developed using VHDL codes and then it can be implemented using FPGA. The output from each module was tested using appropriate software to ensure the correctness of the output result. On the transmitter part there are four blocks which consists of mapper (modulation), serial to parallel, IFFT and parallel to serial block. Each of these blocks was tested using FPGAadvantages 7.2 software during design process. This is to ensure that the hardware module was correctly working when implemented in the FPGA hardware. During the implementation stage; the same process was done at the receiver part whereby each of the modules was tested during design process. The relation between SNR and BER for different systems for OFDM was introduced using Matlab software tools.

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