Implementing FFT Algorithms on FPGA

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Summary
The hardware description and modeling of digital signal processing (DSP) algorithms and applications for implementing on Field Programmable Gate Array (FPGA) chips are challenging issues. In this paper, some practical Fast Fourier Transform (FFT) algorithms including Cooley-Tukey, Good-Thomas, Radix-2 and Rader methods are modeled by Verilog hardware description language and their performance are compared in terms of chip area utilization and maximum frequency operation. The results of synthesizing FFT algorithms by ISE tool on XC3S5000 chip, from XILINX Inc. demonstrate that the Radix-2 FFT method uses the least number of Slices and the Cooley-Tukey and Good-Thomas approaches use the most number of Slices. In term of Flip-Flop utilization, the Cooley-Tukey and Good-Thomas approaches use less than the Radix-2 and Rader approaches. Furthermore, for all methods, the utilized FPGA chip area increases by increasing the number of FFT points. The Radix-2 is the fastest method for calculating FFT. The Good-Thomas method is faster than Cooley-Tukey where there are no coefficients between DFT blocks and the Rader method has the worst operating frequency on FPGA between all proposed FFT approaches.

Key words:
FFT Algorithms, Cooley-Tukey, Good-Thomas, Radix-2, Rader, FPGA, Verilog.

1. Introduction

The Orthogonal Frequency Division Multiplexing (OFDM) technique is one of the most important modulation approaches which is used in many schemes of communication systems such as wireless communications and networks [1,2]. The benefit of the OFDM approach rather than other modulation approaches is the efficient use of bandwidth using overlapping property. A typical OFDM system consists of two parts; receiver and transmitter. The receiver has four important blocks which are serial-to-parallel block, Inverse Fast Fourier Transform (IFFT), QAM table and the RF block. In the other hand, transmitter has RF block at the front end, Fast Fourier Transform (FFT), QAM table and parallel-to-serial block at the back end, shown in Figures 1(a) and 1(b).

One of the most important blocks of an OFDM system is the FFT block where the number of Fourier points is related to the OFDM symbols. There are various methods for implementing FFT block. The methods differ from maximum operating frequency, power consumption and chip area occupation viewpoints and performance evaluating of FFT approaches helps to implement OFDM receiver and transmitter systems according to required characteristics.

The hardware implementation of FFT approaches is a challenging issue where the digital signal processors (DSPs) and the field programmable gate array (FPGA) chips are two considering designing environments for implementing different schemes of FFT approaches.
Recently, the FPGA technology [3] is quit mature for digital signal processing applications [4] due to fast progress in very large scale integration (VLSI) technology. The FPGA devices provide fully programmable system-on-chip environments by incorporating the programmability of programmable logic devices and the architecture of gate arrays. They consist of thousands of logic gates and some configurable logic blocks which make them an appropriate solution for prototyping the application specific integrated circuits (ASIC) with dedicated architectures for specified digital signal processing applications. The introduction of Verilog Hardware Description Language (HDL) [5] provided a modeling and simulation environment for fast prototyping digital circuits and systems on FPGA.

Implementing of different schemes of FFT algorithms and applications received much attention in literature [6-10].
The aim of this paper is to model and hardware description of different schemes of FFT approaches including Cooley-Tukey, Good-Thomas, Radix-2 and Rader methods by Verilog HDL and realization of them on Xilinx FPGA chip. Then the performance of different algorithms is compared for chip area utilization and critical path time.

The rest of the paper is as follows; Section 2 describes four well-known FFT approaches using mathematical models and block diagrams. FPGA implementation of FFT approaches and comparing their performance are presented in section 3 and finally the paper is concluded in section 4.

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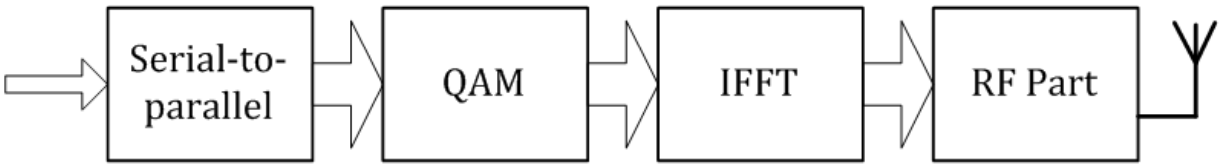

Fig.1(a) The receiver block of a typical OFDM based system

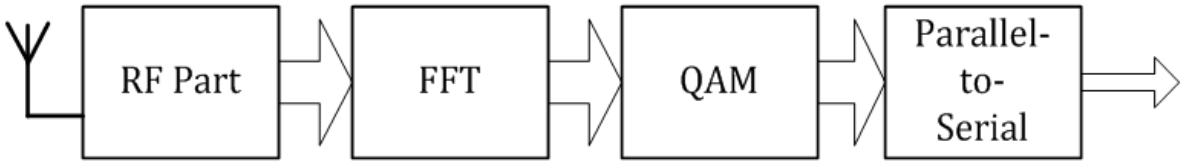

Fig. 1(b) The transmitter block of a typical OFDM based system

2. FFT Algorithms

In this section four common FFT methods including Cooley-Tukey, Good-Thomas, Radix-2 and Rader are described in details and the mathematical models of them are reviewed. For this, the mathematical background of each method is presented and the block diagram of each approach for N-point FFT operation is provided.

2.1 The Cooley-Tukey FFT Algorithm

This method was proposed by Cooley and Tukey [11] and generally is used for computing FFT. In this approach, the number of FFT points can be divided into two factors [12], N_1 and N_2 as follows;

$$N = N_1 \times N_2 \tag{1}$$

Input indexes, *n*, are obtained from following expression;

$$n = N_2 \times n_1 + n_2 \quad where \quad \begin{cases} 0 \le n_1 \le N_1 - 1 \\ 0 \le n_2 \le N_2 - 1 \end{cases} \tag{2}$$

Furthermore, the output indexes, *k*, are obtained from following expression;

$$k = k_1 + N_1 \times k_2 \quad where \quad \begin{cases} 0 \le k_1 \le N_1 - 1 \\ 0 \le k_2 \le N_2 - 1 \end{cases} \tag{3}$$

For example, when N is 15 then N_1 and N_2 are chosen to be 3 and 5 respectively. According to (2) and (3) input and output indexes are described by following expressions;

$$k = k_1 + 3k_2 \quad where \quad \begin{cases} 0 \le k_1 \le 2 \\ 0 \le k_2 \le 4 \end{cases} \tag{4}$$

$$n = 5n_1 + n_2 \quad where \quad \begin{cases} 0 \le n_1 \le 2 \\ 0 \le n_2 \le 4 \end{cases} \tag{5}$$

The block diagram of this method for N=15 is show 2.

2.2 The Good-Thomas FFT Algorithm

This method was suggested by good [13] and Thomas [14]. Considering Cooley-Tukey method shown in Figure 2, between two blocks at the front end and back end, some coefficients are placed. These coefficients can be eliminated by some assumptions and consequently for the same number of FFT points this method has less chip area occupation. Main supporting idea of this method is that N_1 and N_2, those are two-factor of N, are prime to each other. Input and output index mapping is done according to equations (6) and (7), respectively.

$$n = N_2 n_1 + N_1 n_2 \bmod N \quad where \quad \begin{cases} 0 \le n_1 \le N_1 - 1 \\ 0 \le n_2 \le N_2 - 1 \end{cases} \tag{6}$$

$$k = N_2.A.k_1 + N_1.B.k_2 \bmod N \tag{7}$$

$$where \quad \begin{cases} 0 \le k_1 \le N_1 - 1 \\ 0 \le k_2 \le N_2 - 1 \end{cases}$$

AN_2 and BN_1 satisfy following equations:

$$AN_2 \times N_1 \bmod N = 0 \tag{8}$$

$$BN_1 \times N_2 \bmod N = 0 \tag{9}$$

Furthermore, in Good-Thomas method, in addition to equations (8) and (9), below assumptions must be established at the same time:

$$AN_2^2 \bmod N = N_2 \tag{10}$$

$$BN_1^2 \bmod N = N_1 \tag{11}$$

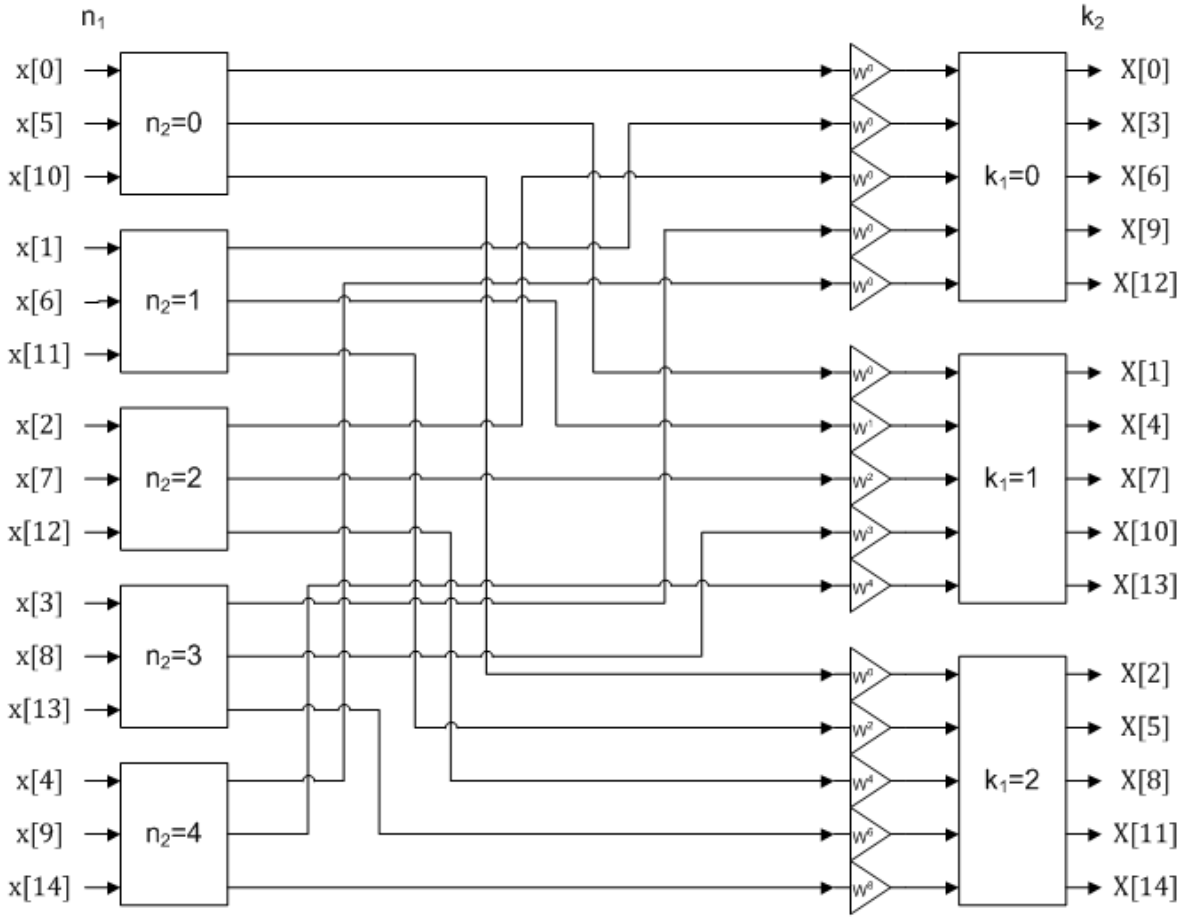

Fig. 2 The block diagram of 15-point Cooley-Tukey FFT Algorithm

For example for N=15, $N_1$and N_2 are 3 and 5 respectively and input and output indexes are:

$$n = 5n_1 + 3n_2 \bmod 15 \quad where \begin{cases} 0 \le n_1 \le 2 \\ 0 \le n_2 \le 4 \end{cases} \tag{12}$$

$$k = 10k_1 + 6k_2 \bmod 15 \quad where \begin{cases} 0 \le k_1 \le 2 \\ 0 \le k_2 \le 4 \end{cases} \tag{13}$$

The block diagram of Good-Thomas method for N=15 is presented in Figure 3.

2.3 The Radix-2 FFT Algorithm

This method is the subset of the Cooley-Tukey method. In this method, N_1 or N_2 is chosen to be 2 and the other one is $\frac{N}{2}$. It is assumed that N is a power of 2 [15-17]. As an example, for N=16, N_1=2 and N_2 is 8 and the following equations describe the implementing approach of this method.

The main expression of the Fourier transform is (14) and N=16 then $k = 0,1,2,...,15$.

$$Y(k)=\sum_0^{15} y(n)W_{16}^{nk} \qquad (14)$$

If odd and even parts of (14) would be separated, then (15) is:

$$Y(k)=\sum_0^{7} y(2n)W_{16}^{2nk}+\sum_0^{7} y(2n+1)W_{16}^{(2n+1)k} \qquad (15)$$

Considering $W_{16}^{2nk}=W_8^{nk}$ then:

$$Y(k)=\sum_0^{7} y(2n)W_8^{nk}+W_{16}^{k}\times\sum_0^{7} y(2n+1)W_8^{nk} \qquad (16)$$

Furthermore when $W_{16}^{k+8}=-W_{16}^{k}$ then:

$$Y(k)=\sum_0^{3} y(4n)W_8^{2nk}+W_8^{k}\times\sum_0^{3} y(4n+2)W_8^{(2n+1)k}+ W_{16}^{k}\times(\sum_0^{3} y(4n+1)W_8^{2nk}+W_8^{k}\times\sum_0^{3} y(4n+3)W_8^{(2n+1)k}) \qquad (17)$$

and eventually;

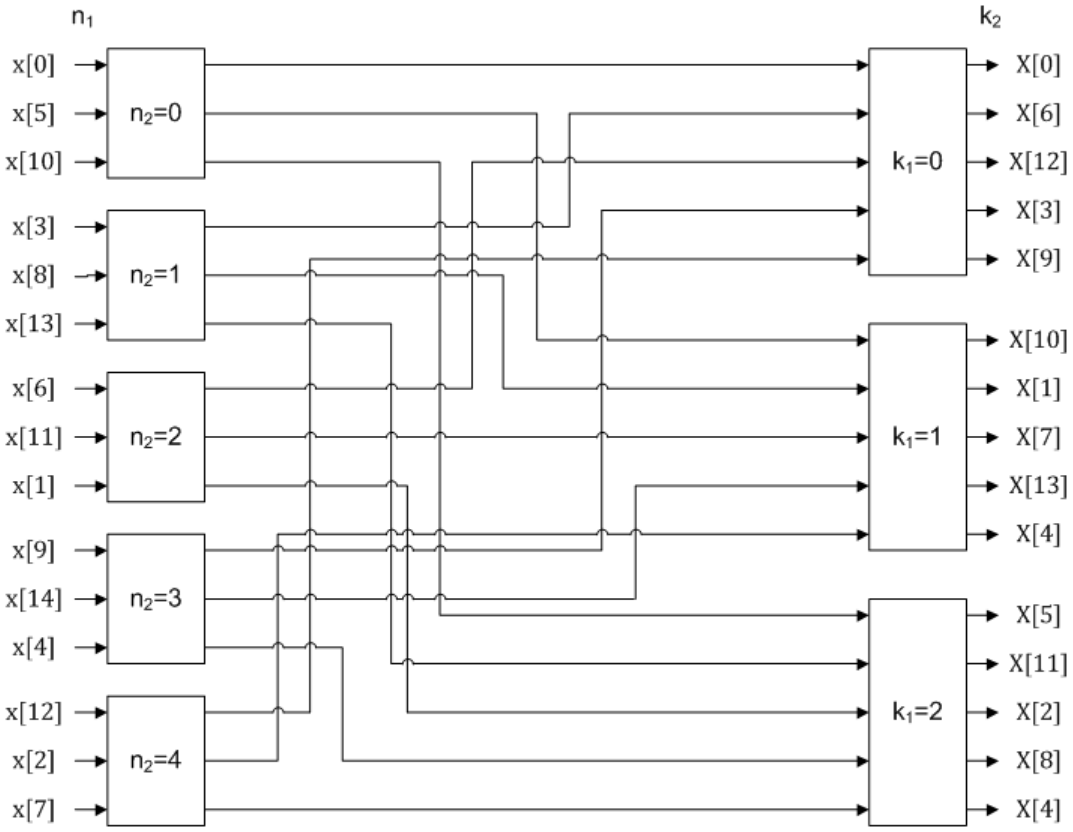

Fig. 3 The block diagram of 15-point Good-Thomas FFT Algorithm

$$\begin{aligned}Y(k)=&\sum_0^{1} y(8n)W_2^{nk}+W_{16}^{4k}\times\sum_0^{1} y(8n+4)W_2^{nk}+\\ &W_{16}^{2k}(\sum_0^{1} y(8n+2)W_2^{nk}+W_{16}^{4k}\times\sum_0^{1} y(8n+6)W_2^{nk})+\\ &W_{16}^{k}(\sum_0^{1} y(8n+1)W_2^{nk}+W_{16}^{4k}\times\sum_0^{1} y(8n+5)W_2^{nk}+\\ &W_{16}^{2k}(\sum_0^{1} y(8n+3)W_2^{nk}+W_{16}^{4k}\times\sum_0^{1} y(8n+7)W_2^{nk}))\end{aligned} \qquad (18)$$

The block diagram of Radix-2 FFT method for N=16 is presented in Figure 3.

2.4 The Rader FFT Algorithm

This method was introduced by Rader [18, 19] where it is assumed that N is prime. According to [20, 21], each prime number has one or more primitive root, here called *p*. Selecting one of the primitive root and using (19), the input index sequence can be obtained so that the FFT operation is calculated with the cyclic convolution. The output indexes of the convolution are 1 to N-1 and the 0 index must be calculated separately.

$$p^n \bmod N \qquad 0 \le n \le N-2 \qquad (19)$$

For example when N=17, the primitive roots are 3, 5, 6, 7, 10, 11, 12, and 14. Choosing number 3 as primitive root the order of inputs is obtained from Table 1.

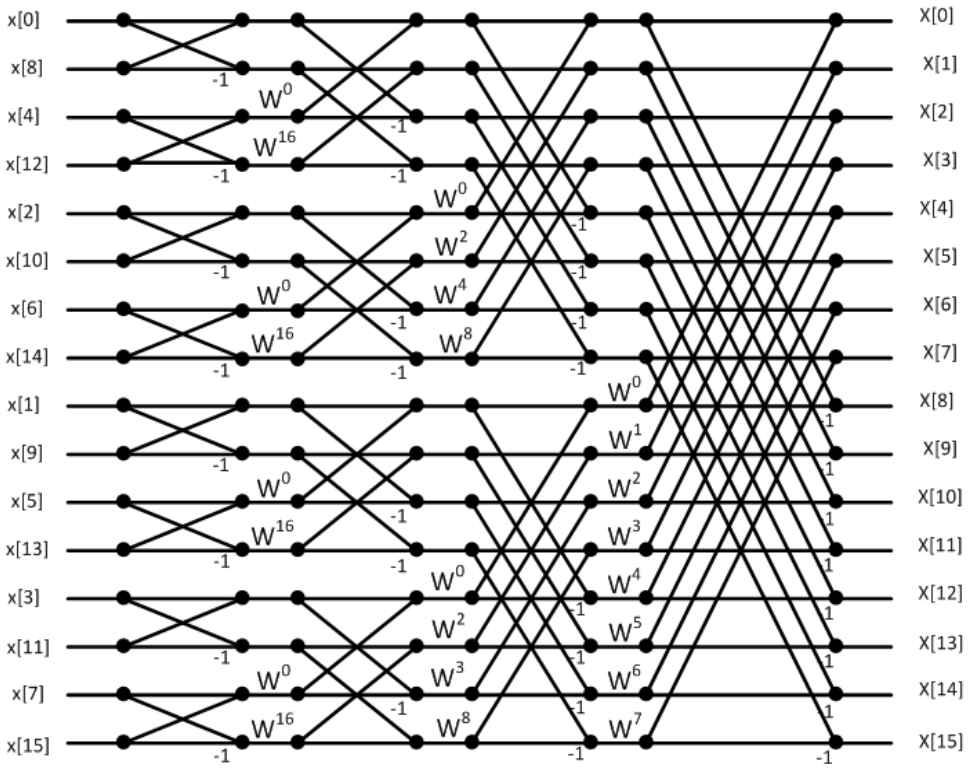

Fig. 4 The block diagram of 16-point Radix-2 FFT Algorithm.

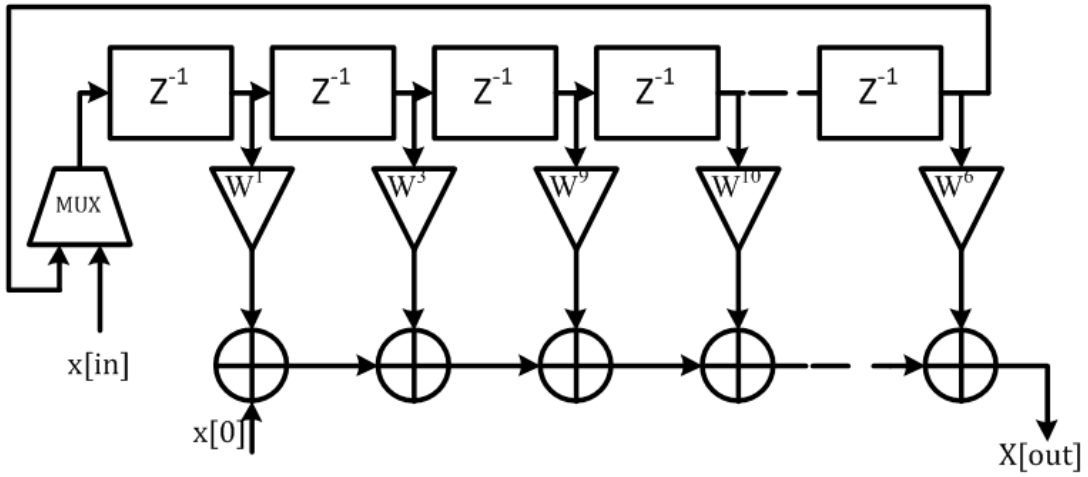

Fig. 5 Cyclic convolution of Rader FFT Algorithm.

In addition to input indexes, the coefficients must be arranged like inputs indexes.
Figure 5 shows the cyclic convolution part of Rader FFT method. The entries come into the rotational part and go forward with each clock pulse.
In the other hand, these entries are multiplied by the coefficient weights and added with x[0] finally to make the output.

Table 1: The Index Number of Rader FFT Algorithm

n	Index number	n	Index number
0	1	8	16
1	3	9	14
2	9	10	8
3	10	11	7
4	13	12	4
5	5	13	12
6	15	14	2
7	11	15	6

3. FPGA Implementing and Comparison Study

In this section the simulation results of realization the FFT algorithms on a single FPGA chip are presented and the performances of FFT algorithms are compared in terms of chip area utilization and maximum operating frequency on target chip. The FFT algorithms are modeled by Verilog HDL and implemented on XC3S5000 chip from Xilinx Inc. [14]. The specification of the test bench chip is listed in Table 2. The ISE software is used for synthesize and simulation of Verilog codes.
In the proposed study, the prime numbers for Rader method are 7, 17, 31 and 61, for radix-2 algorithm the two-powered numbers are 4, 8, 16, 32 and 64 and for Cooley and Good methods the numbers 10, 15, 20 and 63 are considered.
The results of FPGA chip area occupation including number of utilized Slices and Flip Flops by FFT algorithms are compared in Figures 6 to 8.
As shown in Figures 6 and 7, the Radix-2 method uses the least number of Slices. While the Cooley and Good approaches use the most number of Slices. In term of Flip-Flop utilization, the Cooley and Good approaches use less than Radix-2 and Rader approaches. Furthermore, for all methods, the chip area utilization is increased by increasing the number of FFT points.

The reason that Cooley has less chip area rather than Good method is that in Good method, in addition to DFT block, some coefficients are placed between DFT blocks.
In Figure 8, performance of FFT methods is compared for maximum frequency operating viewpoint. As shown, the Radix-2 is the fastest method for calculating FFT due to less processing in the calculating path. The Good-Thomas method is faster than Cooley-Tukey where there are no coefficients between DFT blocks. The Rader method has the worst operating frequency due to calculating time in this method takes more time.

Table 2: The specification of test bench chip

Slices	33280
Slice Flip Flop	66560
LUTs	66560

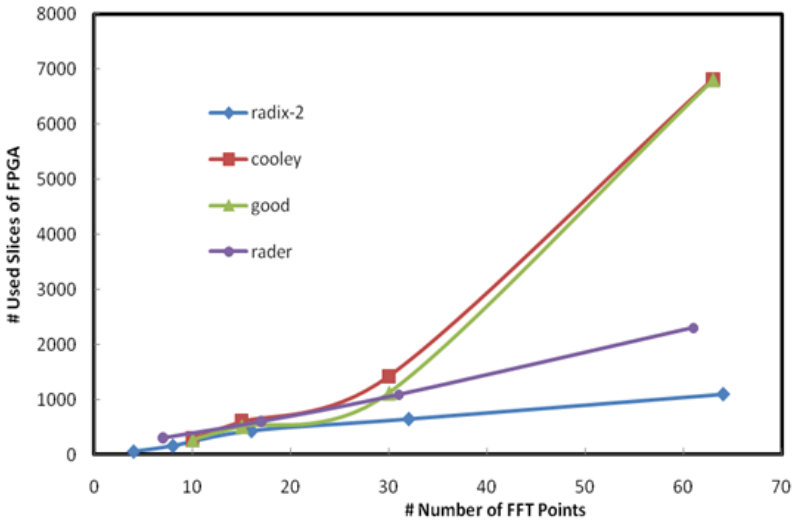

Fig. 6 Comparing the FFT methods for Slice utilization.

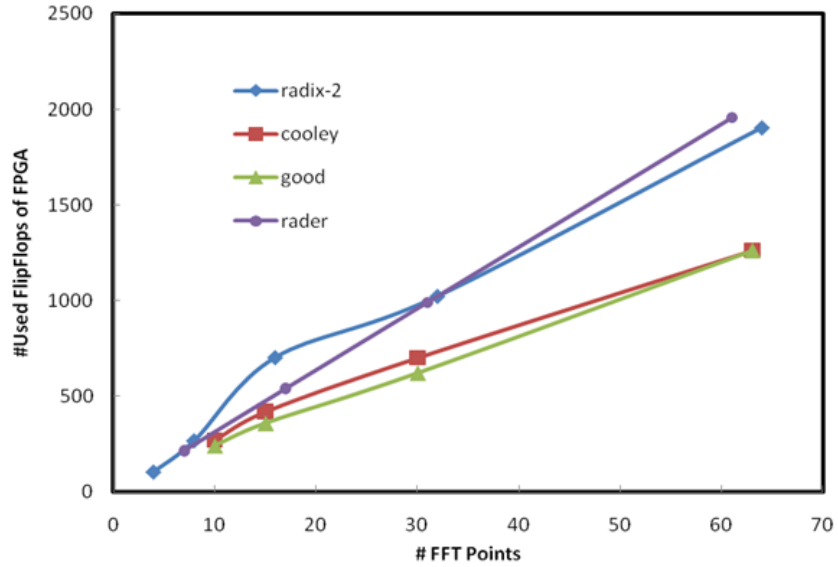

Fig. 7 Comparing the FFT methods for Flip-Flop utilization.

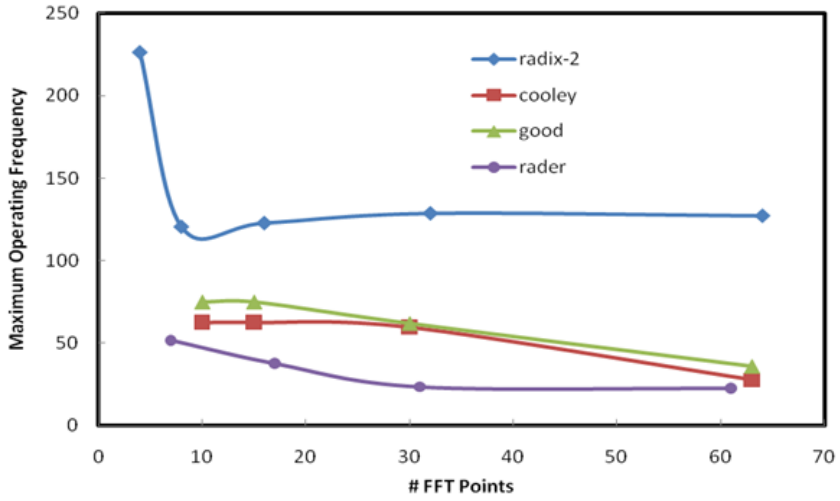

Fig.8 Comparing the FFT methods for maximum operating frequency.

4. Conclusion

Modeling and hardware description of some FFT approaches such as Cooley-Tukey, Good-Thomas, Radix-2 and Rader FFT algorithms by Verilog hardware description language and realization of them on Xilinx FPGA chip was proposed. The results demonstrated that the Radix-2 FFT method used the least number of Slices and the Cooley-Tukey and Good-Thomas approaches used the most number of Slices.

The Good-Thomas method was faster than Cooley-Tukey and the Rader method had worst operating frequency on FPGA between all proposed FFT approaches. In term of Flip-Flop utilization, the Cooley-Tukey and Good-Thomas approaches used less than the Radix-2 and Rader approaches. Furthermore, for all methods, the utilized FPGA chip area increased by increasing the number of FFT points.

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