A Pseudo 12-bits 8,33MS/s Charge Redistribution Successive-Approximation ADC in CMOS 65nm for Image Sensors

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Summary
A new charge redistribution Successive Approximation A-D Converter (SA ADC) potentially suitable for array implementation in CMOS Imagers is presented. The performances achieved exceed the performances of the actual sensors in terms of both resolution and image quality. The reached sampling rate is more than sufficient for mobile applications (30fps for a pixel array of 5Megapixels). The converter is designed in CMOS 65nm technology and the low power constraints have been respected, the consumed silicon area was optimized in order to fit into the actual sensors die size with no major changes affecting the other blocks, thus this new conversion system will be readily usable in image sensors of next generation with pitches less than or equal to 1.1µm.

Key words:
CMOS Image Sensors, column-level ADC, Successive Approximations ADC, Differential Charge Redistribution DAC, Fringe capacitor.

1. Introduction

At the early days of CMOS imaging, the main markets for these devices were low resolution, budget cameras. With extensive research and growth in the field, CMOS is seeking to capture more of the top end digital imaging market. As for the image sensor technology, more than 24 megapixels and smaller than 1.4µm pixel pitch have been realized for the digital still cameras and the mobile-phone cameras, respectively. These technologies have to be developed without increasing die and optical sizes (cost and portability constraints [1]). The roadmap recently unveiled for CMOS Image Sensor (CIS) is announcing ever smaller pixels, after 1.4µm pixel pitch, demos with a pitch of 1.1µm were presented, and it also announces the future generation of pixels with 0.9µm pixel size.This progress has resulted in a great strain on sensors analog readout electronics, and, in particular, on their ADC architecture. The role of the ADC architectures is that of enabler for the required specification. Certain converter architectures are optimized for certain parameters. For example, sigma delta architectures are optimized for power efficiency while flash converters are optimized for speed. Various other architectures, like SAR, are optimized for varying combinations of speed, dynamic performance and power. Therefore, it is by the selection of the architecture that individual specifications are often achieved.

Many types of ADCs for CIS have been reported, whose integration range from chip-level to pixel-level. For low resolution video rate applications, a single high-speed ADC can be used [2]. The ADC is shared by all pixels in the imager, and converts only one pixel at a time. This serial approach is no longer feasible in modern high resolution CMOS Image Sensor, as millions of pixels need to be converted all in a few milliseconds. Instead, a column-parallel approach is often employed, where an ADC is dedicated to each column (or a few columns) of pixels, and all ADCs operate in parallel. In this case, low power and low-to-medium speed ADCs can be used.

The benefit of this approach is that, it allows to quickly extract data off the sensor. Additionally, each ADC has a much longer time to operate on a sample, thus allowing longer settling times, lower noise, and higher accuracy. Hence, the ADCs are small and the speed-per-ADC requirement is low. Most CMOS Imaging sensors Column-parallel ADCs use single-slope integrating- ADC architectures. Only the comparator and the counter need to be in the column pitch. The devices can generate the ramp-reference signals and clocks outside the column, and all the ADCs can share these signals and clocks.

Reported parallel ADC types include single slope [3], cyclic [4], sigma-delta (ΣΔ) [5], and successive approximation (SA) [6]. Pixel-level integration has also been proposed. As the ADC would take up valuable space,

Manuscript received April 5, 2012
Manuscript revised April 20, 2012

a compact architecture with minimal amount of transistors is preferred. Such ADC types include among others the known ΣΔ [7] and the Multi-Channel Bit Serial (MCBS) [8] structures.
The future direction of Mobile CMOS Imaging will be either towards larger image-formats or high dynamic range imaging which require much faster readout rates. It can be easily understood that the most currently used column-parallel counter ADC appears to be at its limit of performance. Migrating to faster architectures such as SAR in the column in conjunction with column sharing can result in a more scalable system. Alternatively migrating to a column serial architecture enables faster readout rates and the possibility of higher resolutions.

This work introduces an alternative technique which combines column sharing and parallel ADC architecture, based on SA approach and designed for 10 ns per conversion step, which is equivalent to 30 frames per second in a high resolution camera (2 624 columns x 1 968 lines, pseudo-12-bits, one ADC for every 32 columns) suitable for mobile applications. This kind of converters is also well adapted regarding their low level power consumption [9].
The design of such an ADC is a very challenging task. In particular, three design targets must be simultaneously met. First, it is imperative that the read-out channels have a uniform response compared to one another. Any difference in response between the column ADCs will be highly visible as vertical stripes in the produced image. These artifacts are even visible if the magnitude of the non-uniformity is lower than that of other temporal noise sources in the read-out circuit. Second, the required chip area for each readout column should be minimized, since the column ADC should have the same width as a pixel on the chip, which is typically less than 1.4μm. Third, the power consumption of the column ADC should be minimized with an eye towards mobile applications. The design of ADC strongly determines how well the above-mentioned design targets can be met.
The paper is organized as follows. Section II describes a background of noise in CMOS Image Sensors, and justifies the principle of the presented conversion architecture. Section III illustrates the architecture of the sensor. The actual circuit implementation and configuration are detailed in sections III and IV. Simulation results are provided in section V. Section VI lists the advantages of the proposed architecture when compared with the previous works and finally, the section VII concludes the paper.

2. Theory: Noise in CMOS Image sensors

In the CMOS Image Sensor the noise depends on the signal amplitude. Two noises are expected to influence the Signal-to-Noise-Ratio (SNR) of the ADC converter in a CIS. The first is the read noise, linked to the acquisition chain and independent from the signal level; it predominates for low-level signals (low lighting of the sensor) and directly impacts the analog equivalent of the Least Significant Bit (LSB). The second is the shot noise which is directly related to the signal level and it is proportional to the square root of the number of electrons received by the sensor [10]. On the analog signal side, once the read noise has become smaller than the shot noise, the signal-to-noise ratio (SNR) is equal to $\sqrt{N}$ [11], where N represents the number of electrons received by the sensor.

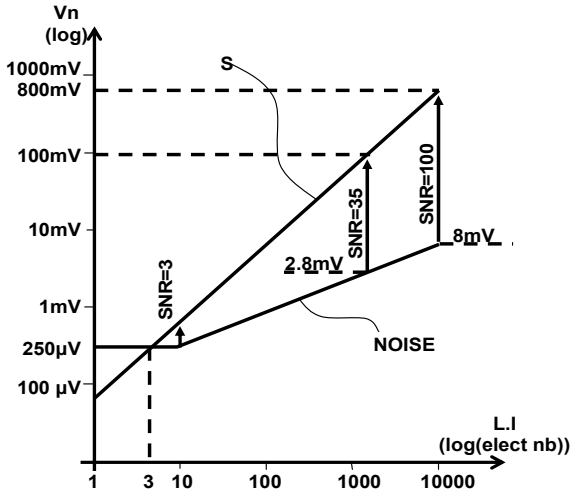

Fig. 1 Analogue output voltage versus lighting intensity in a pixel of a CMOS Image Sensor, SNR values and noise level [12].

Fig. 1. shows the output voltage, the SNR and the noise level versus lighting intensity of a pixel in a CIS. The level of signal 'S', representing the output voltage of a pixel follows an approximately linear course of constant slope in logarithmic scale, according to the light intensity. It is clear that as soon as the signal 'S' becomes greater than the read noise, noise 'NOISE' represents the shot noise which is proportional to $\sqrt{N}$; the preponderating contributor to noise 'NOISE' is the shot noise. As a result, SNR also has a $\sqrt{N}$ variation [11]. In other words, for low level signals, quantization and thermal (flicker) noises are limiting, and for high level signals shot noise in limiting.
To be able to properly exploit the results, the resolution of the analog to digital converter must be selected according

to this read noise. In practice, a resolution that approximately corresponds to the read noise for low-level signals is selected. However, for high-level signal, the noise level becomes such that several bits provided by the converter are no longer significant.

It has already been provided to take into account the shot noise in an image sensor by varying the slope of the ramp of a ramp converter. This amounts to settling, for high-level signals, for a coarser resolution than with a low-level signal. Actually, the ramp slope increases along time over measurement period. Such a solution is already described [13]; it exploits the shot noise phenomenon to provide an ADC with a ramp which is variable along time. A variable-ramp solution does not increase the number of bits provided by the converter, but it provides a benefit in time by decreasing the number of quantization levels. Further the response time of the converter comparators depends on the ramp slope. The variable ramp is thus likely to generate a quantization error.

This paper provides, in successive approximation converter architecture, having a conversion step increasing along with the analog input voltage value. This step is in relation with the noise expected on the corresponding signal. This enables decreasing the conversion time comparing with a single-ramp converter.

3. ADC circuit description

The proposed design, shown in Fig. 2, provides a method of analog-to-digital conversion over 12-bits of an analog signal that includes: comparing the amplitude of the analogue signal with a threshold representing the amplitude of the full scale analogue signal divided by 2^3=8 and then performing an analog-to-digital conversion by successive approximations of the analog signal over 9-bits to obtain:

- The 9 Most Significant Bits (MSB) of a binary word over 12-bits if the result of the comparison step indicates that the amplitude of the input signal is greater than the threshold,
- The 9 Least Significant Bits (LSB) of the 12-bits binary word otherwise.

The choice of 3-bits for the coarse comparison is not random; it is based on the noise profile of CMOS Imagers (detailed in section II), the limitation between the respective areas where both the read noise and the shot noise predominates respectively corresponds to $\frac{V_{ref}}{2^3}$.

Other choices like having 4-bits for the coarse comparison and 8-bit DAC array are possible, this will provide more area saving, but it will be inappropriate for the targeted application in a CIS, the approximation made depending on the noise will be erroneous.

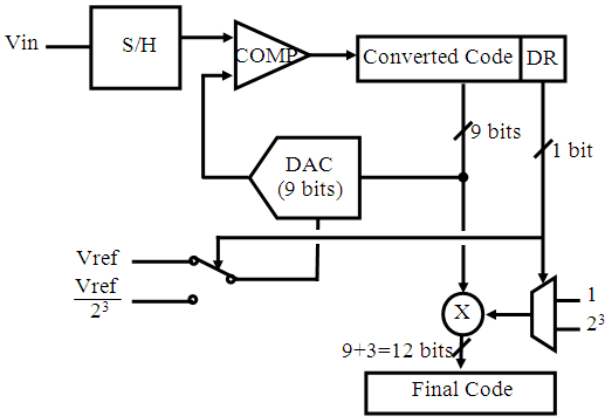

Fig. 2 Successive Approximation ADC block diagram.

The resolution of the converter does not vary: 12-bits for the global converter and 9-bits for the "effective" converter. The main components of the designed differential SA ADC include two charge redistribution DACs, a single comparator (used for both comparison and conversion), successive approximation registers, and some logic to control capacitor switches. Fig. 3. shows a schematic overview of the SA ADC topology, which can be divided into four parts: the DAC, the comparator, the SAR and the output stage.

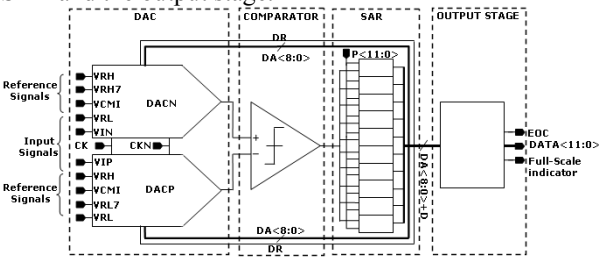

Fig. 3 SA ADC architecture.

Reference signals mentioned above (which determine the two full-scales of the converter) are set to correspond to the dynamic of the pixel.

3.1. Charge redistribution DAC:

A switched-capacitor DAC architecture based on the charge redistribution principle is used. The scheme is fully differential; in fact there are two identical branches at the input of the comparator, each based on a set of 2^9 binary-weighted capacitors. The schematic of a branch is shown in Fig. 4.

There are several design considerations for the DAC which is the most critical part in the overall design. Inaccuracy in capacitor sizing will cause Differential Non

Linearity (DNL) errors. Inaccuracy is greatest for the smallest value capacitor but in larger capacitors it causes the most DNL [14]. Capacitor sizes are determined by matching, quantization and kT/C thermal noise constraints. Where k is the Boltzmann constant, T denotes the absolute temperature and C corresponds to the pixel parasitic capacitance.

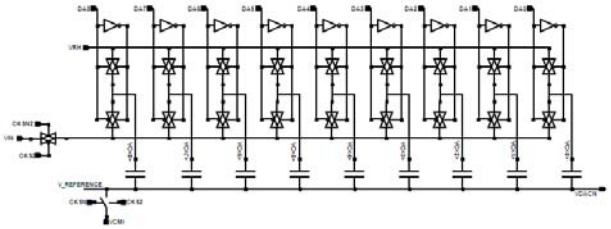

Fig. 4 Schematic of a branch from the proposed charge redistribution DAC.

For better performances, fringe capacitors are used and to maximize the matching between the capacitors, a careful attention to layout is required: the common-centroid capacitor arrays are used with symmetric connections to minimize the parasitic capacitors.

3.2. Comparator

The comparator is responsible for resolving small, near an LSB voltage, inputs into full-scale digital values. The LSB corresponds to a 12-bits performance. A high-sensitive comparator is required for fast conversion. The delay of the comparator must be stable with the variation of input voltages. As a result, the trade–off between power dissipation and the speed should be considered. With these considerations, a three stage cascade regenerative track-and-latch comparator with high-gain is selected. The schematic of the proposed comparator is shown in Fig. 5.
Design considerations for the comparator were centred between high speed, 12-bits resolution, low power consumption and a reduced offset (offset cancellation scheme is not shown in Fig 5). The size of the transistors, especially the input differential pair of each stage, was selected after several Monte-Carlo simulations.
It must be noticed that the same comparator performs the first comparison for full scale selection and the comparisons for the conversion.

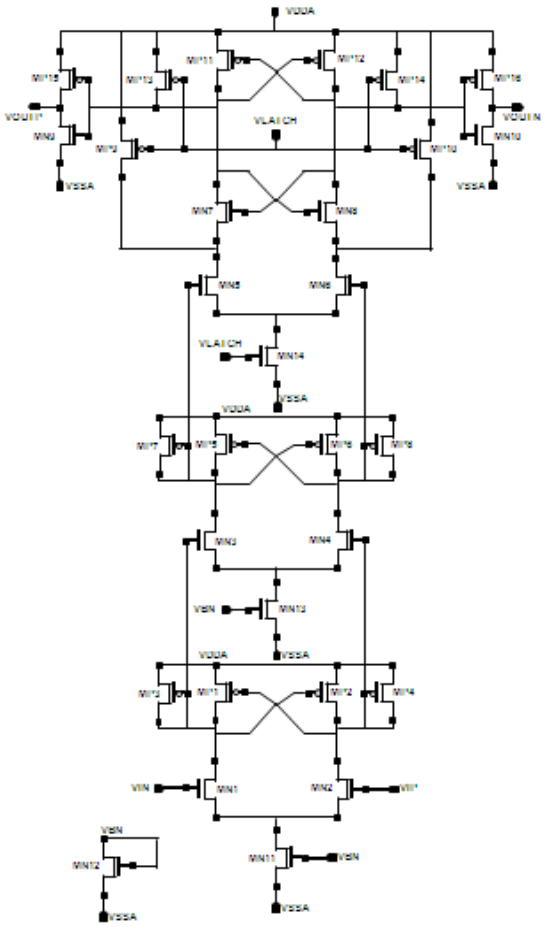

Fig. 5 Schematic of the proposed comparator.

3.3. Successive approximation Registers (SAR)

This block implements the binary search algorithm and drives the DACs. It determines the value of each bit of the control word in a sequential manner, based on the output of the comparator. The register stages are composed of RS latches arranged to have a 10-bits register: the first bit is a flag bit R used to refer to the comparison result (performed before the conversion begins, it is equal to 1 if the amplitude of the analog signal is greater than the threshold and is equal to 0 otherwise), and the 9 other bits are obtained from the conversion.

3.4. Output stage

The converter includes a digital element as output stage, capable of adding, in case where the flag bit DR is equal to 1, three random LSBs to the conversion result, and in case where DR is equal to 0, three MSBs (set to 000) to

the conversion result. Thus, the final 12-bits word is formed by digital processing.
The output stage mentioned above is used only for simulations. It will be removed from the sensor, and instead an appropriate algorithm in the digital part of the sensor will be implemented.

4. ADC circuit configuration

The performed conversion starts by sampling the input signals and then determining an amplitude range where these signals to be digitized can be found. If Vref is the full-scale value, the conversion range is equal to Vref $x2^{3(DR-1)}$, flag bit DR is set to 0 if the amplitude of the analog signal is smaller than or equal to the threshold and value 1 otherwise, then the conversion by successive approximation takes place.
The circuit uses periodic pulses as control signals; each conversion needs 12 steps, the corresponding timing diagram for a conversion is given in Fig. 6.

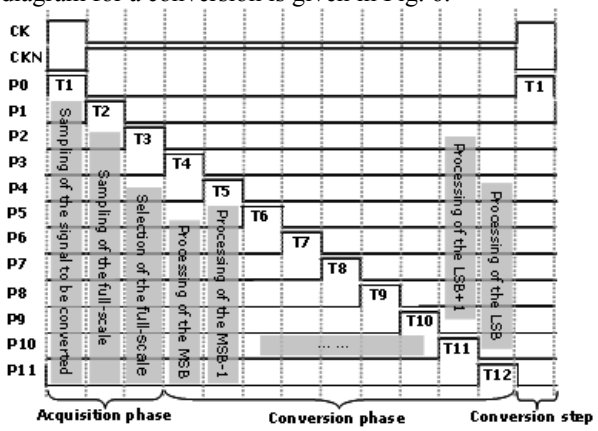

Fig. 6 Timing of the proposed ADC.

- The acquisition phase which takes three clock cycles corresponding to P0, P1 and P2 is summarized in the table-I bellow:
  - P0=1: Sampling of *VIN* & *VIP*, DACs outputs are equal to:

$$V_{DACN}(n) = V_{DACP}(n) = VCMI \quad (1)$$

  - P1=1: Sampling of the full-scale, DACs outputs are equal to:

$$V_{DACN}(n+1) = VRH7 + VCMI - VIN \quad (2)$$

$$V_{DACP}(n+1) = VRL7 + VCMI - VIP \quad (3)$$

  - P2=1: Selection of the effective conversion full-scale, DACs outputs are equal to:

$$V_{DACN}(n+2) = \frac{VRH - VRI}{2} + VRH7 + VCMI - VIN \quad (4)$$

$$V_{DACP}(n+2) = \frac{VRL - VRJ}{2} + VRH7 + VCMI - VIP \quad (5)$$

VRI and VRJ are selected depending on the comparison between *VADCN* & *VDACP:*
- If *VDACP* > *VADCN* : *VRI=VRH7*, *VRJ=VRL7*
- If *VDACP* < *VADCN* : *VRI=VRL*, *VRJ=VRH*

Table 1: Acquisition phase

CK	DR	P0	P1	P2	COMMENT
0	-	1	0	0	Sampling of *VIN* & *VIP* in all the *VC<i>* All *DA=0*
1	0	0	1	0	Sampling of the full-scale, Initialisation of DR, All *DA=0*
1	0	0	0	1	Selection of the effective conversion full-scale depending on the comparison between *VADCN* & *VDACP* If *VDACP* > *VADCN*
1	1	0	0	1	Selection of the effective conversion full-scale depending on the comparison between *VADCN* & *VDACP* If *VDACP* < *VADCN*

Table-I is elaborating the first three comparisons of signal with 3-bit coarse comparison to decide whether DR is equal to 0 or 1, and then to assign the corresponding voltage references to the DAC. This implemented in the converter using the circuit of Fig. 7. which is connected to the V_REFERENCE input of the DAC.

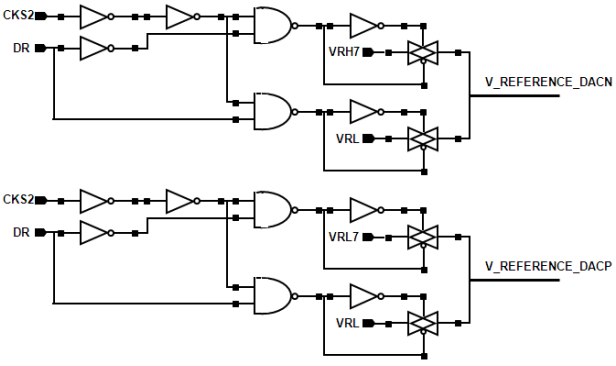

Fig. 7 Implementation of the full scale selection circuit.

- The conversion phase takes 9 clock cycles, the conversion by successive approximation begins when P3=1, the MSB is set to 1 and then the input signal is compared to 100 000 000 corresponding to half the full-scale, the value of the MSB is chosen depending on the comparison result, then the MSB-1 is set to 1,

the same process is repeated till the value of the LSB is found.

- If the selected full-scale is FS1: *DR=1* (*VRL<VIN< VRH7 & VRL7 <VIP<VRH*), DACs outputs are equal to:

$$V_{DACN} = \frac{\sum_{i=0}^{8} C_i (VRH - VRL)}{C_{total}} + VRH7 + VCMI - VIN \quad (6)$$

$$V_{DACP} = \frac{\sum_{i=0}^{8} C_i (VRL - VRH)}{C_{total}} + VRL7 + VCMI - VIP \quad (7)$$

- If the selected full-scale is FS2: *DR=0* (*VRH7<VIN< VRH & VRL <VIP<VRL7*), DACs outputs are equal to:

$$V_{DACN} = \frac{\sum_{i=0}^{8} C_i (VRH - VRH7)}{C_{total}} + VRH7 + VCMI - VIN \quad (8)$$

$$V_{DACP} = \frac{\sum_{i=0}^{8} C_i (VRL - VRL7)}{C_{total}} + VRL7 + VCMI - VIP \quad (9)$$

C_i: are the capacitors connected to bits equal to 1.
C_{total}: the sum of capacitors connected to the reference signals.
Supposing the conversion result (over 9-bits) is $B_8B_7B_6B_5B_4B_3B_2B_1B_0$, depending on the value of DR, the output stage gives the conversion result over 12-bits:

- If DR=0, then the final result will be $000B_8B_7B_6B_5B_4B_3B_2B_1B_0$.
- If DR=1, then the final result will be $B_8B_7B_6B_5B_4B_3B_2B_1B_0XXX$ (XXX is a random 3-bits code).

5. Simulations results

The pixel value has a fixed range, commonly between 0V and 1V, the chosen dynamic range for the converter is equal to 1.024V to reach saturation if pixel illumination is high, and the ADC has an input common mode voltage VCMI equal to 1.55V.
The reference signals must values which are symmetric toward VCMI (Fig. 3.), so the reference voltages are equal to:

$$VRH = 2.062V; VRH7 = 1.934V; VRL7 = 1.166V; VRL = 1.038V$$

$$VRH - VRL = 1{,}024V$$

$$VRH - VRL7 = VRL7 - VRL = \frac{VRH - VRL}{8} = 0{,}128V.$$

The generation of these reference voltages is achieved using an existing ramp DAC with a resistor ladder (of the actual single slope ADC), the absolute matching requirements leads to precision lower than ½ LSB (for the 12-bits resolution).
If the conversion is performed in the FS1, the LSB is equal to LSB1=2mV, otherwise if the conversion is performed in the FS2, the LS is equal to LSB2=250µV.
At 30frames/s, the required ADC time for each conversion (which takes 12 clock cycles) is 120ns corresponding to a frequency of 8. 33 MHz, a clock frequency of 100 Mhz is used here.
A compromise between the quantization noise, the kT/C noise and matching requirements in the DAC gives the value of the unitary capacitor: kT/C noise must be lower than the quantization noise, if C_{total} is the equivalent capacitor of each DAC (C_{total} =511 x $C_{unitary}$), so

$$\frac{kT}{C_{total}} = \frac{V_{LSB}^2}{12} \quad (10)$$

For matching requirement we added a factor of 7 in the previous equation. C_{total} is the equal to:

$$C_{total} = \frac{7 \times 12 \times kT}{V_{LSB}^2} = 6.8\,pF \quad (11)$$

The unitary capacitor is equal to:

$$C_{unitaryl} = \frac{C_{total}}{511} = \frac{6.8\,pF}{511} = 13\,fF \quad (12)$$

Each ADC was laid out in 44.8µm (corresponding to 32 column with 1.4µm pitch).
The concept of successive approximation is verified. Fig. 8. shows the differential output signals of the DACs corresponding to the inputs of the comparator.

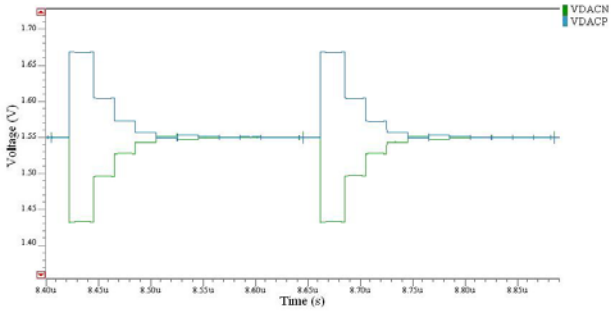

Fig. 8 Illustration of voltage convergence in the SA ADC.

For evaluation purposes, the input signals of the SA ADC (corresponding to reset voltage and useful signal voltage) are set to be symmetric toward the input common mode voltage (VCMI) and to sweep the entire full scale, in order to obtain the equivalent of a ramp varying from code 1 to code 4095 corresponding to the 2^{12} codes of a 12-bits converter. The simulation results are shown in Fig. 9.
The first result represents the input signals with the four voltage references for the DACs, the second is an analogue representation for the converted 9-bits data, and

the third is an analogue representation for the converted data over 12-bits.

The curve (d) corresponds to flag bit DR which controls the digital block responsible of adding three MSBs (set to 000) or three LSBs (set to 111) as detailed in Fig.10. The binary representation of the codes generated over 12-bits shows that when DR=0, the codes may be symbolized by 000XXXXXXXXX and when DR=1, they may be symbolized by XXXXXXXXX111.

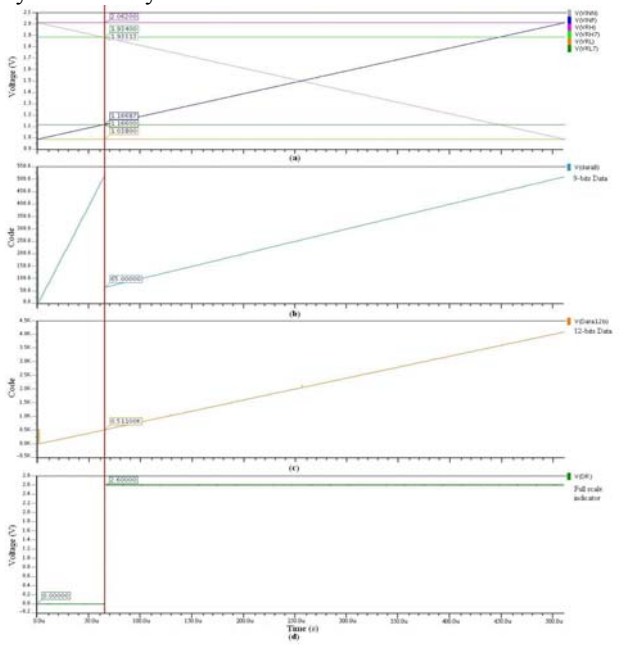

Fig. 9 Simulation results of SA ADC. (a) Input signals, reference voltages and the two Full-Scales. (b) Generated ramp over 9 bits (c) Generated ramp over 12 bits (d) Transition between the two Full-Scales.

A zoomed view of the transition between the two full-scales and the corresponding binary codes are shown in Fig. 10.

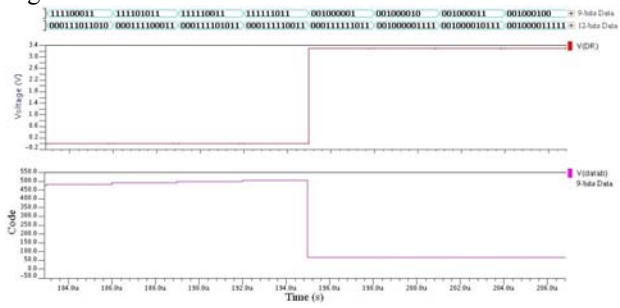

Fig. 10 Zoomed view of the transition between the two Full-Scales.

In Fig. 10. it is shown for DR=0/1, how the MSB/LSB bits are set. In this simulation, the LSB bits are fixed to 111. It was mentioned that the LSB bits are randomly selected to some value for DR=1 to avoid missing codes. A suitable algorithm will be added to implement this functionality.

The simulations were operated using a 2.8V analogue supply and a 1.2V digital supply. Power dissipation in each ADC was estimated to be 1.3548mW which is a reasonable value when compared to the actual sensor (using a column parallel single slope converter); this power is nearly all consumed by the biasing of the comparators each at 80μA.

Specifications of the static linearity, including integral nonlinearity (INL) and differential nonlinearity (DNL), were measured based on the sinewave code density testing method [14]. The measured DNL and INL at 8.33 MS/s are shown in Fig. 11. and Fig. 12.

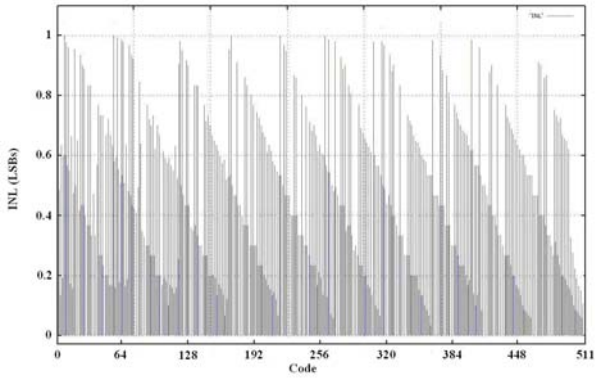

Fig. 11 INL plot for SA ADC with input increasing by ½ LSB per conversion step.

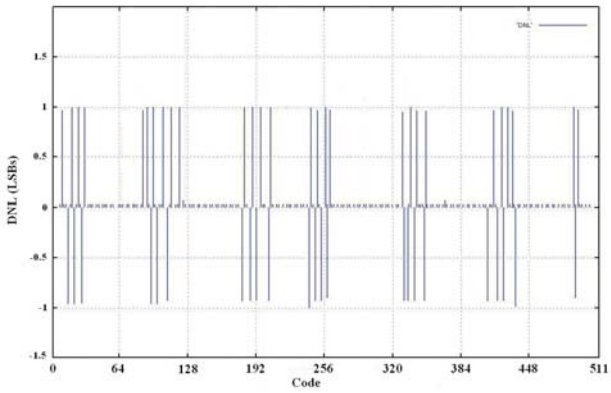

Fig. 12 DNL plot for SA ADC with input increasing by ½ LSB per conversion step.

It is noticed that the INL errors are mainly between the limits of 0 and +1 LSB, which corresponds after normalization to plus or minus 1/2 LSB, usually reported in other works. The maximum DNL is +1 LSB/-1 LSB, and t he maximum INL is +1.1LSB/0 LSB.

6. Assets of the proposed conversion architecture

As compared with a variable ramp converter [13], a difference is that no conversion is performed with the converter over the entire range (12-bits). Thus, not only does this provide a time gain, but also does it simplify the converter architecture and thus the surface area that it takes up.

Almost all CMOS Imagers for mobile applications using a single-slope ADCs have an average ADC resolution between 10 and 11-bits [15, 16, 17], this work gives the equivalent of a ramp of a 12-bits ADC , with the same timing and size constraints. The overall timings of the sensor using this new conversion architecture are set to correspond to timings of actual sensors, in other words, each of the 82 converters used in this architecture performs 32 times faster than the actual ramp converter (a conventional single-rate single slope ADC).

The pixel value has a fixed range; when dealing with dark scenes, the pixel values will only be using a fraction of this range. If this voltage is directly forwarded to the ADC, the full dynamic range and resolution of the converter will not be used, therefore ideally this voltage should first be amplified to occupy the full range, and then be forwarded to the ADC. The amplification value is calculated by a statistical based digital block, which constantly monitors the images produced. So the analogue block provides some form of programmable gain amplification which can be controlled by the digital block.

To achieve the desired analogue signal gain, when dealing with simple ramp architectures, it is only required to change the slope of the counter ramp while leaving the SRAM ramp unchanged, however for the proposed architecture, applying an analogue gain to the conversion chain is also feasible, by changing the value of the LSB and so by changing the DACs references values depending on the required gain, Fig. 13 shows simulation results for an analogue gain equal to 2. The line in blue is the analogue representation of the converted data corresponding to the gain x1 (codes from 1 to 4 095 over the entire full-scale). The line in pink represents the conversion results for an analogue gain x2 (codes from 1 to 4 095 over the first half of full-scale, for the remaining half, the flat curve corresponds to the saturation zone).

The switched-capacitor converter used in this design enables, as compared with usual switched-capacitor converter, to increase the resolution by 3-bits at the cost of a small surface area (one bit register for DR, and the full scale decision circuit connected to the DAC). In fact, in an usual switched-capacitor converter, adding 1 resolution bit requires multiplying the surface by approximately 8 (the number of resistors and capacitors used for the voltage subdivision is multiplied by 2, which results in an approximately four times larger surface area, and each subdivision must be on the order of twice as accurate, which results in an approximately double surface area for component matching reasons). Increasing the resolution by 3-bits requires a surface area factor of more than 500 (8^3) [12].

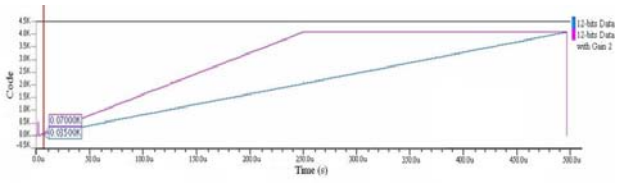

Fig. 13 Simulation results for an analogue gain equal to 1 and an analogue equal to2.

Using a conventional 12-bits SA ADC will never fit in the available silicon area of the sensor which is 44.8µm×447.48µm for each converter. The 9-bits SA ADC in this implementation with 12-bits matching is 64 times bigger compared a generic 9-bits SA ADC with 9-bits matching components. So, the area savings in this design is a factor of 8 as compared to a generic 12-bits SA ADC.

7. Conclusion

A new conversion architecture based on a charge redistribution Successive Approximation Analogue-to-digital converter is proposed for CMOS Imagers for mobile applications. It's intended for the next generation imagers with pitches less than 1.4µm. The apparent resolution of the converter is 12-bits, it is obtained from a 9-bits converter, and it varies depending on the pixel noise value.

To overcome the challenge of designing a converter per column with small pitches, where the available area for layout is very critical, the new converter will process the data from 32 columns of the pixel array and the layout will be extended to 32 columns instead of 1 column. Comparing with the actual sensors of STMicroelectronics (5Megapixels, CMOS 65nm) for the same available silicon area and timings, the proposed converter provides a higher resolution. A minimum number of changes will occur to the overall architecture of the sensor; the only concerned is the readout block in its conversion and memorization parts.

The converter is designed in CMOS 65nm technology, and will be implemented in a 5Megapixel sensor, at a sampling rate of 8.33MS/s. The simulation results show that the constraining requirements in resolution, speed, size and low power consumption are met.

Acknowledgments

The authors would like to thank the analogue team from Imaging Division at STMicroelectronics Rabat, L. Simony and M. El Hachimi, for their technical assistance in this work, and the CNRST Rabat for their support.

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