Testing of RF Differential Low Noise Amplifiers using Built-In-Test circuits

[1] J.Kaviyarasan, [2] S.Suvitha

[1] P.G Scholor, S.A Engineering College, Chennai-77.
[2] Assistant professor/ECE, S.A Engineering College, Chennai-77.

Abstract
This paper presents an efficient, low-cost, built-in test (BIT) circuit for radio frequency differential low noise amplifiers (DLNAs). The BIT circuit detects amplitude alterations at the outputs of the DLNA, due to parametric or catastrophic faults, and provides a single digital Pass/Fail indication signal. A triple modular redundancy approach has been adopted for the BIT circuit design to avoid possible yield loss in case of a malfunctioning test circuitry. This technique evaluated on typical CMOS RF DLNA and simulation result is presented.

Keywords
Built-in-test (BIT), design for testability, LNA testing, RF testing, triple modular redundancy.

1. Introduction

AS consumer demands for low cost telecommunication circuit's increase, testing cost becomes a major concern being a large portion of the total production cost. Especially in the case of high frequency/RF integrated circuits (IC) the cost of testing is prohibitive. In this area, high cost dedicated automatic test equipments (ATEs) are used to measure performance characteristics of the circuit under test (CUT) and compare them against predefined limits that are called specifications. Testing cost becomes a major concern being a large portion of the total production cost. Especially in the case of high frequency/RF integrated circuits (IC) the cost of testing is prohibitive. In this area, high cost dedicated automatic test equipments (ATEs) are used to measure performance characteristics[1] of the circuit under test (CUT) and compare them against predefined limits that are called specifications .Although these measurements are simple, they require a variety of test resources, which along with the long test application time, increase further the manufacturing cost. However, BIT schemes are not always suitable for the implementation of direct measurement techniques, due to the high hardware overhead that is required. The objective of the alternate test methodology is to find a suitable test stimulus and to predict circuit characteristics accurately from the corresponding alternate test response [2].

Manuscript received April 5, 2012
Manuscript revised April 20, 2012

Although many alternate test techniques exploit BIT schemes to support testing [3], still the elaboration of test responses is accomplished off chip.

2. The Built-In-Test Circuit

The principle under the proposed DLNA-BIT circuit is based on the following generalized observation: catastrophic and parametric faults produce output amplitude alterations on at least one of the output nodes of a differential circuit. The DLNA-BIT topology outline is presented in Fig. 1. The BIT circuit is driven directly from the outputs of the DLNA and provides a single digital PASS/FAIL signal. It consists of two main sub circuits: a) the first one is the Amplitude Alterations Detector (AAD) and b) the second is the Timing Difference Discriminator (TDD). The first sub circuit monitors the outputs of the DLNA and provides two digital signals, TEST1 and TEST2, which perform a transition from VDD to ground. Obviously, integrating BIT circuits in RF design is a challenge that needs further investigation. High frequency analog design is extremely vulnerable to deteriorations caused by the additional test circuitry and test related pads. Moreover, the deviation from normal operation are appearing in a continuous form.

a. The Amplitude Alterations Detector (AAD)
The topology of the Amplitude Alterations Detector is presented in Fig. 2. It is driven by the differential outputs of the DLNA. The basic building components ofAADare four sensing transistors [two pMOS (M5, M7) and two nMOS (M6, M8)] and the corresponding current mirrors attached to them [two pMOS current mirrors (transistors M15, M16 and M19, M20) and two nMOS current mirrors (transistors M13, M14 and M17, M18)].
In the presence of a fault, the compression of the amplitude, on at least one of the oscillator outputs, results in a reduction of the current that flows through the corresponding PMOS "sensing" transistor (M7 or M6). Consequently the corresponding NMOS current mirror (M11/M12 or M13/M14) fails to discharge its dedicated node (S1 or S2) and thus the output of the corresponding

buffer (BUF-1 or BUF-2) remains high, indicating fault detection as shown in Fig. 3. The gates of the sensing transistors are fed by the outputs of the DLNA so that each output (RFout and RFout) drives the gates of a single pair of nMOS/pMOS sensing transistors (M6/M5 and M8/M7 respectively The operation of the AAD subcircuit will be further analyzed for the fault free and the faulty DLNA cases.

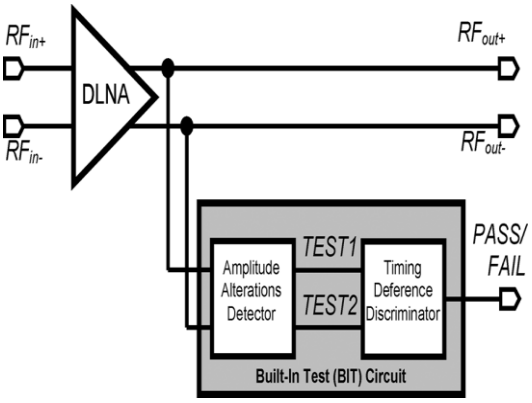

Figure 1.Proposed BIT-DLNA topology

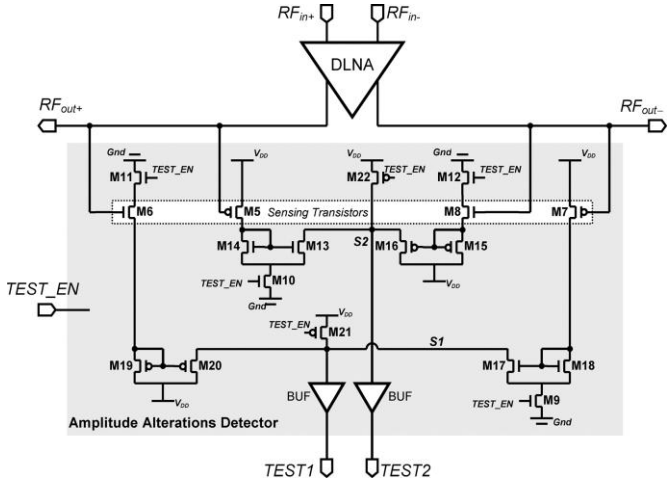

Figure 2. Amplitude alteration detector

During the test application phase, the DLNA is driven by a sinusoidal differential signal of a given frequency and amplitude. In general, the test stimulus signal must only satisfy two prerequisites: a) it must be a suitable signal to support the BIT circuit in order to provide a high fault coverage b) it must be an appropriate signal so that its application does not induce any malfunction into the functional circuit.

Fault Free DLNA: In the fault free case, the transient output of the DLNA is a differential sinusoidal signal, according to the performance characteristics of the circuit, as it is shown in

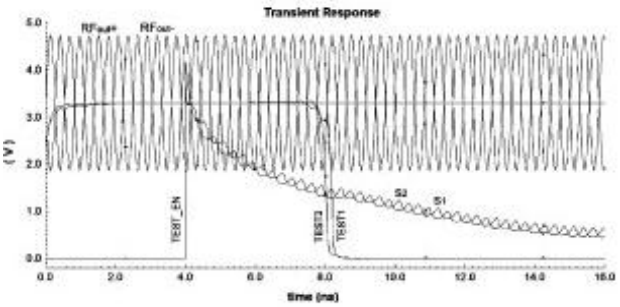

Figure 3. Fault free case: DLNA and BIT response

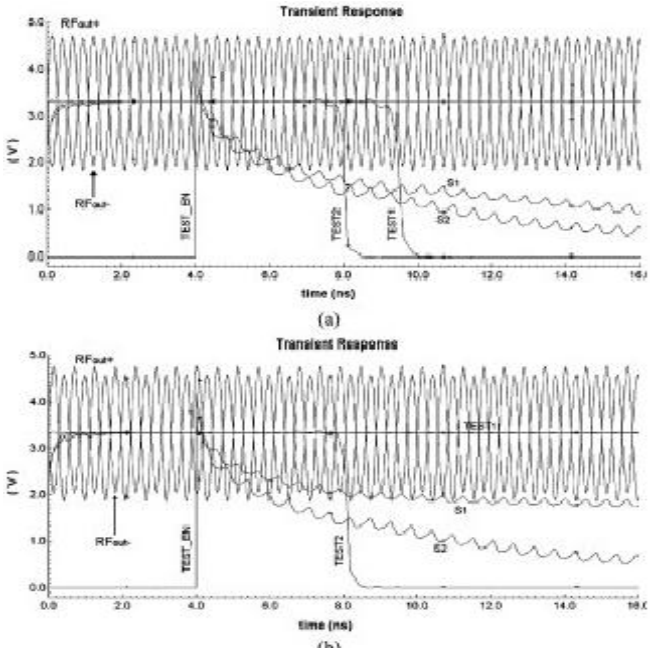

Figure 4. Faulty case: DLNA output amplitude attenuation and BIT responses.

b. Timing Difference Descrminator

Before the presentation of the Timing Difference Discriminators special situation must be taken into account. In the fault free case, possible device mismatches in the DLNA induce small Amplitude alterations that subsequently introduce small delays between the transition times of TEST1 and TEST2 signals[6]. The same stands due to device mismatches in the AAD sub circuit. The D inputs of the Flip-Flops are permanently high, tied to VDD. Before test mode activation the Flip-Flops outputs are preset to low with the use of a reset signal. Thus, the PASS/FAIL signal is initially high. As reset signal the complement of the TEST_EN signal is used.

In the presence of a fault in the DLNA or “acceptable” device mismatches, one of the TEST1, TEST2 signals turns to low earlier than the other. Without loss of

generality, let us consider that this is the TEST1 signal. Consequently, the output of the corresponding NOR1 gate rises to high triggering the pertinent Flip-Flop. The TEST1 and TEST2 signals drive the NOR gates. Since both signals are initially high, the outputs of the NOR gates are initially low. The output of each NOR gate triggers the CLK input of a D Flip-Flop. The D inputs of the Flip-Flops are permanently high, tied to vdd.

Before test mode activation the Flip-Flops outputs are preset to low with the use of a reset signal. Thus, the PASS/FAIL signal is initially high. As reset signal the complement of the TEST EN signal is used[7].Then, the output of the corresponding NOR2 gate remains permanently low and the same stands for the output of the related Flip-Flop.. the falling edge of the TEST2 signal, with respect to TEST1, the second Flip-Flop may be also triggered or not. In the first case, the falling edge of the TEST2 arrives earlier than the rising edge of the Delayed TEST1 signal (this is a small delay on TEST2 related to device mismatches). [5].Then, the output of the NOR2 gate goes high (since both TEST2 and Delayed TEST1 signals are low) and the second Flip-Flop is triggered raising its output to high.

C. BIT Circuit Reliability Improvements

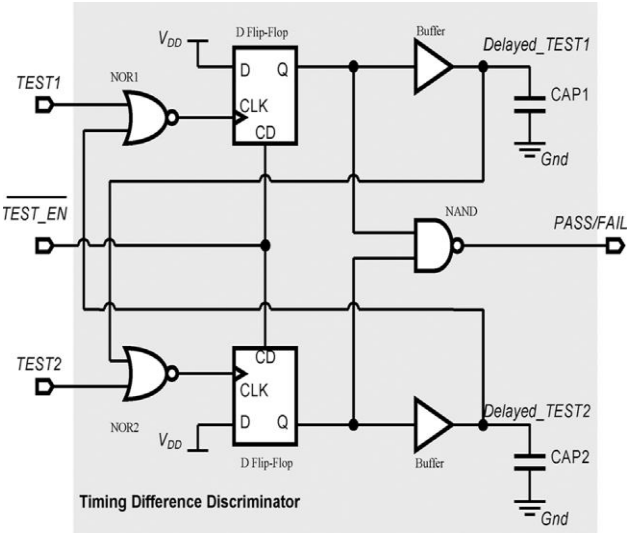

Figure 5. Timing difference discriminator

A special care should be given to the fact that the BIT circuit is also prone to faults or device mismatches. This may result in an undesirable yield loss since a malfunctioning BIT circuit may report a fault free DLNA as faulty.

To overcome this situation self testable or fault tolerant BIT circuit is required. In this work we have adopted a triple modular redundancy (TMR).

3. LNA-BIT Design Issuse And simulation Results

The effectiveness of the proposed test strategy has been evaluated using the DLNA structure presented in Fig.6. The DLNA has been designed in a 0.35 m SiGe CMOS technology (12mV) for GSM 1800 receiver applications.

The architecture selected for the DLNA, is based on the inductive common-source degeneration topology[8],[9]. Differential LNA structures are in general immune to the common-mode interference from substrate or supply perturbations [10]. In the DLNA of Fig. 12, inductors L3/L4 and capacitors C3/C4, form the input impedance matching network, while L1/L2 and C1/C2 form the necessary LC output impedance for the tuning frequency of 1.8 GHz.

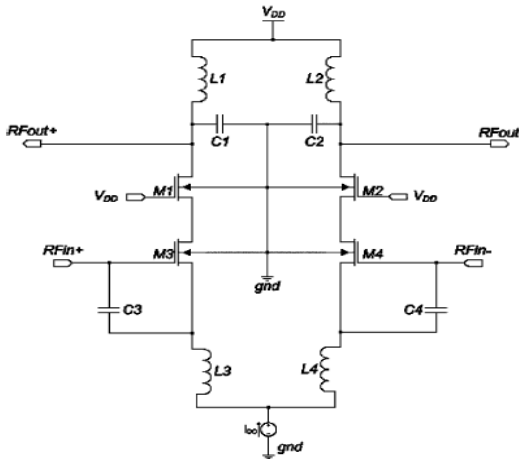

Figure 6. The Differential Low Noise Amplifier under consideration.

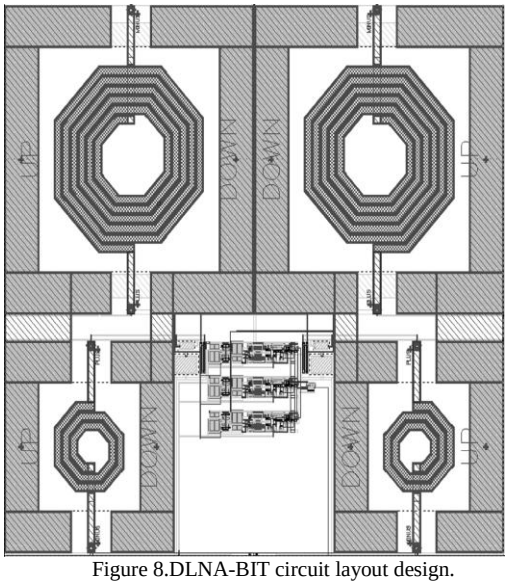

Figure 8.DLNA-BIT circuit layout design.

The layout of the whole circuit is shown in Fig. 8. Layout design techniques to cope with device mismatches have been taken into account in the design[14].The area occupied by the TMR version of the BIT circuit corresponds to only 3.75% of the total DLNA silicon area.

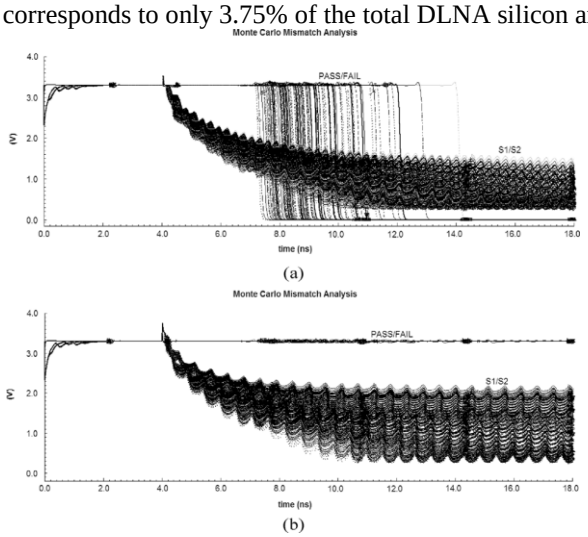

Figure 8. Monte Carlo simulations for the BIT response in a) the fault-free and b) a faulty DLNA case.

Moreover, Monte Carlo mismatch simulations (using the statistical models of the technology) have been performed on the BIT circuit for the fault free and all possible faulty cases to assure that there is no yield loss due to erroneous fault indications related to these mismatches[15]. In Fig. 9(a) the fault free Monte Carlo simulation is illustrated while in Fig.9(b) an indicative Monte Carlo simulation for a faulty case is shown. The overall fault coverage of the proposed BIT circuit in this design is 90.4%.

4.Conclusion

We propose a Built-In Test (BIT) circuit suitable for testing differential LNA circuits. The test circuit is capable to detect fault related amplitude alterations at the outputs of a differential LNA and discriminate fault free from faulty circuits. The response of the BIT circuit is a single digital PASS/FAIL indication signal.

The fault model under consideration consists of catastrophic faults due to manufacturing defects and parametric faults due to device parameter deviations related to manufacturing process variability. Yield loss, related to false indications by a malfunctioning BIT circuit, is avoided by adopting the triple modular redundancy approach for the test circuitry. The proposed BIT scheme has been designed in a standard RF CMOS technology and evaluated by extensive simulations using as test vehicle a typical differential LNA topology for GSM receivers. According to the simulation results, a high fault coverage can be achieved at a very low silicon area. Consequently, suspicious DLNA circuits can be easily identified early in the production cycle (e.g., at the wafer or die level) reducing the total manufacturing cost. Finally, our experiments proved that the BIT circuit is capable to work for a wide range of input signal frequencies (at least up to 5 GHz).

References

[1] P. Variyam, S. Cherubal, and A. Chatterjee, "Prediction of analog performance parameters using fast transient testing," IEEE Trans. Computer- Aided Des. Integr. Circuits Syst., vol. 21, no. 3, pp. 349–361,2002.

[2] J. Dabrowski and J. Gonzalez-Bayon, "Mixed loop-back BIST for RF digital transceivers," in Proc. Int. Symp. Defect Fault Tolerance VLSI Syst. (DFT), 2004, pp. 220–228.

[3] M. Cimino, M. De Matos, H. Lapuyade, T. Taris, Y. Deval, and J.-B.Bégueret, "A low-power and low silicon area testable CMOS LNA dedicated to 802.15.4 sensor network applications," in Proc. Int. Conf.Electron., Circuits Syst. (ICECS), 2006, pp. 383–386.

[4] R.G.J. Arendsen, "Defect based test selection for large mixed-signal circuits," Ph. D. thesis, University of Twenty, the Netherlands,

[5] S.Dragic, Margala M., "A Versatile Built_in CMOS Sensing Device for Digital Circuit Parametric Test", Submitted to IEEE Transactions on Instrumentation and Measurement

[6] Dabrowsky, J., "BiST Model for IC RF International Symposium on Defect and Fault Tolerance in VLSl Systems, Nov. 2003, pp. 295-302. E. Sacchi, I. Bietti, F. Gatta, F. Svelto, and R. Castello,

[7] "A 2 dB NF, fully differential, variable gain, 900 MHz CMOS LNA," in VLSI Circuits, 2000. Digest of Technical Papers. 2000 Symposium on. Mohd. Zinol Abidin Abd Aziz(2004). "Low Noise Amplifier Circuit

[8] Design for 5 GHz to 6 GHz", Proceeding of the 2004 IEEE – 0-7803- 8671-X/04/-RF and Microwave conference, October 5-6, Subang, Selangor, Malaysia. 81300 Skudai, Johor, Malaysia will be deleted from the biography.

[9] X. Fan, M. Onabajo, F. O. Fernandez-Rodriguez, J. Silva-Martinez, and E. Sanchez-Sinencio, "A current injection built-in test technique for RF low-noise amplifiers," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 7, pp. 1794–1804, 2008.

[10] Y. Xing, "Defect-oriented testing of mixed-signal ICs: Some industrial experience," in Proc. IEEE Int. Test Conf., 1998, pp. 678–687.

[11] M. Sachdev and J. P. de Gyvez, Defect-Oriented Testing for Nano- Metric CMOS VLSI Circuits. New York: Springer, 2007.

[12] L. Dermentzoglou, Y. Tsiatouhas, and A. Arapoyanni, "A design for testability technique for differential RF low noise amplifiers,"

[13] A. Hastings, The Art of Analog Layout. Englewood Cliffs, NJ: Prentice-Hall, 2005.

[14] W. B. Vinnakota, Analog and Mixed Signal Test. Englewood Cliffs, NJ: Prentice-Hall, 1998.

[15] J.-Y. Ryu, B. C. Kim, S.-T. Kim, and V. Varadarajan, "Novel defect testing of RF front end ," in Proc. 9th IEEE Int. Mixed-Signal Testing Workshop, 2003, pp. 31–34.

Kaviyarasan.j received the B.E. degree in Electronics and communication Engineering from Trichy engineering college under the Anna university, Chennai, 2010. He is currently pursing M.E- communication Systems in S.A Engineering college,Chennai.His area of interests is low power VLSI, signal integrity design for high speed digital system.