Design of Mesh & Torus Topologies for Network-on-Chip Application

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Abstract:
Network-on-Chip (NoC) is a general purpose on-chip communication concept that offers high throughput, which is the basic requirement to deal with complexity of modern systems. In Network on chip topology design is one of the significant factors that affect the net delay of the system. In this paper mesh topology and torus topology are compared in terms of network delay for a given NOC application using Xillinc 9.1c.

Keywords*:*
Network on Chip, Topology, Router

I. INTRODUCTION

The Network-on-Chip (NoC) is a communication centric interconnection approach which provides a scalable infrastructure to interconnect different IPs and sub-systems in a SoC [5, 7, 15]. Moreover, NoCs can make SoCs more structured, and reusable, and can also improve their performance [5, 8]. However, solutions to overcome performance limitations in NoCs are yet to be presented.
Many topologies with different capabilities have been proposed for NoCs including Mesh [8], Torus [7], Octagon [9], SPIN [4], and BFT [10]. In such cases, one of the main goals is to improve network performance by providing better static topological characteristics such as diameter and average inter-node distance [8]. However, when designing communication architecture, it is vital to consider the effect of physical design constraints such as wire routing, wiring density, and power consumption. The authors of [11] showed that in contrast to normal beliefs, on chip interconnections suffer from certain physical limitations which lead to great performance reduction. According to their results, when we consider these physical design constraints, higher dimensional networks may have serious limitations. Moreover, these constraints cause designers to decline the number of communication channels or wire bandwidth. If we compare mesh and torus topology in the contest of delay then torus topology is better as compared to the mesh topology i.e. time required to route the packet in torus topology is less as compared to the mesh topology.
This paper organised as follows, Section II deals with related work, Section III gives the simulation scenario of mesh topology and torus topology and Section IV deals with result Section V represents graph and finally Section VI represents conclusion and Section VII represents references.

II. RELATED WORK

In the previous work various topologies such as mesh, torus, folded torus, BFT, SPIN etc are compared according to various parameters such as power consumption, delay, area, throughput. In this paper we are designed mesh topology and torus topology and delay required for that topologies are find out. In this paper we are take 3x3 mesh topology and 3x3 torus topology. There are 9 routers are connected to each other and C marks IP cores, Switch addresses indicate the XY position in network as shown in fig. 1 and fig. 2.

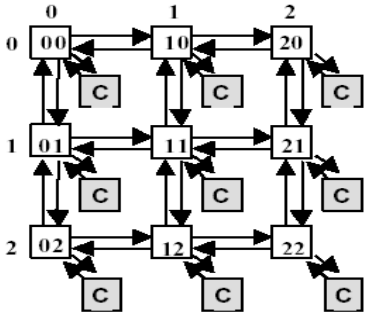

Figure 1. 3x3 Mesh NoC structure.

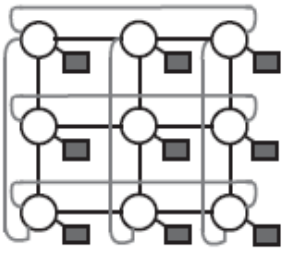

Figure 2. 3x3 Torus NoC structure.

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In this topologies we have to first design the router. Router is the heart of NoC architecture. In this paper we are using the packet of 160 bits. The packet is divided into flits. Each packet contains four flits each flit is of 40 bits. The first flit contains the source and destination address. In this we are used router having certain blocks as follows:

1] FIFO
2] Cross-bar
3] Arbiter

1] FIFO

We are using FIFO (First In First Out) which is used as input buffer to store the data temporarily. First in first out type of buffer is shown in figure.3

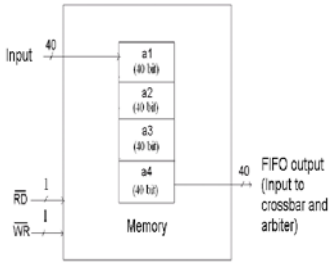

Figure.3 FIFO Buffer

When first flits of 40 bit arrives at the input port and write signal of corresponding FIFO is low, it gets stored in memory denoted by a1. When next flit arrives, data stored in a1 shift to a2 and new flit stored in a1. Similarly when third flit arrives, data stored in a2 shift to a3, data stored in a1 shift to a2 and new flit stored in a1. Finally when last i.e. fourth flit arrives, data stored in a3 shift to a4, data stored in a2 shift to a3, data stored in a1 shift to a2 and new flit stored in a1. Now very first flit is stored in a4 which is nothing but header flit containing source and destination address and last flit is stored in a1. All the flits follow the path of header flit.

2] Cross-bar

In this paper we have design of crossbar switch has 5 inputs and 5 outputs. Fig. 4 shows Multiplexer based crossbar switch. As we are getting five inputs of 40 bits from five ports of router, number of 5:1 multiplexes used inside the crossbar is five. All five inputs are given to all the multiplexers. Select line is of three bit. Select lines are generated by the arbiter (depending on the round robin algorithm). Outputs of multiplexers are the output ports of the 5X5 router.

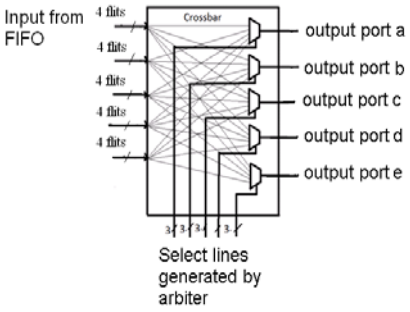

Figure. 4 Crossbars

3] Arbiter

Arbiter controls the arbitration of the ports and resolves contention problem. It keeps the updated status of all the ports and knows which ports are free and which ports are communicating with each other. In this work, we are using round-robin arbitration algorithm. Packets with the same priority and destined for the same output port are scheduled with a round-robin arbiter. If there are many input ports request the same output or resource, the arbiter is in charge of processing the priorities among many different request inputs. The arbiter will release the output port which is connected to the crossbar once the last packet has finished transmission. So that other waiting packets could use the output by the arbitration of arbiter. A round-robin arbiter operates on the principle that a request which is just served should have the lowest priority on the next round of arbitration. Depending upon the control logic arbiter generates select lines for mux based crossbar and read or write signal for FIFO buffers.

Router

The heart of an on-chip network is the router, which undertakes crucial task of co-coordinating the data flow. In this paper the router operation revolves around two fundamental regimes: (a) the data path and (b) the associated control logic. The data path consists of number of input and output channels to facilitated packet switching and traversal. We are using 5 input X 5 output routers. Out of five ports four ports are in cardinal direction (North, South, East, and West) and one port is attached to its local processing element.

In this paper we are using nine routers which are connected to each other in mesh topology. There are nine routers in this topology out of this nine if all routers i.e. 8 routers all of these are demanding the 9 number router i.e. all routers having the same destination address then contention occur and all packets of routers are reach one by one according to the priority. But the delay required in this case is more as compared to the contention free network.

III. Simulation

i)Mesh Topology

Figure. 5 a) Simulation Waveform without Contention for 3x3 mesh topology. In this we are sending packet from each router i.e. from input nine routers and send to the other router i.e. to output nine routers. And check that how much time required to reach last packet to its destination. After that we are calculating the time in nsec. In this way we are doing this for 50 packet slots. In which one packet slot means nine input of router and their output also. Following is the simulation without contention so time required to reach the packets is less. Because each input source router demand another destination router i.e. source and destination addresses are different for each input and output. . Following is the table for source and destination address for router in one packet slot.

Sr. No.	Source address (in Hexadecimal)	Destination address (in Hexadecimal)
1	0 (0000)	A (1010)
2	1 (0001)	9 (1001)
3	2 (0001)	8 (1000)
4	4 (0100)	6 (0110)
5	5 (0101)	0 (0000)
6	6 (0110)	4 (0100)
7	8 (1000)	2 (0001)
8	9 (1001)	1 (0001)
9	A (1010)	5 (0101)

Figure. 5 b) Simulation Waveform With Contention for 3x3 mesh topology. In this we are sending packet from each router i.e. from input nine routers and send to the other router i.e. to one output router. And check that how much time required to reach last packet to its destination. After that we are calculating the time in nsec. In this way we are doing this for 50 packet slots. Following is the table for source and destination address for router in one packet slot.

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7	8 (1000)	5 (0101)
8	9 (1001)	5 (0101)
9	A (1010)	5 (0101)

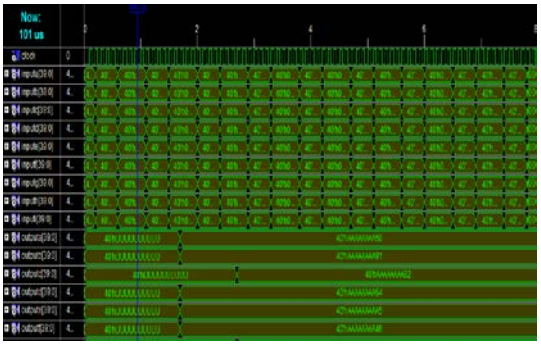

Figure 5. a

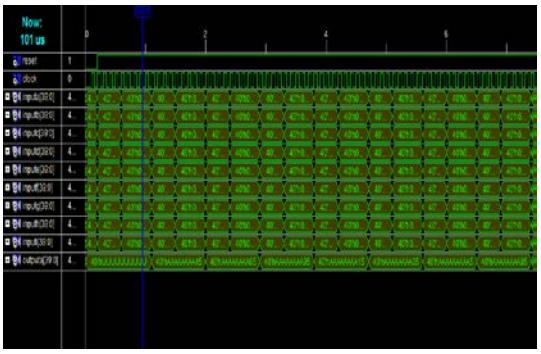

Figure 5. b

Figure 5. Simulation Waveform of Mesh Topology a) Without Contention Scenario. b) With Contention Scenario.

ii)Torus Topology

Figure. 6 a) Simulation Waveform Without Contention for 3x3 torus topology. In this we are sending packet from each router i.e. from input nine routers and send to the other router i.e. to output nine router. And check that how much time required to reach last packet to its destination. After that we are calculating the time in nsec. In this way we are doing this for 50 packet slots. In which one packet slot means nine input of router and their output also. Following is the simulation without contention so time required to reach the packets is less. Because each input source router demand another destination router i.e. source and destination addresses are different for each input and output. Following is the table for source and destination address for router in one packet slot.

Figure. 6 b) Simulation Waveform With Contention for 3x3 torus topology. In this we are sending packet from each router i.e. from input nine routers and send to the other router i.e. to one output router. And check that how much time required to reach last packet to its destination. After that we are calculating the time in nsec. In this way we are doing this for 50 packet slots. Following is the

table for source and destination address for router in one packet slot.

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8	9 (1001)	1 (0001)
9	A (1010)	5 (0101)

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3	2 (0001)	5 (0101)
4	4 (0100)	5 (0101)
5	5 (0101)	5 (0101)
6	6 (0110)	5 (0101)
7	8 (1000)	5 (0101)
8	9 (1001)	5 (0101)
9	A (1010)	5 (0101)

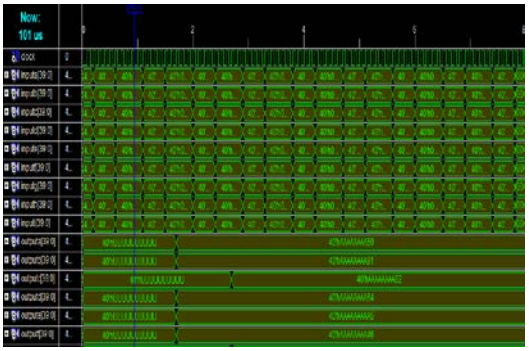

Figure 6. a

Figure 6. Simulation Waveform Of Torus Topology a)Without Contention Scenario b)With Contention Scenario.

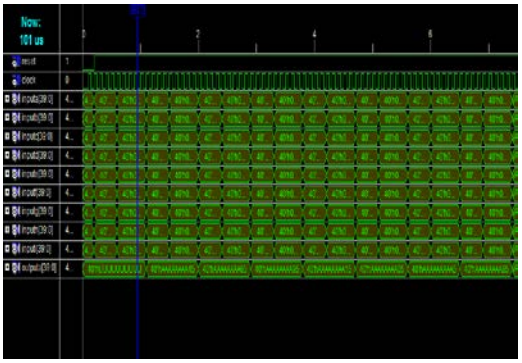

Figure 6. b

IV. Result

Time required to transfer packets in mesh and torus topology in nano second are given in the following table.

Mesh topology without contention

Sr. No.	Packet Slots	Time required to transfer packet slot in nsec
1	10	11700
2	20	20700
3	30	29700
4	40	38700
5	50	47700

Mesh topology with contention

Sr. No.	Packet Slots	Time required to transfer packet slot in nsec
1	10	79600
2	20	159600
3	30	239600
4	40	319600
5	50	399600

Torus topology without contention

Sr. No.	Packet Slots	Time required to transfer packet slot in nsec
1	10	9900
2	20	18900
3	30	27900
4	40	36900
5	50	45900

Torus topology with contention

Sr. No.	Packet Slots	Time required to transfer packet slot in nsec
1	10	79600
2	20	159600
3	30	239600
4	40	319600
5	50	399600

V. Graph

Graph for mesh topology & torus topology in which y1 represents without contention and y2 represents with contention time in nsecs and x axis represents number of packet slots.

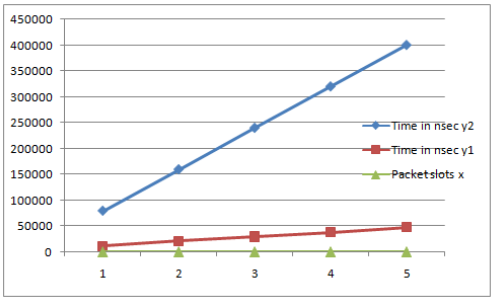

Figure. 7 Graph of Mesh Topology With and Without Contention

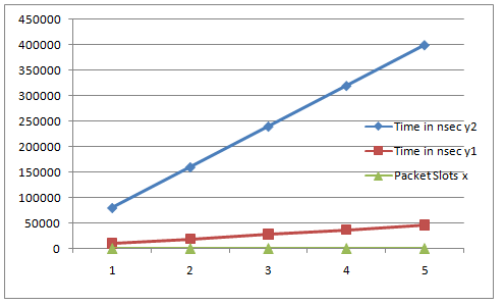

Figure. 8 Graph of Torus Topology With and Without Contention

VI. CONCLUSION

Finally after simulating above we get a simulation report of Mesh Topology and torus topology. And also we are getting the graph for mesh and torus topology and time required for each topology is also calculated in the table. In contention free network time required is less as compared contention network. From the above result in this torus topology takes less time as compared to mesh topology.

VII. REFERENCES

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