

Design of 4-bit Flash Analog to Digital Converter using CMOS Comparator in Tanner Tool

Nupur S. Kakde

Dept. of Electronics Engineering
G.H.Raisoni College of Engineering
Nagpur, India

Amol Y. Deshmukh

Dept. of Electronics Engineering
G.H.Raisoni College of Engineering
Nagpur, India

Abstract

This paper proposes a 4-bit, 1.8V, Flash ADC (Analog to Digital Converter) design using CMOS Comparator with 180nm technology. The conventional comparators have been replaced with the CMOS inverter based comparator designs. The PSRR (Power Supply Rejection Ratio) results obtained are improved with the use of CMOS comparator and by systematically sizing the transistors of the comparators. Thus it has been observed that it consumes 0.46827mW of average power.

Keywords

Comparator, CMOS inverter, flash ADC, PSRR

into logic '1' or '0' by comparing the reference voltage V_{ref} with V_{in} .

Flash type ADCs employ parallelism and the distributed sampling to achieve a higher conversion speed. As illustrated in Fig.1, a m -bit flash type ADC consists of 2^{m-1} comparators, a resistor ladder comprising of 2^{m-1} equal segments and an encoder. The resistor ladder network subdivides the main reference voltage (V_{REF}) into 2^{m-1} equally spaced voltages. The comparators then compare the input voltage (V_{IN}) with these voltages. Thus, the performance of a flash type ADC is fully dependent on its constituent comparators.

I. Introduction

Recently, the digital multimedia applications become more and more popular due to its functionality rich. However, all human interactive signals, such as video, music, are analog signals. A/D converter (ADC) is a basic device in digital signal processing systems. ADC bridges the gap between the analog world and the digital systems. With increasing use of digital computing and signal processing in various applications like medical imaging, instrumentation, consumer electronics and of course communication, the field of data conversion systems has rapidly expanded over the past few years. Resolution, Speed and Power Consumption are the primary criteria for determining the effectiveness of any data conversion system.

Among the various ADC architectures, the flash type ADC is the fastest and conceptually the simplest one. The high operating speed of a flash type ADC has made it suitable for the use in radar detection, high speed instrumentation, wide band radio receivers, high data-rate serial links and optical communication. Although the full-flash type A/D converter architecture is the most attractive solution for high-speed A/D converter designs, but it is not efficient for the resolution of more than 8-bits from a power dissipation and area perspective. The comparator count will be reasonable as long as the resolution level is kept small. Therefore the comparator structure is the most important part in flash type architectures.

The most important component in the ADC architecture is the comparator. Its role is to convert an input voltage V_{in}

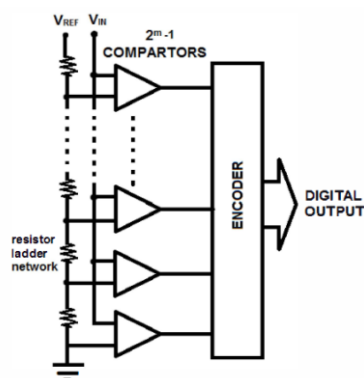


Fig 1: Block level representation of a flash type ADC architecture

Though the shortcoming of any Flash type ADC is its exponential growth in power consumption with the increase in resolution, but considering its high operating speed and simple

architecture, it is quite popular in many high speed instrumentation, signal processing applications. Thus, it becomes very much important to find some means with which the high power requirement of the flash type ADCs can be reduced. Some of the main problems of the conventional comparator structures used in A/D designs can be listed as follows:

1. large transistor area for higher accuracy
2. DC bias requirement
3. charge injection errors
4. metastability errors
5. high power consumption

6. resistor or capacitor array requirement

Two major areas of concern, for improving the power performance of a flash type ADC are:

1) *Series of resistances used for generating the reference voltages:* The power consumption of the ADC structure can significantly reduce by replacement of the resistor ladder network with any other suitable alternative.

2) *Conventional comparator circuits:* Reducing the number of transistors used in a conventional comparator will in turn reduce the total power consumption as well as the area overhead.

So, instead of using the conventional ADC, some other comparators are used. Some of the comparator structures reported in the literature are differential amplifier latch type, auto zeroed sequentially sampled comparator, dynamic, TIQ (Threshold Inverter Quantizer) comparator and QV (Quantum Voltage) comparator. The TIQ comparator has single ended input and is very sensitive to power supply noise. The reference voltages are changed when there is a noise in the power supply voltage. To overcome this problem the CMOS Linear Tunable Transconductance Element (CMOS-LTE) comparator has been proposed, in which the TIQ comparator concept has been used for the generation of reference voltages.

II. Types of ADC Architecture

A] TIQ Comparator Flash ADC

The TIQ technique, eliminates the resistor array implementation of conventional comparator array flash designs that is based on systematic transistor sizing of a CMOS inverter in a full-flash scheme. In TIQ comparator, two cascaded inverters are used as a comparator for high speed and low power consumption as shown in Fig. 2.

By means of transistor sizing, the analog input signal quantization level is set in the first stage by changing the voltage transfer curve (VTC). L is kept constant and only W is changed during the design process, since the transistor channel length, L , is more effective than the channel width, W , in controlling the performance ($fT \propto 1/L^2$). The second inverter stage is used to increase gain and logic level inversion so that the circuit behaves as an internally set comparator circuit. And the second stage must be exactly the same as the first stage to maintain the same DC threshold levels, and to balance the linearity for the voltage rising and falling intervals of high frequency input signals.

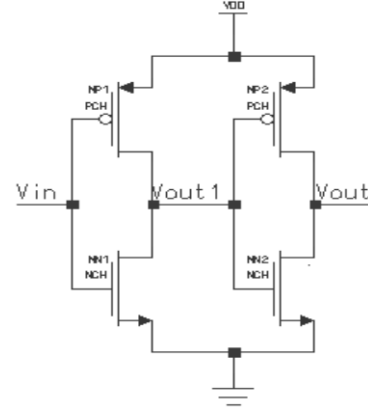


Fig 2: TIQ Comparator

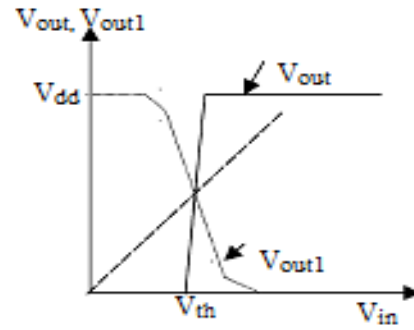


Fig 3: Voltage transfer curve (VTC)

It can be shown that the V_{th} point on the VTC of a CMOS inverter, which is shown in Fig. 3, can approximately be given by the following equation,

$$V_{th} = \{V_{dd} - |V_{tp}| + V_{tn} \sqrt{(K_n/K_p)}\} / \{1 + \sqrt{(K_n/K_p)}\}$$

where V_{tn} and V_{tp} are the threshold voltages for NMOS and PMOS devices respectively; and

$$K_n = (W/L)_n \cdot \mu_n C_{ox}$$

$$K_p = (W/L)_p \cdot \mu_p C_{ox}$$

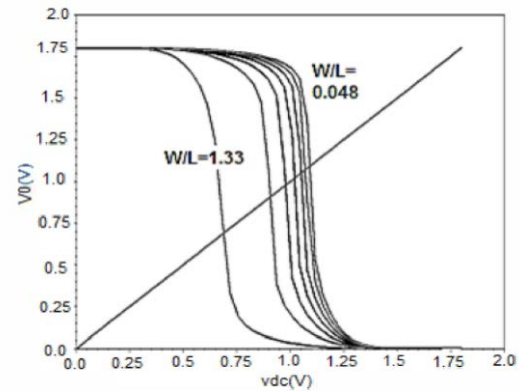


Fig 4: Inverter threshold levels for different (W/L) values

As shown in Fig. 4, the threshold of the inverter can be varied by varying the transconductance ratio. This can be done by varying the (W/L) ratio or the aspect ratio of the MOSFETs. Here, both channel width (W) and channel length (L) of the MOS transistors are varied instead of varying just one parameter to obtain a better precision.

B. CMOS-LTE Comparator Flash ADC

The simplest voltage-to-current transducer (VCT) implemented in CMOS technology is the well-known CMOS inverter. As shown by experiment and simulation, the inverter has the excellent frequency response and very low distortion; however its power supply rejection (PSR) is poor and the linear behavior depends critically on the matching between p-channel and the n-channel transistors; i.e., the parameter $\mu_{\text{eff}}C_{\text{ox}}W/L$ must be the same for both the transistors. The MOS parameters in the previous expression have their usual meaning. Unfortunately, the effective mobilities μ_{eff} of electrons and holes depend on doping, bias voltages and temperature, so perfect matching is difficult to achieve in practice.

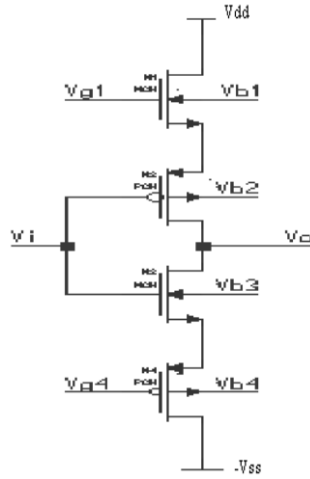


Fig 5:CMOS Linear Tunable Transconductance Element

The solution of this problem is the four transistor CMOS transconductance element, whose operation resembles in most respect that of the CMOS inverter but without having PSR problems. Fig.5 shows the CMOS Linear Tunable Transconductance Element.

1. CMOS Linear Tunable Transconductance Element (CMOS-LTE) Comparator

The CMOS-LTE Comparator uses Linear Tunable Transconductance Element and inverter as shown in Fig. 6. The internal reference voltages are generated by systematically varying the transistor sizes of the CMOS linear tunable transconductance element.

All transistor sizes of this element are identical in this design, with V_{g1} and V_{g4} as fixed voltages. The output of this component is connected to CMOS inverter to increase the voltage gain of the comparator.

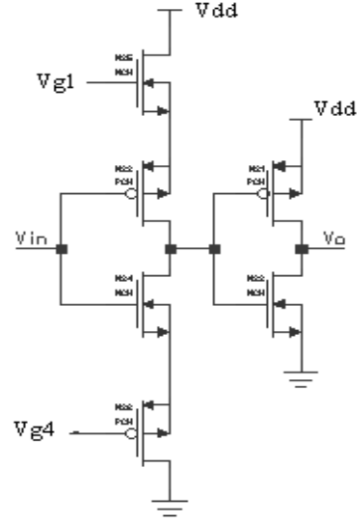
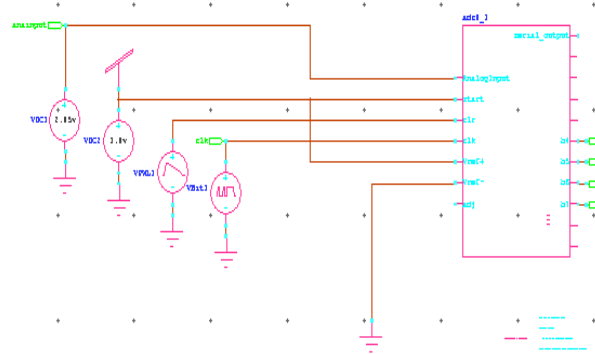


Fig 6: CMOS-LTE Comparator

III. The Structure Of Proposed Flash Adc



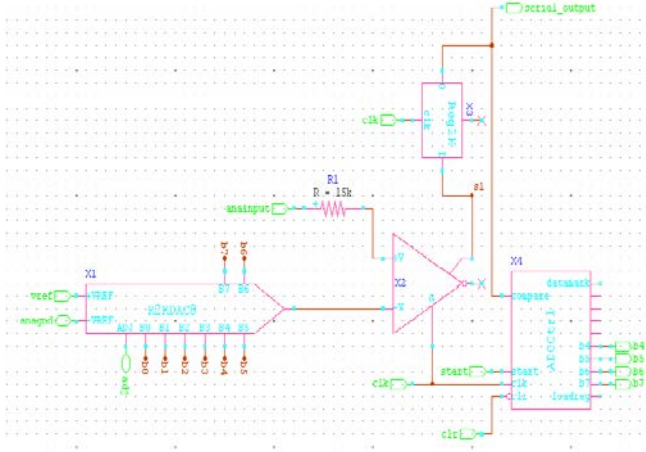


Fig 8: ADC Comparator

B] R-2R Digital to Analog Converter(DAC):

An example of a 3-bit R-2R MOS converter is shown in Figure9. In this figure R-2R cell shown with a possible combination with the bit current switch. All transistors in this

system are equal. Transistor M1 and M2 divide the input current $2I$. Transistors M1 and M2 can operate in saturated mode or in a triode mode. In saturated mode transistors M1 and M2 divide the input currents $2I$ in to two equal currents I . In this case transistor M3 acts as a cascade transistor and supplies the output currents to the load. At the moments transistors m1 and M2 are in triode region, then these transistors can be seen as a resistor with value R . In this case transistor M3 performs an equal resistor of value R . In this way R-2R network is implemented and with careful termination an accurate binary weighted current division is obtained.

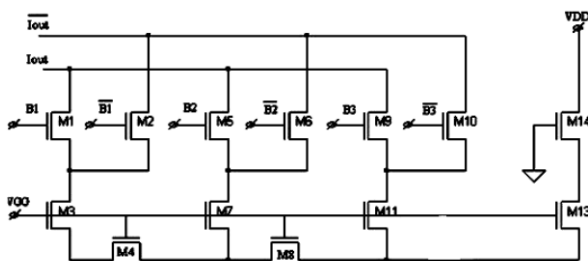


Fig 9 : CMOS equivalent circuit of 3-bit R-2R DAC

C] System Performance:

The proposed CMOS comparator has been designed for 180 nm technology using Tanner Tool 15 Fig. 10 and Fig. 11 show the output of ADC and waveforms of average power respectively. It is observed that with the use of CMOS Comparator power supply variation problems are

reduced. Simulation results of CMOS Comparator Flash ADC are furnished in table 1.

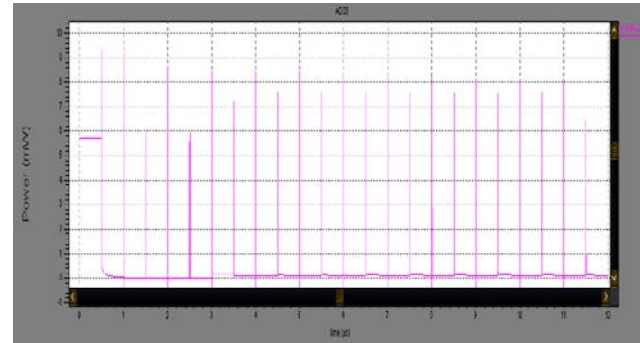


Fig 10: Power Waveforms

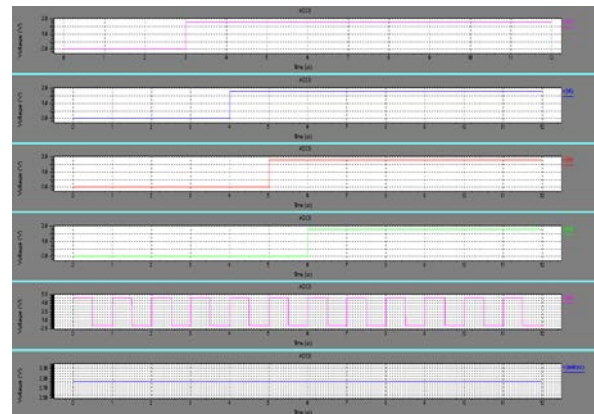


Fig 11: Output of CMOS-LTE Comparator Flash ADC

TABLE 1: SIMULATION RESULTS OF 4-BIT CMOS-LTE COMPARATOR FLASH ADC

Features	Specifications
Resolution	4 bit
Power Supply	1.8V
Technology	180 nm
Total Power Dissipation	0.46827mW

IV. CONCLUSIONS

CMOS Comparator Flash ADC have been designed and simulated with 180 nm technology. The results obtained are encouraging and indicate that the CMOS Comparator approach has the advantage of better power supply noise rejection. Also the power dissipation is reduced because of the internally generated reference voltages.

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