A simulation-based optimization of low noise amplifier design using PSO algorithm

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Summary
In this paper we propose a particle swarm optimization based approach for designing CMOS low noise amplifier (LNA). Existence of tradeoffs between noise, gain, linearity, stability and power consumption in LNA design, forces the designer to accomplish such a long time complicated work to optimize the circuit. So the utilization of a modern optimization is inevitable. In this work the usage of PSO algorithm in LNA circuit design optimization has been investigated. The performance of LNA circuit is evaluated through HSPICE and PSO algorithm is implemented in MATLAB, so a combination of MATLAB and HSPICE is performed. A cascode LNA is designed using 0.18μm CMOS technology foe near 2.4 GHz band applications. The results of this work indicate the effectiveness of this optimization approach that is a time saver method.

Key words:
LNA, PSO, optimization, CMOS.

1. Introduction

Nowadays, due to emerging commercial wireless application, high-performance RF circuits are required in modern communication. Low noise amplifier (LNA) is one of the most important and essential building blocks in RF transceivers [1]. It is integrated into the receiving chain and is either directly connected to the antenna or placed after RF pass band filter[2], and it should provide a proper low noise amplified signal to the next stage, e.g. mixer, from a week input signal by adding as little inherent as possible[3].
The LNA should provide sufficient tranceconductance gain with acceptable linearity and power consumption to allow for long battery life especially in portable hand-held applications. Therefore there are some tradeoffs between gain, noise figure (NF), linearity and stability in LNA design optimization [4].
In order to achieve the best performance of the designed circuit, designers must continuously and repeatedly tune the designed circuit elements and perform a circuit simulation using an electric computer-aided design (ECAD) software, to optimize active devices model parameters and sizes , passive devices parameters, biasing conditions, etc. it is in general a long time, high complexity and complicated work. A proper optimization method can be used to overcome this problem.
In this work we implement a particle swarm optimization (PSO) algorithm in MATLAB [5] which has been linked with an electrical simulator, HSPICE [6]. The performance of LNA is considered in terms of NF, IIP3, gain, s-parameters and power consumption.
Price and other market requirements force RF receivers to be integrated in standard CMOS technology along with the rest of digital signal processing unit [7]. Since several applications have been developed near the 2.4 GHz band, such as IEEE802.15.4 , IEEE802.11b and Bluetooth, we have simulated a 2.4 GHz CMOS LNA using TSMC parameters for 0.18 μm mixed signal and BSIM30 version 3.1[8]. This paper is organized as follows: The particle swarm optimization concept is explained in Section 2. In Section 3 the platform of optimization is explained. In Section 4 the LNA design specifications and consideration has been described. We propose the method of optimizing LNA design using PSO in Section 5. The achieved simulation results are discussed in Section 6 and finally, we draw conclusions in section 7.

2. Particle swarm optimization

Particle swarm optimization (PSO), first introduced by Kennedy and Ebehart[9], is an evolutionary computation method based on the social behavior and movement of swarm searching for the optimal and best location in a multidimensional search space and has been found to be robust in solving continues nonlinear optimization problems[10].
This approach simulates the social behavior of bird flocking or fish schooling model. Each particle (i-th particle) position is represented by a d-dimensional vector and denoted as Xi = [xi1, xi2, …, xid] and is randomly initialized . The set of n particle in the swarm are called population: X=[X1, X2,…,Xn]. Each particle is assumed to move around in the so called multidimensional space to reach the best position which has the best fitness value. In each iteration of simulation the fitness function is evaluated by taking the current position of each particle,

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and if achieved fitness value is better than previous best fitness of i-th particle, the current position will be selected as the best previous position of i-th particle and described as PBi=[pbi1, pbi2,…, pbid]. The best position among the population is called global best position and described as GBi=[gb1, gb2,…, gbd].
The rate of position change for each particle is called particle velocity: Vi = [vi1vi2, … , vid]. each particle would like to return to its own optimum point, so the velocity has a term proportional to (pbi-xi), it would like to follow overall best global optimum point too, so a term proportional to (gb-xi) is added to velocity. Therefore:

vidk+1 = wvidk +c1 rand1k (pbid -xik) + c2 rand2k (gbdk-xidk) (2)
Where w is intera weight parameter which controls the tradeoff between the global and the local search capabilities of the swarm. c1 and c2 are acceleration factors and indicate the relative attraction toward pb and gb respectively. rand1 and rand2 are two random numbers uniformly distributed between 0 and 1, which indicate the craziness of particles[10]. k is the iteration number. The new position of i-th particle is then determined by:

xidk+1 = xidk + vidk+1 (2)
Generally PSO has the advantage of being very simple in concept, easy to implement and computationally efficient algorithm. Since updates in algorithm consist of simple adding and multiplication operators and no derivation operation is included, computation time is dramatically decreased compared to other heuristic algorithms. In order to avoid premature
Convergence, PSO utilizes a distinctive feature of controlling a balance between global and local exploration of the search space which prevents from being stacked to local minima [11].

3. System platform

The purpose of optimization is to achieve the optimal size of MOS transistors (channel length and width), passive component values and bias currents of the circuit, in order to meet the desired specifications. This paper proposes a technique that utilizes a simulation-based approach for circuit design optimization.
The system platform is illustrated in Fig. 1. The starting point is a spice-like netlist of the circuit topology, currently entered in the optimization engine as its input. Desired specifications are other inputs. Optimization engine consist of a PSO algorithm written in MATLAB which has been linked with an electrical simulator, HSPICE, as its performance evaluator.

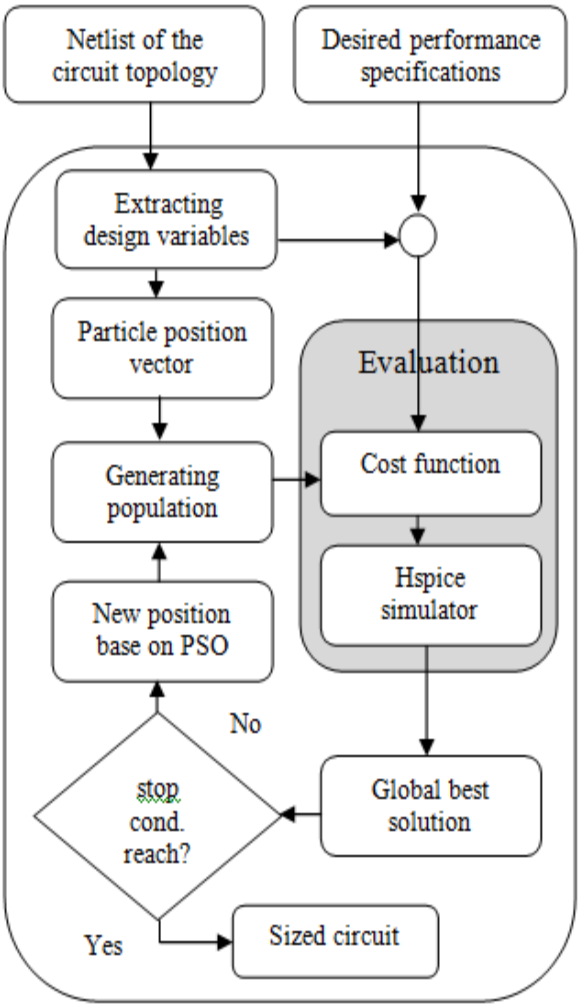

Fig. 1 system platform flow.

Optimization is executed on a vector of design variables of circuit extracted from the netlist. In fact, the particle position vector is the channel length (L) and width (W) of MOS transistors, passive component values, and bias currents.
At first, each particle (i-th particle) position vector is randomly initialized. In each iteration, the algorithm runs the HSPICE for each particle and evaluates a cost function (CF), described in (3):

$$CF = \sum_{i=1}^{k} w_i \left| \frac{f_i(x) - f_{id}}{f_{id}} \right| \quad (3)$$

Which, fi(x) is i-th design specification, k is the number of specifications, fid is desired value for i-th design specification and wi are the importance factors that say which specification has more importance for designer regarding to different especial applications of the circuit. With this approach, the searching algorithm (optimizer) will find the best solution that meets this cost function.

Therefore, PB and GB are showing the minimum CF for best previous position and global best position respectively that each particle attempts to reach them. At the end of each iteration, GB gives the best solution of the population.

4. LNA design specifications

As called previously, there are some tradeoffs between noise figures (NF), gain, linearity and stability in LNA design process. There are some considerations about these design Specifications:

4.1 Linearity

Increasing the gain of LNA can degrade the linearity. Linearity of LNA is measured in terms of IIP3 that is required to be maximized. Generally, to achieve higher linearity in RF receivers, IIP3 must be more than -10dBm [12].

4.2 Stability

The stability conditions, if and only if k>1 and |Δ|<1, presented by stability factor k must be satisfied [3] where

k= (1-|S11|2-|S22|2+|Δ|) / (2|S21×S12|) (3)

Δ= S11× S22 - S21×S12 (4)

For CMOS LNAs, the required S21 is normally larger than 10 dB. For S11 and S22, the input/output return losses, less than -10 dB are desirable. Also to avoid unwanted signals to reach the LNA input from the following stages, reverse power gain S12 must be less than -20 dB [12].so in LNA design optimization these specifications must be considered.

4.3 Noise

The noise performance of a circuit is typically characterized by a noise factor F or NF which indicates how much degradation occurs in the output signal-to-noise ratio due to the circuit's internal noise [13]:

$$F = \frac{(S/N)_{in}}{(S/N)_{out}} = \frac{total\quad output\quad noise}{total\quad output\quad noise\quad due\quad to\quad source}$$

or

$$NF = 10\log\frac{(S/N)_{in}}{(S/N)_{out}} \qquad (5)$$

Fig .2 shows the standard CMOS noise model [14]. One of the noise source caused by channel resistance, which is modulated by Vgs. its power spectral density given by:

$$\bar{i}_{nd}^2 = 4kT\gamma g_{do} \quad , \qquad (6)$$

$$g_{do} = \left.\frac{d(i_d)}{d(V_{DS})}\right|_{V_{DS}=0}$$

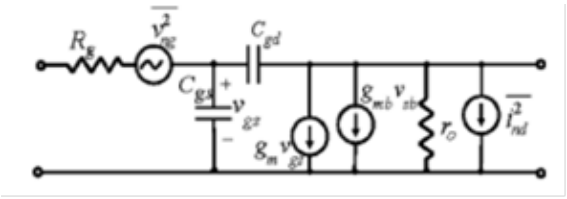

Fig. 2 Standard CMOS noise model.

Which, gdo is the conductance when VDS is equal to zero. γ is the channel thermal noise coefficient, which depends on channel length and its bias conditions. Finite gate resistance also exhibits the other source of noise. Power spectral density of gate's thermal noise is given by:

$$\bar{v}_{ng}^2 = 4kTR_G \quad , \qquad (7)$$

$$R_G = \frac{R_g W}{3n^2 L}$$

Where Rg is the gate polysilicon sheet resistance, W and L are the width and length of the device and n is the number of gate fingers in the device layout.

Therefore, size and other parameters of active devices and the value of circuit's resistance and bias condition affect the NF and must be optimized in LNA design.

5. The LNA circuit design and optimization

The schematic of LNA under investigation [3] is shown in fig.3. It has the cascode topology with inductive degeneration to provide a high gain and high reverse isolation, which improve the stability and simply input port matching.

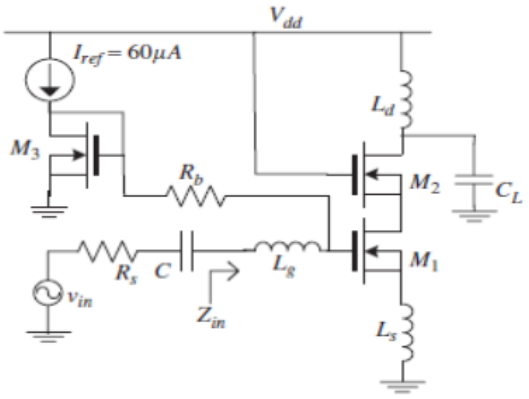

Fig. 3 The cascade LNA schematic.

The purpose of LNA optimization is to achieve the active devices size and passive values that give the best design specifications, which considered in section 3.for this purpose; the PSO algorithm gets a spice netlist of LNA circuit as its inputs. In fact, the particle position vector is the size and value of the active and passive devices. In this work, it is a 9-dimensional vector, as shown in table 1.

Table 1: The design parameters and specifications

The position vector's elements	*Design specifications*
I_{ref}	NF
W_{M1}	IIP3
W_{M2}	Power dissipated
W_{M3}	S_{11} (input return
L_d	S_{22} (output return
L_s	S_{21}(power gain)
L_g	S_{12}(reverse power gain)
C	
R_b	

At the optimization engine, each particle (i-th particle) selects random values for active and passive devices (or random value for i-th position vector). In each iteration, the algorithm runs the HSPICE for each particle and evaluates a cost function (CF), described in (3). So, at the end of each iteration, PB and GB are showing the minimum CF for best previous position and global best position respectively that each particle attempts to reach them. Finally, as the stop condition of algorithm is reached, GB shows the optimized values of the circuit.

6. Simulation results

Considering so called importance factors, three case studies of LNA is carried out using PSO. For each case, achieved value of passive devices and size of active devices and bias current are tabulated in table 2, and a comparison whit three other works is shown in table 3.

Table 2: achieved value of passive devices and size of active devices and bias current

	Case study1	*Case study2*	*Case study3*
I_{ref} (µA)	69	142	128
W_{M1} (µm)	111.8	94.5	109.9
W_{M2} (µm)	700	588	700
W_{M3} (µm)	.2	7.5	2.5
L_d (nH)	9.17	10	25
L_s (nH)	.2	.01	.07
L_g (nH)	15.2	16.4	13.6
C (pF)	284.35	305	387.35
Rb	200	251	87

Table 3: The circuit specifications in comparison whit other works

	Case study1	*Case study2*	*Case study3*	*Ref[17]*	*Ref[13]*	*Ref[18]*
technology	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS
f_0 (GHz)	2.4	2.4	2.4	2.4	5.4	5.4
NF (dB)	1.5	2.1	1.06	3.5	1.8-2.6	0.423
gain	22.15	14.17	18.9	13	20.5	12.55
IIP3 (dBm)	-7	-3	-2.3	-6.5	-6.2	-4
S_{11} (dB)	-15	-15	-20.3	-8	-18.5	-23.84
S_{12} (dB)	-36.8	-43	-44.6	-14	-48	-20.54
power (mW)	14	2.1	3.6	3.4	-	2.84

In case study 1, the gain has assumed to get much higher priority among other design specifications. As indicated in table 3, the improvement in gain is achieved in cost of linearity degradation and power dissipation. Conversely, the power has more importance for designer, in case study 2. It is clearly visible from table 3 that although the power consumption is decreased but the gain of LNA is decreased too. Finally, considering all specifications, a reasonable LNA design for general applications is carried out in case study 3, which its gain, s11, s12 and NF are depicted in fig.4

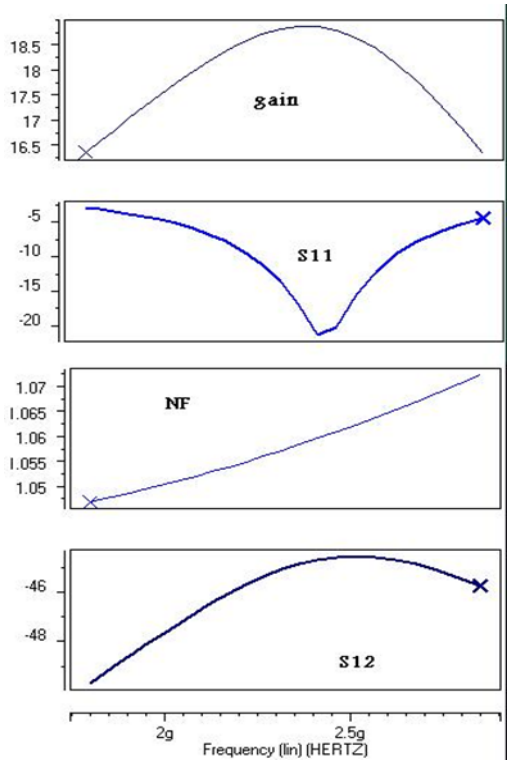

Fig. 4 The specifications of case study 3.

7. Conclusion

In this paper, a PSO based approach for optimal design of LNA circuit has been reported. Electrical characteristics of the LNA circuit considered in the optimization process are the gain, S parameters, noise figure, power consumption and the input third-order intercept point. The results of this work indicate the effectiveness of this optimization approach that is a time consuming method. We note that this approach can also be applied to design optimization of other circuit and can be embedded into any electronic CAD software which improves the process of design and fabrication.

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