Design Transfer impedance amplifier circuit with low power consumption and high bandwidth for Optical communication applications

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Abstract
Nowadays, use of optical communications is widely used in data transmission applications at near and far distances. The main parts of an optical communication system includes a transmitter, channel and receiver which the design and construction of each of these parts have their own problems and challenges. Since the optical data sent from the transmitter to the receiver have been found with large deficits such as weakness, noise, distortion, diffraction, interference, etc. design of the receiver has faced further challenges. The receiver consists of different parts including an optical detector, amplifier, filter, circuit decision and etc. The task of optical signals is converting optical signal into electrical signals. Amplifier which develops the most important part of optical receivers amplifies the signal generated through optical detector. The optics emitted through an optical fiber has been incurred large losses before reaching to the optical detector in receiver part. Then optical detector converts light intensity to a current proportional to the light intensity, which subsequently it has been amplified via a Trans-Impedance Amplifier (TIA) and converted to the voltage. However, the signal generated in the output of TIA has usually small amplitude in about several tens of millivolts. So after class TIA, another amplifier class should be used to increase signal fluctuations in the reasonable levels, i.e. in range of 500 mV. An amplifier that is used for this purpose is called Limiting Amplifier shown with LA. LA has large output fluctuations in addition to generation of High voltage gain. This research aims to design LA and TIA in a way to reduce the consumed power as much as possible by creating gain and suitable bandwidth to transfer data at a rate of 2.5 Gb/s.

Key words:
Transfer impedance amplifier, optical receiver, Limiting amplifier, CMOS

1. Introduction

Due to the man's increasing need for use of high-speed systems in recent years, the use of optical communication systems were of particular importance. As mentioned in abstract, the signal from the transmitter to the receiver has many flaws, which caused many challenges in the design of the receiver. The amplifier used in optical receiver has consisted of two circuit structures TIA and LA, which design of TIA includes the intense balance between noise, bandwidth, gain, feeding voltage and power consumption, raised many difficult challenges in both bipolar technology and CMOS technology. TIA converts a current in input to a voltage in output [1]. The circuit is defined by means of the transfer impedance gain in form of ratio of changes in output voltage to changes in input current. For instance, a gain of 1 KΩ implies that TIA in response to a change with 1 μA in the input generates a change with 1mv in output. This is due to the fact that the optical detectors generate a small current and since most of next processes appear at voltage area, the current should convert to the voltage [2]. Indeed, a resistance can work out this lonely and generate the transfer impedance gain equal to R, but time constant from an optical detector capacitance and resistance leads to intense balance between gain, noise and bandwidth. In fact, the combination of diode / resistance drastically reduces bandwidth. The amount of resistance should increase to reduce input noise, which this causes reduction in bandwidth. In practice, the circuit consisting of diode and resistance has very low bandwidth and very high noise [3]. In addition, resistance compared to the transistor consumed much more power, thus use of resistance causes considerable increase in power consumption. To resolve these problems, TIA is used to reduce noise and power consumption as much as possible in addition to high bandwidth and gain. In design of TIA, a variety of techniques are used to increase performance of amplifier, i.e. increase in gain and bandwidth and decrease in noise and so on. For instance, gain boosting is used to increase gain, capacitive coupling is used to resolve problem at feeding voltage and inductive peaking method is used to increase bandwidth. Bandwidth of TIA is considered about 70% of the data rate so as to reduce the noise [4]. However the signal generated in output of TIA has small amplitude about a few tens of millivolts. Thus, after class TIA, another amplifier class should be used to increase signal fluctuations in the reasonable levels, i.e. in range of 500 mV. An amplifier that is used for this purpose is called Limiting Amplifier shown with LA. LA has large output fluctuations in addition to generation of High voltage gain [5]. Las used in optical receivers should

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supply numerous circuit needs. LA should have small input capacitor in a way the bandwidth of TIA does not reduce the previous class. To resolve this problem, it can use the buffer, but use of buffer between TIA and LA is difficult in small feeding sources, especially if the noise appears critical. Further, at the first class of LA, balance should be created between input capacitor, input noise and voltage gain. Bandwidth of LA should be designed larger than TIA, generally equal to the data rate[6]. This is due to the fact that if two classes with identical bandwidth are connected in a cascade form to each other, bandwidth of the small signal is narrowed. The signal generated in TIA has large ascending and descending times in addition to low voltage level. Thus LA should amplify signal and increase slew rate in a way to reduce time ascent and descent. The input noise in LA is of great importance due to two reasons: 1-large bandwidth leads to further noise, 2-design of TIA with high transfer impedance gain increases at high speeds and causes greater importance of noise in LA. LA is designed in form of a multi-class amplifier. The first class of LA should generate sufficient gain in a way to minimize the noise created in next classes [7]. However, it can generate large classes with low gain, the power consumption and noise increase. For this, LA generally consists of three to four classes. In design of LA, a variety of techniques are used to increase bandwidth which it can refer to inductive peaking, capacitive degeneration, Cherry Hooper and fT Doubler. This research aims to design LA and TIA in a way to reduce consumed power as much as possible by creating suitable bandwidth and gain for transfer of data at rate of 2.5 Gb/s.

2. Design of the proposed optical receiver with low consumed power

In this section of research, a transfer impedance amplifier is proposed for optical receivers. This amplifier is based on feedback resistor-capacitor in parallel topology which has been optimized in terms of consumed power, and technique of shunt peaking has been used to increase frequency bandwidth. This circuit has been designed and simulated in 0.18 µm CMOS technology. Results from simulation display gain(67 dBΩ), bandwidth(3 GHz), and consumed power(12 mW), indicating suitable performance of the proposed amplifier for 2.5Gb/s applications for use in SONET OC-48 standard. The diagram obtained for data rate of 2.5 Gb/s displays an acceptable quality of signal for input currents to 10µA [8]. Nowadays, use of optical communications has spread in applications of data transfer at far and near distances. The main parts of an optical communication system includes a transmitter, channel and receiver which the design and construction of each of these parts have their own problems and challenges. Since the optical data sent from the transmitter to the receiver have been found with large deficits such as weakness, noise, distortion, diffraction, interference, etc. design of the receiver has faced further challenges. The receiver consists of different parts including an optical detector, amplifier, filter, circuit decision and etc.[9]. The task of optical signals is converting optical signal into electrical signals. Amplifier which develops the most important part of optical receivers amplifies the signal generated through optical detector. The optics emitted through an optical fiber has been incurred large losses before reaching to the optical detector in receiver part. Then optical detector converts light intensity to a current proportional to the light intensity, which subsequently it has been amplified via a Trans-Impedance Amplifier (TIA) and converted to the voltage [10]. TIA design includes serious compromises between noise, bandwidth, gain, feeding voltage and power consumption, raised numerous challenges in both bipolar technology and CMOS technology. Transfer impedance gain is defined as ratio of changes in output voltage to changes in input current. Currently, if the construction cost is considered low, CMOS technology will be the best choice. In addition, since designer can use the transistors with smaller dimensions, chip area and power consumption can reduce drastically [11]. Three major structures for circuits of Transfer impedance amplifier include open-loop structure with high input impedance, open-loop structure with low input impedance and transfer impedance with feedback loop. Each of these structures have displayed various features in terms of bandwidth and gain and have their advantages and disadvantages, allowed the designer to select the best design for a special application [12]. Among all the amplifiers reported in various references, the structures based on mode-current method and transfer impedance amplifiers with parallel feedback represent the best compromise between all the design conditions, i.e. high gain, high bandwidth and low noise and power consumption[13]. Yet the current mode amplifier due to high power consumption and more noise compared to amplifiers with parallel feedback are less likely used. For instance, J.M Garcia has used a parallel resistance feedback structure to design the transfer impedances amplifier in 0.18 µm CMOS technology, gained gain(58 dBΩ), bandwidth(1.5 GHZ) and power consumption(23.7 mW).

Fig 1 displays the proposed circuit typology.

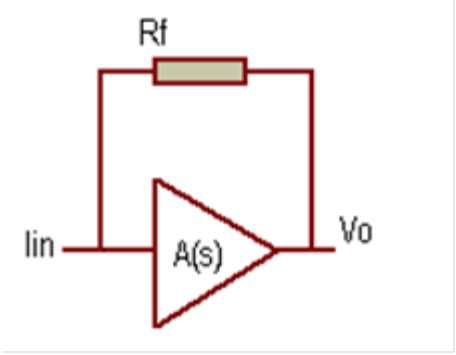

Fig 1. The diagram black for the used transfer amplifier

The bandwidth and gain are less, thus a transfer impedance amplifier with new parallel feedback structure is proposed to improve performance of the structure above. The circuit typology used in this research uses a capacitor in parallel to the resistance in addition to having the feedback resistance in a parallel way. Figure 2 displays the diagram block for the proposed design.

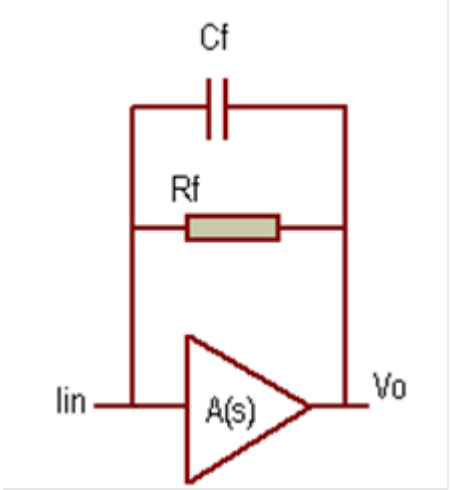

Fig 2. The diagram block for proposed transfer amplifier

In second section, design of proposed amplifier is proposed. Results from circuit simulation and the circuit optimization stages are proposed in next section.

3. The proposed amplifier

As mentioned earlier, noise, bandwidth and gain are the key parameters in an amplifier. Yet if the gain at open loop in an amplifier falls large, the gain at closed loop can be estimated via Rf. Thus the active part should optimize two other aspects, i.e. noise and bandwidth. Therefore, the circuit proposed in fig. 3 is proposed for the amplifier. The first class (MB1, MN) includes a cascade typology which has developed for a common source class. The second class uses the combination of MB2 and MB3. Feedback grid is a combination of resistance (Rf) and capacitor (Cf). The last class is a common drain combination as the driver. Transistors M1 and M12 have been used to adjust DC level. In simulation, the optical detector has been modeled with a current source, but since the amount of current depends on type of optical fiber and type of optical detector, determination of exact amount of this current source for an optical system can be selected with an amount of about 10 µA. in this section, first the design has been made with the resistance feedback and then the capacitor has been added to the circuit, and the optimized results have been proposed and compared with the resistance feedback structure, and ultimately inductor has been added to the circuit and the optimal results of the simulation have been proposed.

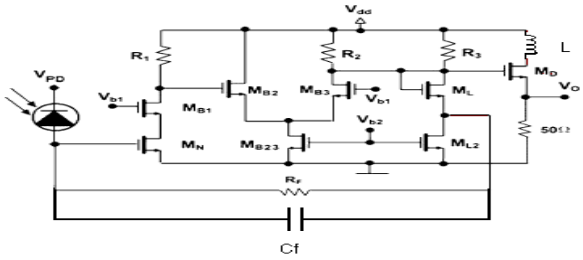

Fig 3. The circuit typology for the proposed amplifier

4. The Transfer Ampedence Amplifier

The transfer ampedence amplifier converts the signal of the curretn generated via detector to the voltage signal which the relationship between these two electrical signals is determined by means of transfer ampedence. As shown in figure 3, it can use this relationship for Rf passive resistance; as shown, use of resistance causes design does not work out properly at simulation technology and various tempreatures. The reason for this is that the resistance is susciptable to the changes of tempreature and process. Thus, after completing design and optimization, the resistances are substituted with transistor. With the presumption for large amplifier gain, the closed loop gain is determiend via Rf. Ths to acheive gain about 70 dBΩ, resistance Rf is selected equal to 3 KΩ which amount of KΩ is obtained equal to 3.8 KΩ after simulation and optimization.

5. Frequency Response

To improve frequency response, it can use a variety of methods for increase of bandwidth. With regard to structure of figure 3, circuit cutoff frequency is obtained via the equation below:

$$f_u = \frac{g_{mB2,3}}{2\times\pi\times C_l} \quad (1)$$

where C1 is the capacitor in the output and gmB2,3 equals to:

$$g_{mB2,3} = \sqrt{2\mu_n C_{ox}\frac{w}{l} I_{MB2,3}} \quad (2)$$

Where bias current (IMB2,3) is supplied through transistor(MB23). Further, the channel length of all the transistors has been considered equal to 0.18 µm to improve frequency response and have suitable phase bound. To increase gain and bandwidth, it can increase W/L at transistors MB2,3 and MB23 but till these transistors do not enter to Triode areas.by optimizing dimensions at transistors via HSPICE, optimal values for W/L at transistors will be as what shown in table 1.

Table 1. Values of W/L at transistors

transistors	W/L
M_n	60/0.18
M_{b1}	45/0.18
M_{b2}	45/0.18
M_{b3}	45/0.18
M_{b23}	120/0.18
M_{L2}	70/0.18
M_L	45/0.18
M_D	40/0.18

Another way to increase bandwidth is to remove pole or create a zero near the pole. In this structure, capacitor Cf has been used. This capacitor has been optimized via simulation and the best place for it is in parallel with feedback resistance. The optimal value via Trial and error method procedure equals to 15 fF for this capacitor. Technique of Shunt-Peaking is another method to increase frequency bandwidth. For this, inductor L in parallel to capacitor has been used in output. Thus we will indicate that it can increase bandwidth to 20% via this technique. Value of this inductor has equaled to 40nH by optimization.

6. Results from simulation

The proposed amplifier has been simulated in 0.18 µm technology via 1.8 v feeding source, represented with the results as follow. To compare and understand the performance of circuit, the simulation is proposed at first for the structure with simple resistance feedback and then the results from adding capacitor with optimal amount are proposed and ultimately the effect of adding inductor will be proposed.

The structure without inductor and capacitor

Figure 4 displays the results from simulation for structure with resistance feedback.

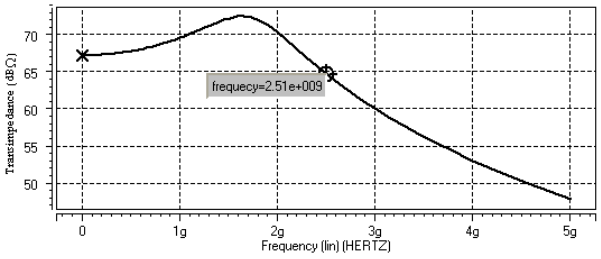

Fig 4. Frequency response of the amplifier circuit with resistance feedback and without capacitor and inductor

As shown in figure, the gain and bandwidth have gained equal to 67 dBΩ and 2.5GHZ, shown a considerable improvement compared to the results in related works. In addition, the consumed power equals to 12 mW which has reduced compared to the results represented in other related works.

6.1. Adding capacitor to the feedback circuit

By adding capacitor at feedback part of the proposed circuit to remove more poles, it was specified that the best place to add capacitor is in parallel to the feedback resistance. Fig. 5 displays the results from simulation for this circuit. As shown in figure 5, adding capacitor causes improvement in bandwidth. At this state, bandwidth and gain will equal to 2.7 GHZ and 68dBΩ. In addition, fluctuation has reduced in frequency response. It is obvius that adding capacitor or inductor does not bring about any change in consumed power.

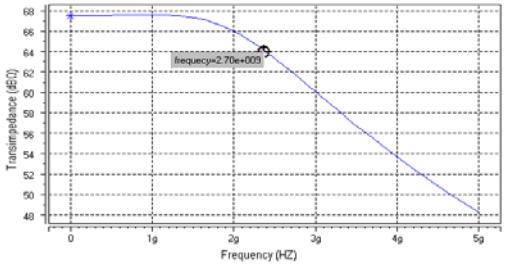

Fig 5. Frequency response of the amplifier circuit with resistance feedback and capacitor without inductor

6.2. Adding inductor

By adding inductor in series with transistor, obtained results will improve. Figure 6 displays the result for adding inductor.

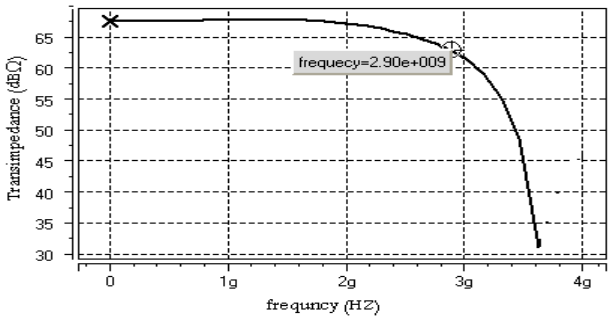

Fig 6. Frequency response of proposed amplifier circuit

As shown in figure, gain has not changed to a large extent, but bandwidth has increased to 2.9 GHZ. Table 2 compares the results from proposed design at various states of circuit implementation.

Table 2. Comparison of simulation results

performance	structure	with resistance and capacitor	with resistance
transfer conductivity gain	67 dBΩ	68 dBΩ	67 dBΩ
consumed power	12 mW	12 mW	12 mW
bandwidth	3 GHZ	2.7 GHZ	2.5 GHZ

These results have obtained at 25ºC temperature and tt technology. As thickness of oxide layer of transistors might change in making integrated circuits in CMOS technology and reduce or increase for a little, the performance of circuit can change a lot. Change of temperature can lead to change in performance of circuit. Designer of circuit should make design in a way that the circuit works out well at all temperatures between -40º-125º and at the entire simulation technology. Simulation technology is considered to consider change at thickness at oxide layer in making integrated circuit. Tt technology implies that all the transistors-type n and p have thickness of typological oxide layer. Ss technology implies that all the transistors have the thickness of oxide layer greater than the typological amount; ff technology implies that the transistors have the thickness of oxide layer less than the typological amount. These three technologies are the major ones, required for the best design. Results from simulation at temperature of 25ºC for the proposed structure have been displayed in table 3.

Table 3. results from simulation at various technologies for thorough structure

performance	tt	ss	ff
transfer impedance amplifier	67 dBΩ	44 dBΩ	65
consumed power	12 mW	14 mW	17 mW
bandwidth	2.9GHZ	0.4GHZ	1.4GHZ

With regard to the results from table 3, it is specified that design is not favorable especially in ss technology. One of the most important reasons is the use of resistance in circuit. Therefore, to resolve this problem, transistor is used instead of resistance, shown with the results as follows:

Substitute resistance and inductor with transistor

If MOS transistor is biased at Triode area, the resistance between drain and source is obtained via the equation below:

$$R_{ds} = \frac{1}{\mu \times C_{ox} \frac{w}{l}(V_{GS} - V_{TH})} \quad (3)$$

This equation indicates that it can design transistor with resistance with considered values by setting gate-source voltage and W/L ratio. To substitute inductor with transistor, active inductor as shown in figure below is used[28].

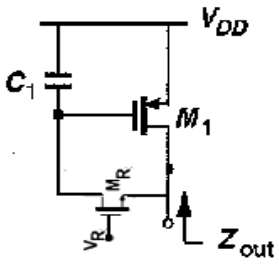

Fig 7. Active inductor using PMOS transistor

Final structure of the transistor has been drawn in figure 8. The results from simulation at various technologies and at temperature of 25ºc have been represented in table 4 for the structure of transistor. These results indicate a considerable improvement at technologies than other implementations.

Table 4. results from simulation at various technologies for structure of transistor

performance	tt	ss	ff
transfer impedance amplifier	67 dBΩ	56 dBΩ	63
consumed power	12 mW	13 mW	15 mW
bandwidth	3GHZ	2.1 GHZ	2.7 GHZ

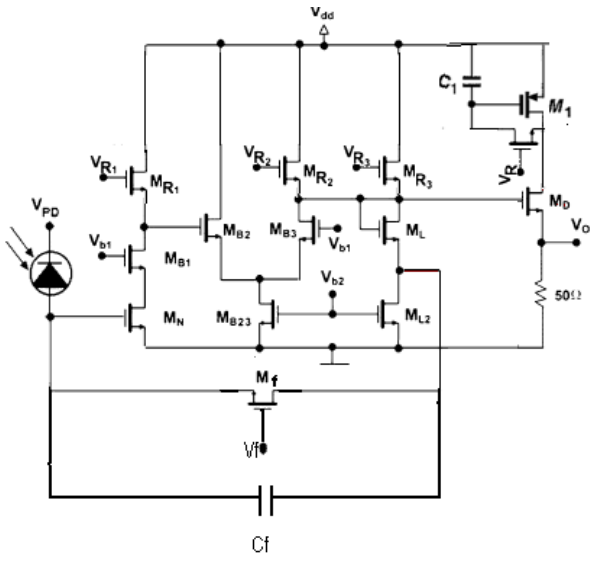

Fig 8. Circuit typology of the proposed amplifier for transistor

The frequency response of the transistor circuit has been drawn in figure 9. As shown in figure, the bandwidth equals to 3 GHZ.

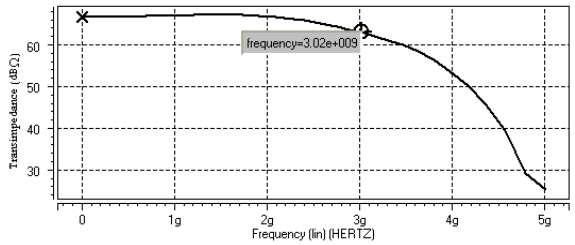

Fig 9. Frequency response of the amplifier circuit at transistor

To examine quality of output signal, the diagram for rate of data(2.5 Gb/s) for input current(10 µA) has been drawn in figure 10, displayed an acceptable quality for this rate of data and current level. Table 5 compares the results from simulation of the proposed structure with other previous implementations at various CMOS technologies. Results from simulation display low power consumption, larger bandwidth and larger transfer impedance amplifier than other works. Indeed, in this research, bandwidth has increased to 50%. The results are acceptable at major technology of simulation, while the results of works have not been proposed at these technologies. To reach to conclusion, we deduce that the proposed design in this simulation has used all the benefits of CMOS and reached to a high performance, outperformed at all technologies.

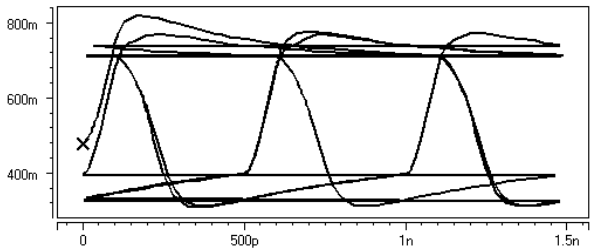

Fig 10. Eye diagram for data rate(2.5 Gb/s) and input current(10 µA)

Table 5. Comparison of results from simulation with related works

performance	This work	[29]	[30]
technology	CMOS 180 nm	CMOS 180 nm	CMOS 90 nm
transfer impedance	67 dBΩ	58 dBΩ	85 dBΩ
feeding source	1.8 V	1.8 V	1 V
consumed power	12 mW	23.7 mW	184 mW
bandwidth	3GHZ	1.5 GHZ	1.5 GHZ

As shown in previous sections, the optical signal received at each receiver converts to electrical signal via photo diode, which range of this signal is about microamps.

This signal has been the current type, which should be converted to voltage signal. TIA converts this current signal to voltage and amplifies it. Yet, amplitude of signal has not been sufficient with several millivolts. This poor signal leads to error in decision circuits. Thus an additional gain loop is required so as to increase the voltage fluctuations to suitable reasonable levels. LA is a method for this purpose, used widely in communication systems, which it is connected to output of TIA and made the tasks below.

1-it generates additional voltage gain

2-it improves input signal in terms of noise and distortion

3-A LA converts the output voltage of TIA to a voltage level to a large extent for decision circuit to detect logical 0 and 1 properly.

The factors below are taken into account to design LA:

1-input capacitor: in general, TIA and LA are make on a chip, thus the input capacitor of LA should be minimized so as not to reduce the bandwidth.

2-noise: LA has a large contribution in making receiver noise. Thus, noise simulation should be taken into account in design and simulation of LA.

3-gain: to ensure the input signal reaches to logical levels, the total gain of LA should be large to a sufficient extent. In general, a 40 dB gain is acceptable for LA.

4-bandwidth: bandwidth of LA should be larger than t ia in order that general bandwidth does not reduce.

Design of LA

To design LA, the circuit shown in figure below is used. In this circuit, transistors M_3, M_4, R_1 and R_2 play the role

of active inductor. Resistances R_1 and R_2 have been made with the transistors with the same name. The reason for use of active inductor is that passive inductors occupy large space and increase the construction cost a lot.

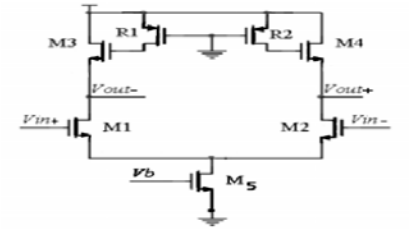

Fig 11. The proposed LA circuit

6.3. Design of the receiver

The receiver circuit includes TIA and LA classes of transistor, represented in figure below. This circuit has been designed and simulated in 0/18 µm cmos technology.

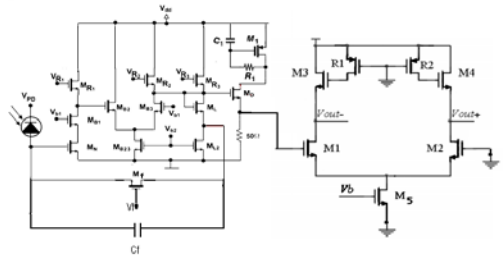

Fig 12. Receiver circuit

In this design, simulation of noise has been also considered and the implementation has been made based on high gain. Low power consumption and required bandwidth have been made for rate of data(2.5 Gb/s). Table 6 represents simulation results at technologies tt, ss and ff.

Table 6. Receiver simulation at corners

	ff	ss	tt
gain	75 dB	69 dB	**75.5**dB
bandwidth	3.3 GHZ	2.8 gHZ	3.25 GHZ
power consumption	11.9 mW	11.3 mW	11.5 mW

At technology tt, voltage, bandwidth and power consumption equal to 75 Db, GHz and mw, respectively. A significant improvement is seen in power consumption compared to the related works.

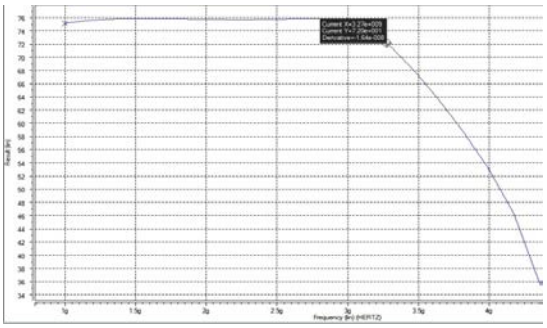

Fig 13. Frequency response of receiver circuit

Table 7 represents the comparison of this research with related works. Effective noise voltage equals to 15 nv/√HZ, which reduced drastically in power consumption compared to related works; the bandwidth displays a significant improvement.

Table 7. Comparison of results with related works

refere	[31]	[29]	This work
gain [dB]	32	58	75.5
bandwidth [GHZ]	3	1.5	3.2
power consumption [mW]	53	24	11.5
noise m V_{rms}	-	0.27	0.8

Figure below displays the noise chart in terms of frequency.

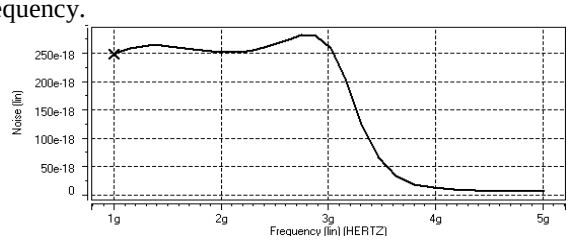

Fig 14. Noise chart in terms of frequency

The eye diagram of the receiver at the rate of data(2.5 Gb/s) is represented in figure below. As shown in figure, the eye diagram has a suitable quality at the rate of data(2.5 Gb/s).

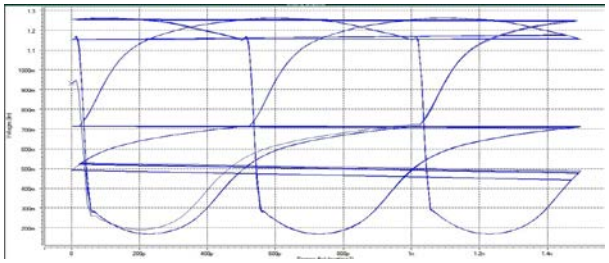

Fig 15. Eye diagram of receiver per rate of data(2.5 Gb/s)

6.4. Design of circuit of the second optical receiver with low power consumption

As mentioned earlier, this research intends to design an optical receiver circuit with low power consumption at 0/18µm cmos technology. At previous section, a receiver circuit was proposed which consists of gain (75dB), consumed power(11.6 mw) and bandwidth(3.2 GHZ). To achieve the aim for lower power consumption of circuit as well as comparison of two various receiver circuit designs, another receiver is designed which LA part in it has been same as previous part, but TIA part is substituted with another circuit.

Design of circuit TIA and optimization methods

The circuit in figure below is suggested for TIA.

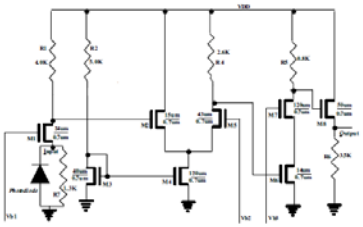

Fig 16. Circuit TIA

The optical signal reached to the receiver converts to the current signal via Photodiode and applied to common gate amplifier (M_1). Resistance (R_1) has been considered to supply bias of transistor (M_1). The output signal in drain (M_1) is applied to another common gate class which has been considered with M_5. M_2 is a leading source class which together with M_5 develops a differential pair. Transistor (M_3) has been designed to supply bias (M_4) and develops a current together with M_4, designed for supplying currents M_2 and M_5. M_6 together with M_7 is a cascade class, considered to increase gain and bandwidth; ultimately M_8 is a follower source which generates an output with low impedance. The results below are gained with design and simulation of this circuit. As shown in figure, gain and bandwidth equal to 75 dB and 1 GHZ, but the power consumption has gained equal to 4MW, displayed a significant reduction compared to the previous design.

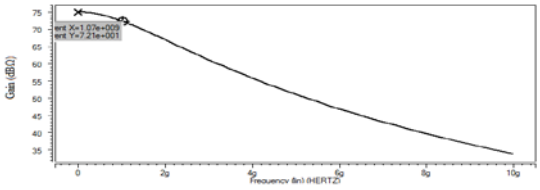

Fig 17. The chart for frequency response

To increase bandwidth at this circuit, firstly a feedback resistance is used, shown in figure 18. This resistance (R_3) causes rise of a feedback which has connected from drain (M_7) to drain (M_2) and causes reduction at time constant (RC) at drain(M_1) and increases bandwidth. In addition to feedback resistance, technique of inductive peaking has been used, shown with inductor (L_1) in drain (M_5). Results from simulation have been displayed in figure 19.

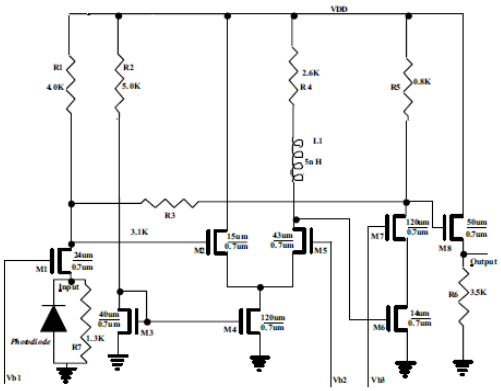

Fig 18. Circuit chart for TIA by adding inductor L1

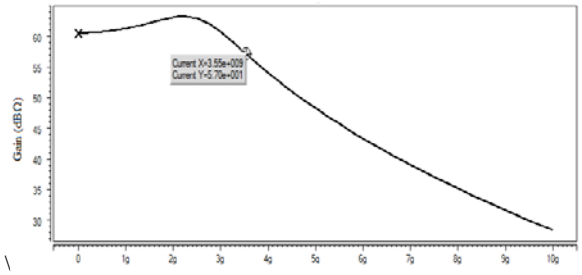

Fig 19. Frequency response

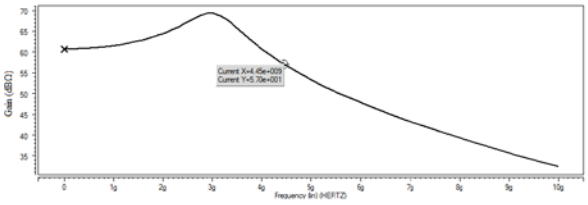

Fig 20. The chart for frequency response of circuit

By adding these two techniques, bandwidth has increased to 3.55 GHZ and gain has increased to 60Db and power consumption has reached to 4mw. To achieve the aim for maximization of bandwidth, the proposed circuit in figure 18 is optimized. Figure 20 has displayed the results from optimization. Results from simulation display a significant improvement in bandwidth. The bandwidth has obtained

to 4.45 GHz at this state, while the gain has not changed and the power consumption (3.9 mw) has reduced for a little. At previous sections, a variety of techniques have been introduced and suggested to increase bandwidth; some of these techniques are used to increase bandwidth in design of this circuit. For this, firstly capacitor(C_f) in parallel to feedback resistance(R_3) has been used and also inductor(l_2) has been used at class(M_7). With simulation, it was specified that simulation has the best favorable effect at drain(M_7). The reason is that the second leading pole has put in drain(M_7) and can be compensated with inductor(L_2). Figures 21 and 22 display the structure of proposed circuit and results from simulation.

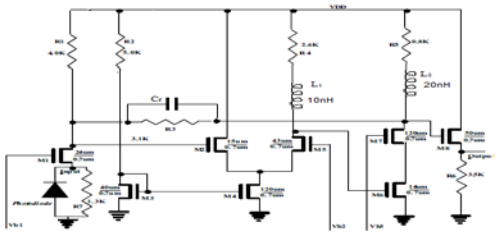

Fig 21. The proposed circuit structure

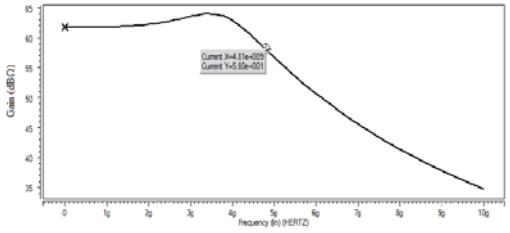

Fig 22. Results from simulation of the proposed circuit

As expected and as shown in results from simulation, the gain has not changed, but the bandwidth has increased to 4.8 GHZ. In this design, feedback resistance technique and feedback capacitor have been used, which figure 23 is suggested to improve structure. In this structure, inductor (L_f) has been used in parallel to capacitor and feedback resistance. As known, no one has used this structure to design TIA and/or integrated optical circuits. Previous circuits have consisted of feedback resistance and/or resistance and feedback capacitor, and inductor has been just used in drain of transistors with leading pole.

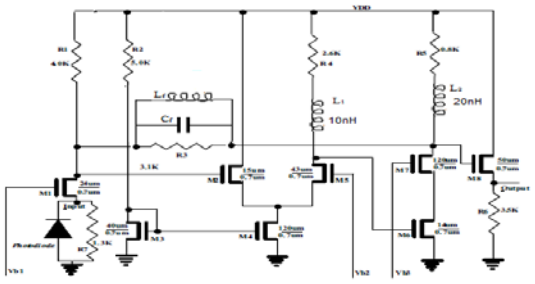

Fig 23. The proposed circuit by adding feedback inductor

The results from simulation for this structure have been proposed in figure 24.

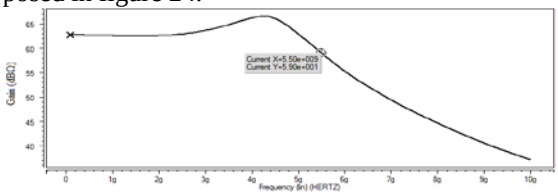

Fig 24. Results from simulation with feedback inductor

As shown in figure 24, use of this proposed new technique has caused a significant improvement in the bandwidth. The bandwidth equals to 5.5 GHZ, found with significant improvement compared to previous structures and techniques.

6.5.L A circuit

The circuit shown in LA circuit is for the receiver designed in previous section, neglected to express the details in this part.

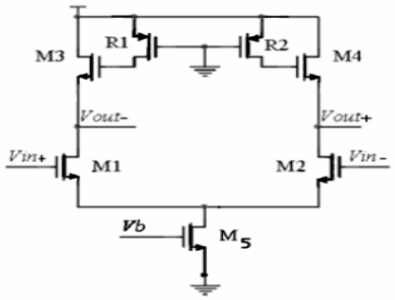

Fig 25. The chart for circuit LA

6.6. Design of the receiver circuit

By connecting circuits LA and TIA designed in previous sections, the optical receiver circuit is obtained with the structure in figure 26.

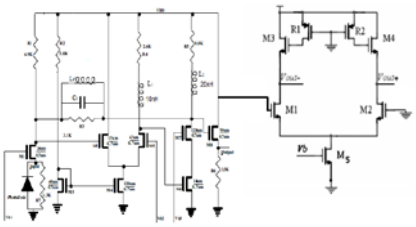

Fig 26. The receiver circuit chart

Figure 27 displays the results from simulation for optical receiver. The receiver bandwidth, gain and power consumption equal to 5.02 GHZ, 76 dB and 5.3 mw, respectively;

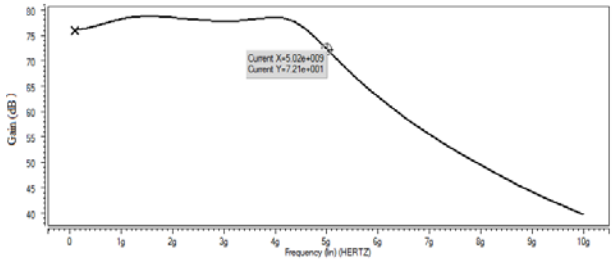

Fig 27. Frequency response of receiver

The noise value has obtained equal to 64nv/$\sqrt{Hz}$. The eye diagram for optical receiver can be observed in figure 28 which has proper quality. Table 8 displays comparison of this design with design of previous circuits.

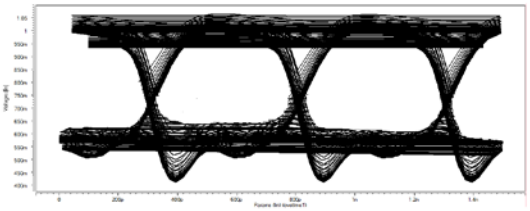

Fig 28. Eye diagram for receiver

Table 8. Comparison of the results from the second design with related works

TECHNOLOGY	0.18 µm cmos	0.5µm cmos	40 nm cmos	0.13µm cmos	0.18µM CMOS
references	[29]	[33]	[44]	[45]	THIS WORK
consumed power	23.7	70 mw	15 mw	32 mw	5.3 mw
gain	58 dB	60 dB	79.5 dB	51 dB	76 dB
bandwidth	1.5 GHz	3.5 GHz	1.5 GHz	26 GHz	5.02 GHz

To avoid the coupling between L_1 and L_2 inductors, they were simulated with active inductors, with the circuit shown in figure below.

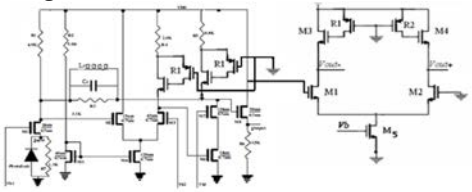

Fig 29. The receiver circuit with active inductor

To examine accuracy of performance of the circuit, it was simulated in the technologies shown in table 9.

Table 9. Simulation of the second receiver circuit

	tt	ss	ff
gain	71 dB	69 dB	73 dB
power consumption	6 mW	4 mW	9 mW
bandwidth	3.6 GHZ	3.2 GHZ	4 GHZ

By adding active inductor and simulation of circuit, we obtained gain(71 dB), bandwidth(3.66 GHZ) and consumed power(6.13 mw), shown in figure below.

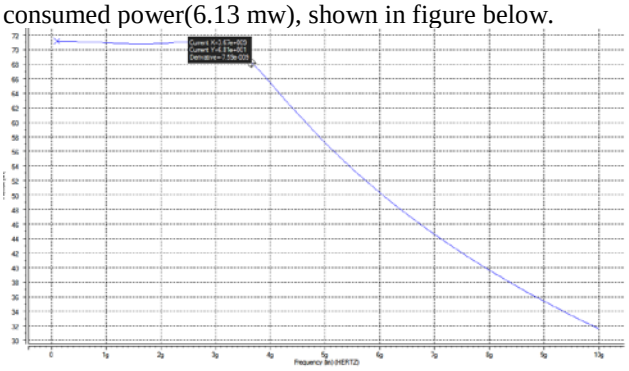

Fig 30. Frequency response of the receiver circuit with active inductor

7. Conclusion

In this research, we examined and designed optical receiver circuit including TIA and LA. Both circuits were designed at 0.18 µm CMOS technology and simulated via software HSPICE. The aim of design has been an optical receiver for 2.5 GB/s applications. Thus, design was made to meet these needs and optimization was made. The obtained results indicated a considerable improvement than related works especially in power consumption. The power consumption was obtained for the first optical receiver and the second receiver about 11.6 mW and 5 mW, which is less than related works. To increase bandwidth, a new method was suggested. The proposed

compensation method is based on use of capacitive-inductive-resistive grid at feedback part. This compensation method displayed a considerable improvement in frequency response. In addition, active inductor was used instead of passive inductors in this circuit, caused reduction in cost of chip construction. One of the features of this research is that we have made this design in technologies and met the circuit needs in them.

8. Suggestions

-study on changes in temperature on optical receiver part
-design of circuits at 0.09 mμ and 0.13 mμ technology to reduce consumed power
-study on aspects of receiver noise
-increase the dynamic range of designed circuits for optical receivers without increase in consumed power

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