Detection and rapid improvement of the transient regime switching in ASD equipment by wavelet transform

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Abstract

Nowadays, due to the increasing spread of using nonlinear loads causing creation of transient regime scenarios on the distribution networks, the necessity of investigation and analysis of the power quality for stability and reduction of energy losses in the power networks has become more important than ever. Transients are often created by injecting energy due to switching or lightning and cause changes in the nominal current and voltage. The sudden increase or decrease of voltage or current makes characteristics of the transient regime. This article is to study and identify the transient regime swinging in distribution networks resulting from a capacitor bank switching by a wavelet transform and then provides a control technique to capture and restore the overvoltage caused by the mentioned switching in the system of Adjustable Speed Drive (ASD). The exact function and accuracy of this method has been shown by simulation in Matlab.

Keywords:

wavelet transform, the transient regime, capacitor banks switching of a capacitor, ASD

1. Introduction

A study on the stability of the power system is an important point and power engineers attempt for making the system better and more stable. In this respect, investigation of power systems in stationary and transient states is extremely important. The sudden increase or decrease of voltage or current makes characteristics of the transient regime. The transient regime is a part of a variable that disappears during the transition from a steady state to other steady conditions. In general, transients are divided into two categories of impact and oscillatory. The main cause of oscillatory transient is switching whereas lightning is the main cause for impact transient.

Transient regimes in power systems are one of the factors that by evaluating them for power transforms, ASDs and network equipment, we can design how to protect and insulate them as well as the corresponding insulation equipment. The parallel capacitor banks due to diverse uses including reduction of power losses and voltage control can increase the capacity of the system and the necessity of using them in the network is inevitable. However, parallel capacitor banks when connected to the network create a transient state in the system that if the caused transition isn't properly identified, quality of the power can be impaired. If switching of a capacitor bank occurs at the voltage moment of 90 degree, a transient regime will be created in the network by several times of the nominal voltage and current that can lead to a serious damage to sensitive equipment of ASDs because of large use of ASDs systems. Hence, the need for inspection and protection of these systems is inevitable. Figure (1-1) shows a view of an ASD system [2, 1].

Different techniques such as neural networks, fuzzy-neural networks or wavelet transform and their combination are used for the identification and separation of the transient regime on the power system [3, 4, 5, 6]. More recently, signal-based techniques on the basis of wavelet transform have been presented which can identify the separation of these transients in less than a quarter of a cycle [7, 11].

A method has been presented in [8] for reducing the transient resulting from switching of a capacitor bank which leads to the increase of the system losses and costs due to the existence of an IGBT which should always be in the system. In [4], using mutual inductance and two transistors, the excess current is restricted that results in the control system complexity and the increase of the ASD system size. In [5], using a technique called as CETL, reduction of the transient regime caused by switching of capacitor banks is investigated. Recently, wavelet transform is used to separate the transient regime caused by the capacitor bank and other disturbances of the power system [8, 9].

The theory of the wavelet transform is expressed in the section 2; a technique based on wavelet transform to identify the transient regime resulting from the switching of the capacitor bank is introduced and examined in the section 3; a 6-busbar network is stimulated and studied in the section 4 to identify and restore the transient energy of

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switching and to protect the ASD equipment; and finally, the results are assessed and concluded.



Figure 1.1: A view of an ADS system

2. Wavelet Transform

Multi-scale feature of wavelet transform allows decomposition of the signal to a number of measures. This feature can be exploited to separate the internal error of the transformer from the transient caused by the capacitor bank switching. The signal multi-resolution decomposition process x [n] is schematically shown in Figure 1-2. Each stage contains two digital filters and two reducers of the sampling rate. The first filter g [.] is a discrete mother wavelet that is inherently high-pass and the second filter h [.] is its symmetry and is inherently low-pass. By crossing the sampling rate reducer, outputs of the two filters generate the component D1 and estimation A1, respectively. Estimation A1 breaks down again and continues according to the Figure 2-1. All wavelet transforms can be specified with a low-pass filter h that can meet the standard mirror filter requirement.



Figure 1.2 Decomposition of the sub-band of the discrete wavelet transform, g [n] high-pass filter and h [n] low-pass filter

H(z) is the z transform of the filter h. Its complementary high-pass filter is defined as the relation 2: $G(z) = z H(-Z^{-1})$ (2)

With the increase in length (index i) the sequence of filters is obtained as the relation (3):

$$H_{i+1}(z) = H\left(z^{2^{i}}\right)H_{i}(z)$$
(3)
$$G_{i+1}(z) = G\left(z^{2^{i}}\right)H_{i}(z), i = 0, ... I - 1$$

With the initial condition of $H_0(x) = 1$, it can be indicated as a two-scaled relationship in time.

$$h_{i+1}(k) = [h]_{\uparrow 2^{i}} * h_{i}(k)$$

$$G_{i+1}(k) = [g]_{\uparrow 2^{i}} * h_{i}(k)$$
(4)

The subtitle [.] $\uparrow m$ represents the increase of sampling rate by the factor m and k is equally sampled in discrete time. Normalized wavelet and the basic function of scales φi , $\mathbf{1}^{(k)}$ and ψi , $\mathbf{1}^{(k)}$ are defined as the relation 5:

$$\varphi_{i,1}(k) = 2^{i/2} h_i (k - 2^i l)$$

$$\psi_{i,1}(k) = 2^{i/2} g_i (k - 2^i l)$$
(5)

The factor $2^{i/2}$ is the product of internal normalization. i and 1 represent the scale and inversion parameter, respectively. Decomposition of discrete wavelet transform is described as the relation 6:

$$a_{(i)}(l) = x(k)^* \varphi_{i,1}(k)$$

$$d_{(i)}(l) = x(k)^* \psi_{i,1}(k)$$
(6)

 $a_{(i)}$ and $d_{(i)}$ are respectively the estimated coefficients and partial factors with the resolution i [12].

To identify and retrieve the transient regime caused by capacitor banks switching by wavelet transform

Since the electronic equipment called as ASDs are very sensitive to transient regime, timely detection of the transient regime to maintain stability and protect the network equipment is a vital issue. In [10, 13, 14], it is shown that the db family is appropriate to be used for analyzing the electrical signals by the wavelet transform. In [6] and [7], using the two following principles and wavelet transform, detection of the transient regime caused by switching of the capacitor bank is evaluated.

1. The level D1 is used to find the starting point of switching because the fastest changes and frequencies can be observed at this level.

2. To separate switching flow of the capacitor bank due to the slope slowing, the level d4 is used for more resolution of the signal components [7].

Using wavelet transform and its energy absorption in a 6busbar system, the transient regime phenomenon is examined in this article. Then, a control system is provided which generate appropriate signals to absorb excess voltage and current, after identifying the transient regime. The values of the network elements are displayed in table 3-1. Figure 1.3 illustrates the studied 6-busbar network schema and Figure 2.3 shows the ASD network protected by the proposed ASD technique.



Figure 1.3 The schema of the studied system with ASD load



Figure2.3. ASD equipment protected by the proposed technique

In the above network, in order to correct the power factor and to increase the voltage, a capacitor bank of 4 megalike is connected to the network at the time of 0.04 seconds. The transient regime caused by the connected capacitor bank is displayed in the Figure 3.3. As shown in Figure 3.3, after connecting the capacitor bank, a damped transient is created in any three phase of the capacitor bank. The regime has the most transient voltage and current in the phase B since the source voltage is maximized.

Table 1.3 Busbar system values



Ts1	63.25	V
Ts2	25.400	V
Load1	1.5	MW
Load2	1.5	MW
Load3	1.5	MW
L	300e-6	Н
С	4	MVAR
C1	1000e-6	F
C2	416e-6	F
ASD	50	KW
load		

Figure 3.3 demonstrates the result before and after the switching of capacitor bank at 0.04 second in the ASD.



Figure 3.3 Voltage and current of the transient caused by connecting a capacitor bank in the studied network

Figure 5.3 respectively displays values of Dc link, inverter voltage, load voltage, and load current before and after the capacitor bank switching to improve the power factor and increase the performed voltage. As can be seen in the figure, at the time of 0.005 second, the phase-to-ground voltage across the load at the moment of the capacitor bank switching has increased from 340 V (before switching) to 500 V (after switching), load current of 120 Amp (before switching) has risen to 180 Amp (after switching) and Dc link voltage has increased from 650 V (before switching) to 950 V (after switching). These transients can have adverse effects on power electronic devices of an ASD system. It should be noted that after connecting capacitor banks in the steady state, the network voltage reaches to 380 V from 340 V. This voltage increase is due to the correction of the power factor.



Figure 4.3 Transient caused by the entry of a capacitor bank to ASD Dc link, (b) inverter voltage, (c) load voltage, (d) load current

In order to detect the transient regime of a capacitor bank of the 3 bus current on 4 levels by the mother wavelet db1, wavelet transform is taken. After determining the values of X, Y in the phase B, the transient caused by the capacitor bank is diagnosed at the time 0.042s. In order to absorb the transient energy the control signal is built for the capacitor C3 by the control section. Figure 6.3 illustrates the inside view of the control unit to detect and generate the IGBT pulse.



5.3 A view of the detection system and protection control unit

Figure 6.3 demonstrates the transient current caused by the capacitor bank switching in the phase B and the values of X, Y for the phase B is shown in Figure 7.3. Algorithms to identify, detect and capture the transient regime caused by a capacitor bank are checked.



Figure 6.3 Wavelet transform from the capacitor bank switching transient of the phase B via db1



Figure 7.3 Magnification of Figure 4.3 and specification of X, Y

3. Simulation

To obtain the data required for studying the proposed algorithm the power system of the Figure 1.3 which is stimulated in the Matlab is used. This system consists of a voltage source, two distribution transforms, three loads and a capacitor for power factor correction. To achieve the accuracy of the algorithm presented in the third part at the time 0.04s when the phase B reaches the maximum value a capacitor bank enters to the circuit to improve the power factor. As shown in Figure 3.3, by entering the capacitor bank, a transient regime is created in the voltage and current signal of the phase B. This regime passes through the transform T2 with a difference of 30 $^{\circ}$ and enters into the ASD at the time 0.042s resulting in overvoltage of

approximately 160 V that is very dangerous for electronic equipment. Now, by connecting the control unit to the circuit, control signal is built and IGBT is commanded that according to the energy size of the transient state caused by the capacitor bank switching, to enter the capacitor C2 into the circuit for absorption of the energy caused by the transient. The absorbed energy is injected into the system via the capacitor C2 using a diode parallel and inverse with IGBT and when Dc link voltage reaches less than 750 V.

Initially, the maximum transient current caused by the capacitor bank is computed by the relations 1-4 to 3-4. In equations 1-4 to 3-4, first, with regard to the generated extra voltage and current, the maximum transient energy is attained from the capacitor bank and the capacitor capacity needed to absorb this energy is obtained. The relevant algorithm is shown in Figure 4. Initially, the inrush current is detected from the wavelet transform using the offered technique and ultimately the control unit generates pulses required for protecting the system, according to the maximum allowed current and voltage. Figure 2.4 shows transients caused by the capacitor bank in the connection mode of the control system that the control system has managed well first to absorb malicious voltages incoming to the ASD equipment in the capacitor C2 and then to reinject it into the system by a diode parallelized and reversed in IGBT and finally to protect the ASD equipment against the overvoltage incidence.



Figure (1-4) Algorithm of detection and control pulse generator for absorption of the transient energy resulting from the capacitor bank switching

According to the Figure 2.4, the output voltage is applied over the load by 55 Volt more after the capacitor bank switching that is due to the reactive power correction. This amount can incrementally increase in order not to occur voltage stepping increase in the load, using SVC soft switching method.



Figure 2.4 Protection of transients caused by entry of the capacitor bank into the ASD of the Dc link

Inverter voltage (b) load voltage (c)load current

Figure 3.4 demonstrates (a) input voltage, (b) the pulse generated by the control system, (c) the capacitor C3 voltage, and (d) the capacitor C3 current

As the figure 3.4 shows clearly, following the completion of the pulse, the protection capacitor voltage begins to discharge the absorbed energy via the diode parallel and inverse with IGBT so that the voltage level becomes Dc link.



Figure 3.4 (a) input voltage (b) the pulse generated by the control system (c) the capacitor C3 voltage (d) the capacitor C3 current

According to the Figure 4.4, the excess voltage caused by the capacitor bank switching after the entry of the control unit is approximately 10 V that doesn't damage ASD equipment and prevent damage to ASD devices.



Figure 4.4 A view of voltage across the load after the activation of the control unit and the load protection at 0.04s

4. Conclusion

In this article, using a wavelet transform and introducing an ultrafast method, inrush current of capacitor bank switching was detected in less than a quarter of a cycle and a technique was offered for absorption and restoration of the transient caused by the capacitor bank switching. Simulation results indicate that the proposed algorithm is an accurate one to identify and absorb the energy of the transient regime that managed to detect the excess voltage in less than 0.005 second and to generate a control signal for inhibition of the overvoltage. Moreover, a method was presented for detection of the capacitor bank transient regime and by offering an appropriate controlling technique the caused overvoltage was absorbed and restored to the system.

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