Analysis of Breakdown in New Stepgate Structures with Graded LDD

Roji Marjorie S†
Saveetha School of Engineering,Chennai,TN,India

Govindacharyalu PA††
Vasavi College of Engineering,Hyderabad,TS,India

Lal Kishore K
CVR College of Engineering,Hyderabad,TS,India

Summary
A new stepped gate structure with a graded LDD is presented. This graded LDD helps to spread the electric field throughout the LDD region and thereby obtain a high breakdown voltage of 68 V. Efforts were made to obtain the optimum structure from the breakdown point of view by determining the number of LDD implantations needed, the optimum LDD dose and the optimum device length. A 2D analysis was carried out on the various parameters such as the horizontal and vertical electric field patterns, the impact generation profiles, generation recombination, impact generation before and after breakdown, the carrier concentration, electron and whole current densities and the conduction current densities of the structure. A mathematical analysis was also carried out which established that the breakdown phenomenon is not only by the ionization integral but the shape of the field contours also contribute to the breakdown region and breakdown occurs in the middle of the wedge shaped neutral region.

Key words:
Stepped gate; breakdown voltage; LDMOS; LDD; carrier.

1. Introduction

LDMOS devices have an important role to play in smart power and RF power applications [1]. LDMOS is mainly used due to its qualities of ease of integration, thermal stability and high input impedance at high drive current. The LDMOS is also used in base station applications in RF power amplifiers since this provides high power. They can also be easily fabricated with the Silicon process and can therefore be involved in integration along with the CMOS technology. The LDMOS devices work on the principle of RESURF wherein the vertical junction is depleted by the horizontal junction which in turn causes the breakdown voltage to increase [2]. Different LDMOS structures such as, the LDMOS with the drift region under the FOX, stepped gate structure, the shallow trench isolation structure and the silicon on insulator structure have been reported in the various journals. Many studies have been reported to optimize or to change the device structure, doping profiles and they are aimed at improving the breakdown voltage and on state resistance Ron [10], [11], [12], [13], [14], [15], [16], [17], [18]. One of the important structures is the stepped gate structure where there is a thicker and a thinner stepped gate. The thicker stepped gate helps get a higher breakdown voltage and the thinner step over the drift region, helps to get a lower on state resistance. The stepped gate structure which was proposed by Der-Gao Lin, S. Larry Tu et al. [3] is a modification to the LDMOS structure. After this there are many developments to this stepped gate structure. A few of these are based on SOI structures. Radhakrishnan Sithanandam and M. Jagadeesh Kumar simulated [4] an extended p+ stepped gate, on thin-film silicon-on-insulator. The hole current generated due to impact ionization is now collected from an n+p+ junction instead of an n+p junction, thus delaying the parasitic bipolar junction transistor action. The breakdown voltage obtained in this work is around 50 V. G. Toulon, I. Cortés et al. [5] had put forth a structure where the breakdown voltage is high but they have thick oxide everywhere and it is a complex structure. In another work by Han Yang, Zhang Bin et al. [6], a structure similar to the one proposed in this paper is used. Their paper mainly focusses on the study of degradation. The breakdown voltage reported in this structure is 30 V. Masoud Kazemy, Morteza Fathipour etal [7] had extended the work done by M. Jagadeesh Kumar and Radhakrishnan Sithanandam [4] where an extended-p+ region is formed beneath the source. The simulation results show a breakdown voltage of 89 V but at the cost of a complex circuit which needs the implementation of two different gates and different biases. They have also reported a breakdown voltage of 37.7 V for a normal conventional structure. A new hetero-material stepped gate (HSG) SOI LDMOS is shown in [8], where the gate is divided into three sections - an n+ gate sandwiched between two p+ gates and the gate oxide thickness increases from source to drain. The breakdown voltage is around 60V. In another work by M. Jagadeesh Kumar et al. [9] using a stepped gate (SG) for the InGaAs LDMOS, the authors were able to obtain a breakdown voltage of 60 V. These works were primarily concentrated on extended gate structures. The present work proposes a new improved structure which is a modification of the conventional stepped gate structure. The breakdown voltage .is optimized to 68 V which is higher than most of the breakdown voltages reported. This is achieved by spreading out the electric field throughout

Manuscript received April 5, 2017
Manuscript revised April 20, 2017

the LDD region by having a graded LDD structure. The graded LDD is implemented by a two stepped LDD implant. By employing this modification, it was possible to obtain a higher breakdown voltage and it demonstrated an increase over the other structures reported so far.

2. Construction of the Structures

Fig 1 shows the proposed graded LDD structure. The structure has a pbody, an oxide layer, a graded LDD structure which is low doped initially followed by a region which is moderately doped and this ends with the n+ contact. The stepped gate device which has been considered in this work is formed on a p-type epitaxial layer whose concentration is 1e15 cm-3. The LDDs were formed with doses of 0.05e14 cm-2 and 0.25e14 cm-2. The gate oxide is also stepped, the thickness initially being 0.04 µm and the thicker oxide is of 0.232 µm thickness. This structure of two stepped LDDs helps in optimizing the potential and field distribution which in turn optimizes the breakdown voltage. The pbody is formed by doing a selective p implant (boron) and a diffusion step. This decides the active channel of the stepped MOSFET (Fig 1). The thicker gate oxide is formed by diffusing dry Oxygen with trace HCl. This is followed by a photolithographic step and the thinner gate oxide is formed next, by doing a dry oxidation again. The gate is formed next, followed by the formation of the source and drain regions. The source and drain regions are formed by doing an Arsenic implant and the metallization process follows this. This complete process results in a device of length 11 µm. This device has the source ending at 2.2 µm from the edge of the device and the LDD starting at 4 µm, the second LDD and the thick oxide at 4.8 µm and the n+ contact at 9 µm.
The effective length of the pbody is 3 µm. The surface concentrations in the first step of the LDD is 1e16 cm-3 and at the second step it is 7e16 cm-3 as shown in Fig 1.
The process simulation software ATHENA is used for simulating the structure. The device simulation software ATLAS is used in the analysis. The simulation in the breakdown region takes place by the curve tracing algorithm. The Selberrherr's model is used to model the impact ionization.

3. Simulation Results and Discussion

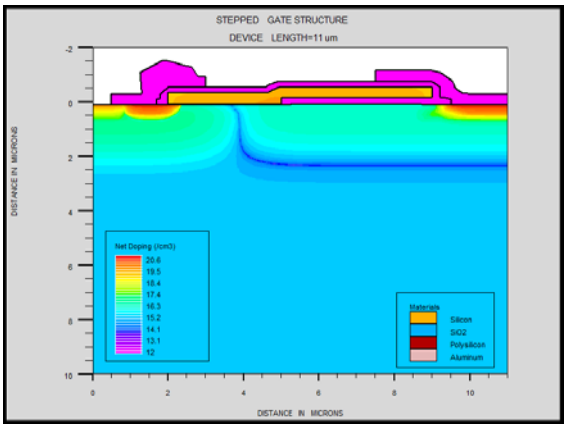

Fig 1. Stepped gate structure

The structure, doses and the concentration were adjusted in order to get an optimum breakdown voltage without compromising the on state resistance. The structure was optimized by forming an LDD first and adding the next step to it. A few experiments were conducted to compare the breakdown voltage of a conventional LDD with that of a graded LDD. The breakdown voltage measurement was done by sweeping the VDS from 0 V to 66 V and keeping the gate voltage constant at 0 V.
The main aim is to optimize the LDD structure with regards to the length of the device and the structure of the device. The first task was to optimize the doping profiles. A few experiments were conducted by keeping the second LDD dose constant at 3.5e14 cm-2 first and changing the doping of the first LDD. The breakdown voltage was at its highest when the first LDD dose was at 5e12 cm-2. A second set of experiments were conducted using the previous structure as a reference, by changing the doping of the second LDD. For all these experiments the device length was kept constant at 11 µm. Another set of experiments were conducted, to study the dependence of the device on the device length by changing the length of the device and finding out the corresponding breakdown voltages.

3.1 Changes in Breakdown voltage with the doping of the stepped LDD structures

The results of the set of these experiments which are outlined in the previous section are given in Table 1 and Fig 2.

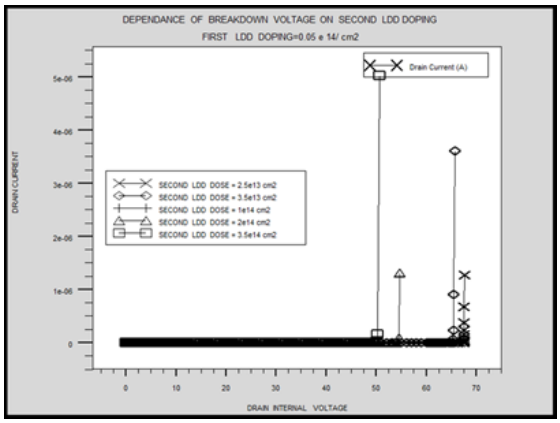

Fig 2. Breakdown characteristics of the stepped gate structure

Table 1. Variation of breakdown voltage by keeping the second LDD dose as 3.5 10 14 cm-2 and changing the first LDD dose.

First LDD implant dose in cm^{-2}	Breakdown voltage in V
5.00e+13	27.06
1.00e+13	40.02
5.00e+12	50.2

From the Table 1. it is seen that the breakdown voltage is high when the first LDD implant dose is at 5e12 cm-2. The second set of experiments were conducted by keeping the first LDD implant dose at 5e12 cm-2 and changing the second LDD implant dose. The results are tabulated in Table 2.

Table 2. Variation of breakdown voltage by keeping the first LDD dose as 5e12 cm-2 and changing the second LDD dose

Second LDD implant dose in cm^{-2}	Breakdown voltage in V	On state resistance in Ω
3.50e+14	50.2	0.012743
2.00e+14	54.68	0.01326436
1.00e+14	58.656	0.014312
5.00e+13	62.458	0.0153789
3.50e+13	65.407	0.01584736
2.50e+13	67.523	0.01646036
1.70e+13	62.67	0.0172
1.00e+13	55.579	0.01833416

From Table 2 it is seen that the breakdown voltage changes from 50.2 V to 65 V for a change in second LDD implant dose from 3.50e14 cm-2 to 3.50e13 cm-2 and then decreases to 55 V when the dose is decreased to 1.1e13 cm-2. The on state resistance values were also calculated and they range from 0.012 Ω to 0.018 Ω. The width of the structures is taken as 1µm which is a standard for Silvaco 2D simulation.

3.2 Dependence of the breakdown voltage on the device length

The next step in optimizing the device structure is to find out the device length which gives the best breakdown voltage. The structure with the highest breakdown voltage in the previous section was considered and its length was changed to analyse the effect. From Table 2 it is obvious that the highest breakdown voltage is achieved when the graded LDD dose is at 2.5e13 cm-2. The changes in the breakdown voltage and the on resistance with device length are given in Table 3.

Table 3. Variation in breakdown voltage with device length

Device length (µm)	Distance at which n+ contact starts in µm	Breakdown voltage (V)
9	7	52
10	8	61.444
11	9	67.523
12	10	69.503
14	12	69.312
15	13	68.9

3.3 Comparison of the breakdown voltages of structures with single and double LDDs

The breakdown voltages of the step gate structure with a single LDD is compared with that of a double LDD step to confirm the enhanced performance of the graded LDD structure. Both the simulations were carried out for the same device length of 11 µm. Fig 3 shows the breakdown voltage curves plotted for both the structures.

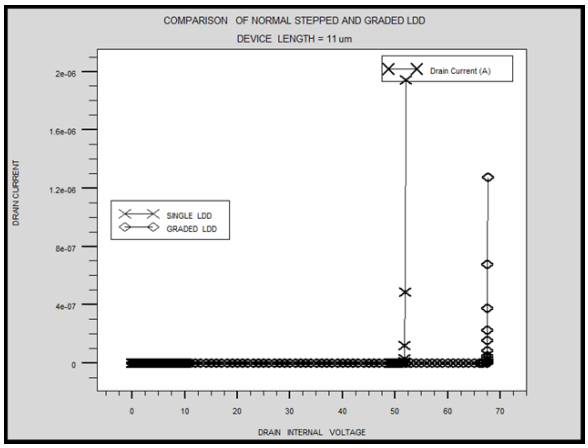

Fig 3. Breakdown voltage curves of a normal stepgate structure and a stepgate structure with two stepped LDDs both with the same device length.

4 Analysis

4.1 Discussion on Change in Breakdown voltage with change in LDD doping

As can be seen in the earlier sections the breakdown voltage depends on the LDD doses and the channel length. To understand this behavior, 2D analysis of the various parameters such as the horizontal and vertical electric field patterns, the impact generation profiles, Generation /recombination / impact generation before and after breakdown, the carrier concentration, electron and hole current densities and the conduction current densities of the structure were analyzed. These analyses were done at a voltage just above the breakdown voltage.

First the analysis was done on the dependence of the breakdown voltage on the LDD doping. As can be seen in Table 2 the breakdown voltage increases and then decreases for an increase in LDD doping. The analysis is carried out for three cases. The first case considered here occurs when the breakdown voltage is low at 50.2 V, this occurs when the graded LDD dose is at 3.5e14 cm-2 and the first LDD dose at 5e12 cm-2 (Refer Table 2). The impact generation profile in Fig 4 shows that the field free region is moving more towards the source under the gate. The maximum vertical and horizontal electric fields of -3 e5 V/cm occur around 6 µm as can be seen in Fig 4 .We can see that it is closer to the point where the LDD starts grading. It is clear from these facts, that the depletion region is confined to a small length or only to the first LDD region. As a result, the field at the tip of the field free region becomes high and leads to the low breakdown voltage.

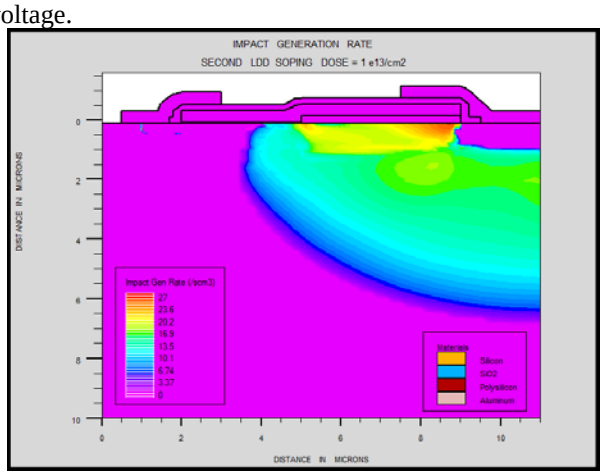

Fig 5. Profile of impact generation rate with second LDD doping of 1e13 cm-2

The same reasoning holds good for the structure with only one LDD implant. As shown in Fig 3 the stepped gate LDMOS structure without the graded LDD has a breakdown voltage of 51.83 V which is closer to the breakdown voltage of the structure with the lowest graded LDD doping. An interesting picture evolves when the graded LDD implant dose is at 2.5e13 cm-2. The breakdown voltage for this dose is high at 67.523 V. Analysis was done on the electric fields and impact generation rates and the following observations were made.

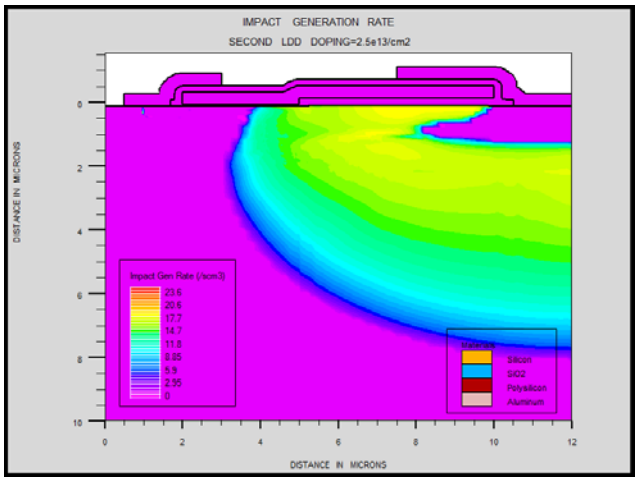

Fig 6. Profile of impact generation rate with second LDD doping of 2.5 × 1013 cm-3.

Fig 6 displays the impact generation contour map for the 11 µm LDMOS device with 66 V on the drain and 0 V on the gate and the substrate, the back contact. The map shows that close to n+ drain the 66 V potential contour extends below the gate away from the n+ drain region. It can be seen from the shape of the contour, that there is a potential gradation between this constant potential region and the gate. This constant potential region narrows down towards source and disappears at a distance of about 8 µm from the beginning of the device, approximately 1.2 µm from the gate edge on the drain side. This kind of potential distribution leads to formation of wedge shaped neutral region in silicon below the gate. The width of the neutral region decreases as we move away from the drain side edge.

Based on the analysis carried out (Fig 8) it is evident that it is the vertical electric field which is dominating in this case. There is a high electric field region between the neutral wedge region and the gate. The breakdown voltage occurs around the middle of the graded LDD as shown in Fig 7 which makes the breakdown large.

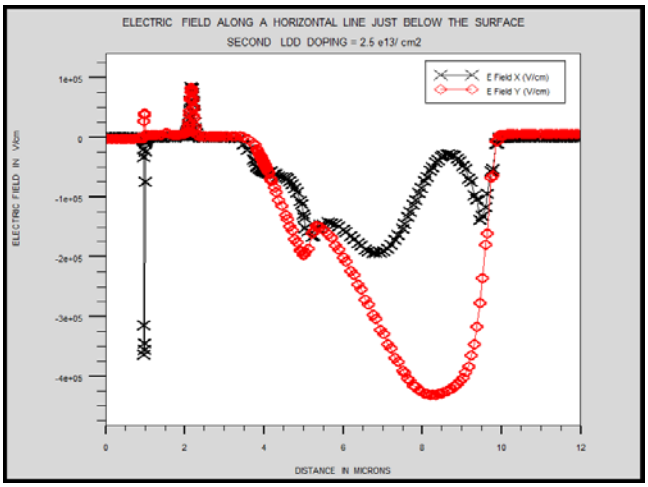

Fig 7. Vertical and Horizontal Components of Electric Fields along a Horizontal Line drawn just below the surface with the first LDD implant dose at 5e12 cm-2 and the second LDD implant dose at 2.5e13 cm-2

The width of the neutral region close to the drain can be calculated by approximating the region as a MOS structure. The MOS structure considered here is formed on a n type semiconductor. A negative bias is applied to the gate electrode which depletes the surface. The gate bias gets divided into two portions for such a MOS structure - one across the oxide layer and the other to support the depletion region in the semiconductor. The division of the bias across the oxide layer and the depletion layer can be determined from basic MOS physics.

Total bias across the MOS structure is given by

$$V = V_{ox} + V_s, \qquad (1)$$

where V is the total bias across the structure, Vox drop across the oxide and Vs drop across the depletion layer in the semiconductor. The drop across the oxide is given by

$$V_{ox} = \frac{Q_s}{C_{ox}} \qquad (2)$$

where Cox is the oxide capacitance per unit area and Qs is the depletion charge in the semiconductor per unit area.

The depletion charge can be expressed in terms of the voltage drop across the depletion region and the doping concentration in the depletion region as

$$Q_s = \sqrt{2\varepsilon_s q N_D V_s} = \sqrt{2\varepsilon_s q N_D (V - V_{ox})} = V_{ox}.C_{ox} \quad , \qquad (3)$$

and the width of the depletion layer can be obtained from

$$w_s = \frac{Q_s}{q.N_D} \quad . \qquad (4)$$

The width of the depletion layer in the region below the gate at different places can be obtained by solving the equations (1), (2), (3) and (4).The doping concentrations as obtained from simulation data at distances of 8.3 µm and 8.6 µm from the start of the devices in the LDD region are 7e16 cm-3 and 1.1e17 cm-3 respectively. Using these values, the Vox, Vs and the depletion width in the silicon are calculated using the above given equation. The calculated values of Vox and Vs are 45 V and 21 V respectively for the 7e16cm-3 (8.3 µm) and 53V and 13V respectively for 1.1e17cm-3 (8.6µm) structures.The corresponding depletion widths calculated are 0.6 µm and 0.45 µm respectively. These match very well with those obtained from simulation

The voltage at the tip of the region is the same as the applied voltage on the drain. The applied voltage is distributed, along the length of the device. The electric field in this direction is not very high and is not primarily responsible for the breakdown of the device. This can be confirmed by determining $\int \propto$ dx over this path where α is ionization coefficient and is field dependent. $\int \propto$ dx is determined in one of the unpublished works by the same authors using the equations given below [11]. The break down condition is set as that for which the ionization integral

$$\int \alpha dx = 1 \qquad (5)$$

The ionization coefficient α is generally found to have the following dependence on the electric field, where E^{crit} is the critical Electric field.From the experimental data available in literature [11], [12], [13] the following expression relating the ionization coefficient to the electric field has been extracted.

$$\alpha = 74408 * exp\left(-\frac{1.24*1000000}{E_{mean}}\right) \qquad (6)$$

This expression has been used to determine the ionization integral from the electric field data which was obtained from the simulation of the LDMOS structures. The breakdown in simple reverse biased diodes can be modelled based on ionization integral. The ionization coefficient (α) is a function of electric field present and the ionization integral ∫αdx calculated over the length of the carrier path should become equal to unity for breakdown to occur. But the value of α extracted from the simulated stepped gate structures in this work is much smaller than unity. This proves that this simple model holds good for one dimensional structures but in the case of 2D structures like the LDMOS a different approach has to be followed. So there should be some other factor apart from the ionization integral which has caused the breakdown and to find it various 2D analyses were carried out the results of which are given below.

This expression has been used to determine the ionization integral from the electric field data which was obtained from the simulation of the LDMOS structures. The breakdown in simple reverse biased diodes can be

modelled based on ionization integral. The ionization coefficient (α) is a function of electric field present and the ionization integral ∫αdx calculated over the length of the carrier path should become equal to unity for breakdown to occur. But the value of α extracted from the simulated stepped gate structures in this work is much smaller than unity. This proves that this simple model holds good for one dimensional structures but in the case of 2D structures like the LDMOS a different approach has to be followed. So there should be some other factor apart from the ionization integral which has caused the breakdown and to find it various 2D analyses were carried out the results of which are given below.

First it has been observed during the simulations that for drain voltages close to the breakdown voltage the drain current and the substrate currents are almost the same and the source current is very less. The picture becomes different just around breakdown. As the drain voltage approaches the breakdown voltage, the source current starts increasing.

At voltages very close to breakdown and in breakdown condition the drain current and source current are almost equal. The substrate current is very small compared to drain and source currents. This is seen more in long channel devices. This indicates that before the breakdown occurs, the drain current is essentially due to the leakage between drain and substrate. However, after the breakdown a large current flows through the channel region and the substrate plays a smaller role.

The following inferences were made from the analysis. The first one was that the horizontal electric field is always negative or in other words the field direction is towards source. The vertical electric field is negative up to a depth of about 0.8 µm from the edge of gate and becomes positive afterwards. To ascertain the field directions plots of electric vectors were also done and is given in Fig 8.

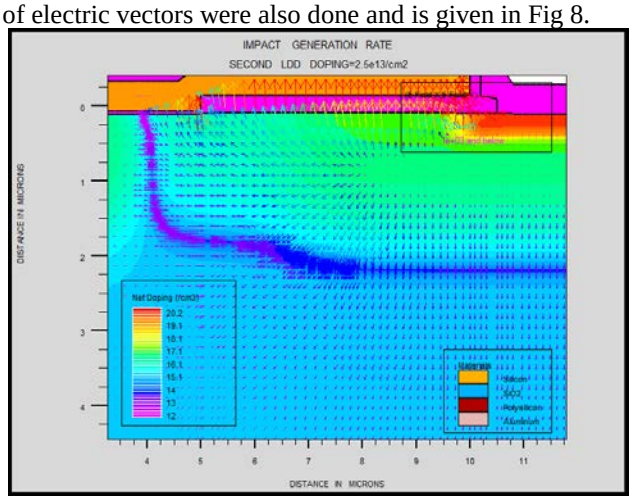

Figure 8. Plots of electric field vectors near the drain region for the 11 µm device

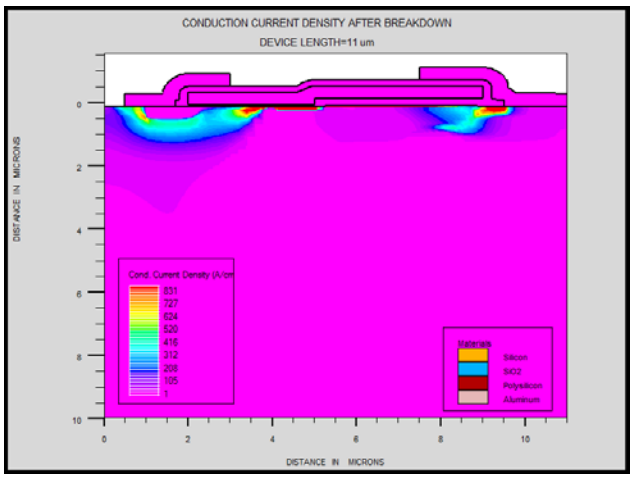

Fig 9. Conduction current density after breakdown in step gate LDMOS for the 11 µm device. Near the drain it is electron conduction and near source it is hole conduction

As a result of these fields the holes generated during the impact generation flow towards the gate and the generated electrons flow downward. This results in an accumulation of holes near the gate edge as is evident from Fig. 9.

As is evident from Fig 8 the potential along the horizontal line is downwards, towards the drain for electrons. Therefore, there is a channel for the electrons in the drain region in the potential well and they flow towards the drain and are collected by the drain. Due to the high electron concentration the drain current also increases to a large value in the breakdown condition.

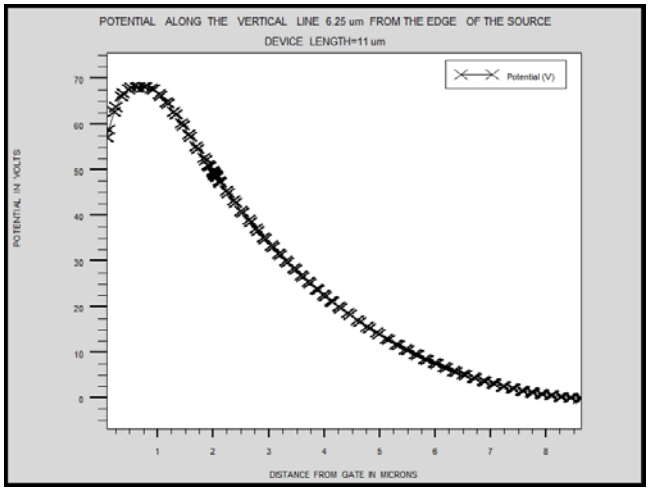

Fig 10. Potential along the vertical line 6.36µm from the edge of the source for the 11 µm device

As is evident from Fig 8 the potential along the horizontal line is downwards, towards the drain for electrons. Therefore, there is a channel for the electrons in the drain region in the potential well and they flow towards the drain and are collected by the drain. Due to the high electron

concentration the drain current also increases to a large value in the breakdown condition. Referring to Fig 8 again, it can be observed that the field direction along the channel in the region, points away from the drain point more towards the source. This facilitates the holes that are created, to move towards the source and get collected by the n+p+ source terminal.

4.2 Discussion on change of Breakdown length with device length

The results of change in breakdown voltage with change in device length are shown in Table 3 and Fig. 3 shows that the breakdown voltage is directly dependant on the device length. The vertical electric field, in the 11 µm device is much higher than the horizontal field, especially near the drain side. Because of the shorter channel length of the 9 µm device, the drain region starts much ahead. Figure 11 gives net doping profiles of the 11 µm and 9 µm devices along the channel, at a depth of around 3 µm below the gate. The doping concentration in the LDD region at the point where the n+ drain starts for the 9 µm is slightly smaller compared to that of the 11 µm device. Because of the shorter LDD region and the lower doping concentration near n+ region, the electric field profile in this region changes and the horizontal field dominates for the 9 µm device unlike the 11 µm device.

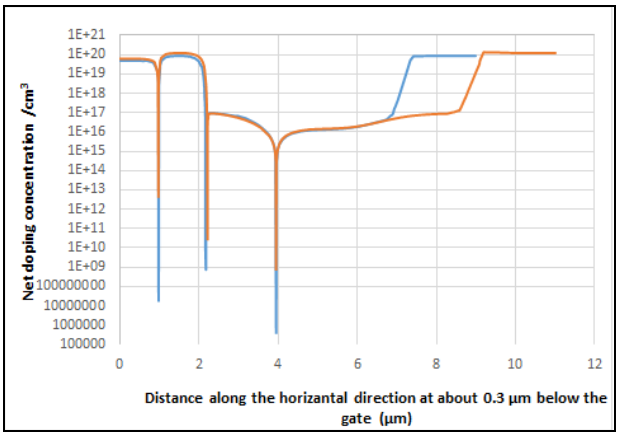

Figure 11. Net doping profile of the step gate structures. In both 9 µm and 11 µm devices the source edge is at 2.2 µm, the p body ends at about 4 µm and the LDD regions starts at this point. The drain region for 9 µm device starts at around 7 µm, while that for 11 µm device at around 8.6 µm

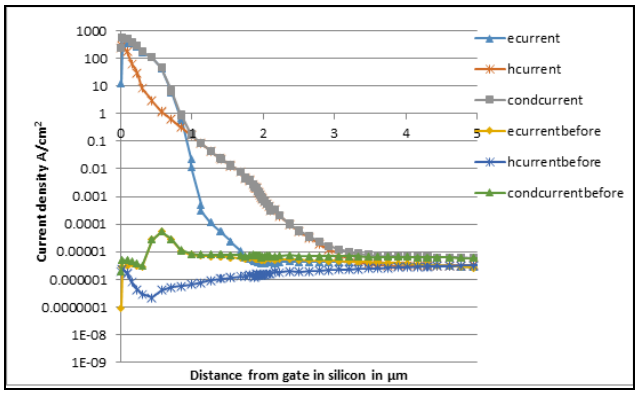

Figure 12. Electron and hole current densities before and after breakdown along a vertical line at a distance of 4.65µm from the edge of the source for the 9 µm device.

As in the case of 11 µm device there is an 8 to 9 orders of increase in the impact generation rate after breakdown compared to before breakdown. Similar is the situation with carrier concentrations. The current components also increase in a similar manner and as Figure 12 shows, near the surface region the electron current dominates.

Thus it can be seen that the breakdown occurs in a different way as the device length increases in the stepped gate LDMOS devices. Analysis of the conduction current densities were also done for the shorter channel device and it was seen that the current flow is confined to the surface in this device. This is in contrast to Fig 9 which shows the conduction current densities of a 11 µm device where the current flow exists upto a depth of 0.8µm.

To get a deeper insight, two more device structures were studied, one without a gate and the other without a step in the gate oxide. All the other specifications were the same as in Fig 1. The cross section of the device without the gate is shown in Fig 13. This device breaks down at 90V. The absence of the gate structures changes the potential pattern and the field pattern. There are no high fields in the vertical direction and the field pattern is symmetrical about the p body and n LDD regions.

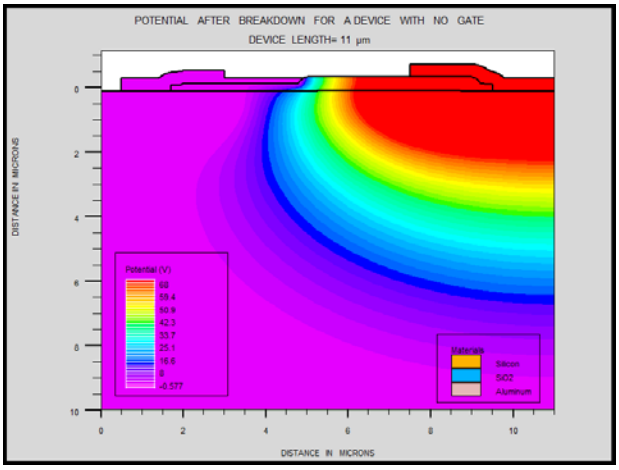

Fig 13 Potential after breakdown in a device with no gate. The device length is 11 µm

In the second structure where there was no stepped oxide, the gate oxide was uniformly formed with a thickness of 40 µm throughout the length of the device. This device breaks down at a much smaller voltage (~ 28V). Thus it can be seen that the presence of stepped gate oxide, LDD region and the doping profiles in the LDD region determine the breakdown voltage. Optimization of these parameters will optimize the device operation.

5. Conclusions

A new stepped gate structure was simulated and analyzed using the process and device simulator tools ATHENA and ATLAS respectively. A high breakdown voltage of 68 V was obtained without compromising on the on resistance which was around 0.015 Ω. The breakdown voltage of a graded LDD stepped gate structure when compared with that of a normal stepped gate structure exhibited an improvement of almost 18 V.

The experiments conducted by changing the first and the second LDD doses to get the highest breakdown voltages showed that, the optimal first LDD dose is 5e12 cm-2 and the second LDD dose is 2.5e13 cm-2. The device structure was further optimized by conducting experiments to see the dependence of the breakdown voltage on the device length and it can be seen that, the highest breakdown voltage is achieved when the device length is at 12 µm. By analyzing the electric field vectors, impact generation and the recombination, it is inferred that the recombination current also contributes to the high drain current after breakdown, unlike simple structures where only the ionization integral is enough to determine the breakdown.

Acknowledgments

The authors would like to thank Prof. Sathyam, Electronics and Communication Engineering Department, Vasavi Engineering College, Hyderabad for the technical discussions which the authors had with him in the analysis of the stepped gate structures.

References

[1] F. van Rijs. “Status and trends of silicon LDMOS base station PA technologies to go beyond 2.5 GHz applications.” Presented at Radio and Wireless Symposium, IEEE, Jan. 2008.

[2] Appels JA, Vaes HMJ, “High Voltage Thin Layer Devices.,” *IEDM Tech Digest*, **Dec. 1979,** Vol.25, pp. 238-241.

[3] Der-Gao Lin, S. Larry Tu, Yee-Chaung See, “A Novel LDMOS Structure with A Step Gate Oxide” Electron Devices Meeting, 1995. IEDM '95., International.

[4] M. Jagadeesh Kumar and Radhakrishnan Sithanandam “Extended-p+ Stepped Gate (ESG) LDMOS for Improved Performance”, IEEE Transactions on Electron Devices, July. 2010, Vol. 57, No. 7.

[5] G. Toulon, I. Cortés, F. Morancho,” Analysis and optimization of a Novel High Voltage Striped STI-LDMOS Transistor on SOI CMOS Technology”, Prague, Czech Republic., Aug. 2012, pp. 122-128.

[6] Han Yan, Zhang Bin, Ding Koubao et.al., “Hot-carrier-induced on-resistance degradation of step gate oxide NLDMOS”, Journal of Semiconductors, **Dec. 2010**, Vol. 32, No. 12.

[7] Masoud Kazemy, Morteza Fathipour “Extended-p+ Stepped Dual Gate (ESDG) LDMOS” Proceedings of the 4th Iranian Conference on Electrical and Electronics Engineering, Gonabad, Iran , 2012.

[8] Radhakrishnan Sithanandam and M. Jagadeesh Kumar “A new Hetero-material Stepped Gate (HSG) SOI LDMOS for RF Power Amplifier Applications”, Proceedings of the 23rd VLSI Design - 9th Embedded Systems, Bangalore, India, Jan. 2010.

[9] M. Jagadeesh Kumar and Avikal Bansal “Improving the Breakdown Voltage, O N–resistance and Gate–charge of InGaAs LDMOS Power Transistors” Semiconductor Science and Technology, Oct. 2012, Vol.27, no.10, Article No.105030.

[10] Kun-Ming Chen, “Performance improvement in RF LDMOS transistors using wider drain contact.,” *IEEE Electr. Device Letters*, Sept, 2013 Vol. 34, no.9.

[11] Ming Qiao, Xi Hu, Hengjuan Wen, “A Novel Substrate-Assisted RESURF Technology for Small Curvature Radius Junction,” in Proceedings 23rd International Symposium on Power Semiconductor Devices & IC's, San Diego, USA, May. 2011, pp.16-19

[12] Min-Hwan Kim, Jong-Jib Ki, “A Low On-Resistance 700V Charge Balanced LDMOS with intersected WELL structure,” in the Proceedings of 15th International Symposium on Power Semiconductor Devices and ICs ***(ISPSD)***, Cambridge, UK, Apr. 2003, pp.220-223.

[13] Helmut Puchner, Sungkwon Lee, "High Voltage LDMOS Transistors Utilizing a Triple Well Structure," in Proceedings of 19th International Symposium on Power Semiconductor Devices and ICs, Jeju, Korea, May. 2007, pp.201-204.
[14] Yuehua Dai, Yuan Hu, "Physics-based Modeling and Simulation of Dual Material Gate(DMG) LDMOS" in Proceedings of Asia Pacific Conference on Circuits and Systems, Singapore, Dec. 2006, pp. 1500-1503.
[15] S. Merchant, R. Baird, "High-Performance 13-65V Rated LDMOS Transistor in an Advanced Smart Power Technologies," in Proc. 27th International Symposium on Power Semiconductor Devices & IC's (**ISPSD**), Toronto, Canada, May. 1999, pp.225-228.
[16] Seiki Ogura, Paul J Tsang, "Design and Characteristics of the Lightly Doped Drain-Source (LDD) Insulated Gate Field-Effect Transistor." *IEEE Journal of Solid-State Circuits*, **Aug. 1980**, Vol. 15, no. 4, pp.424-432.
[17] S. Roji Marjorie, P.A.Govindacharyulu, K.Lal Kishore. "Studies on the dependence of breakdown voltages LDMOS devices on their structure and doping profiles of LDD regions.", presented at Asia Pacific Conference in Post graduate research in Micro Electronics and Electronics, Hyderabad, India, Dec. 2012.
[18] S.Roji Marjorie, P.A.Govindacharyulu, K.Lal Kishore "Dependence of Breakdown Voltage and Other Device Parameters of a Novel LDMOS Structure on Drift Length.

Roji Marjorie S, received her Bachelor of Engineering degree from Govt College of Engineering in 1989. She completed her M.Tech from IIT, Madras in 2000. After productive stints with various colleges in Tamilnadu and Telangana, she is now with Saveetha School of Engineering, Chennai, India.