Review of nano scale MOSFET transistors in high frequency applications

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Summary
This paper reviews the structure and use of nano MOSFET transistors, to achieve significant efficacy in applications of high frequency studies. In this study, we use the transistor model named BSIM4 and comparing the two types of transistors with short channel dimensions of 150 nm and 65nm channel MOSFET technology for prove their performance in radiofrequency applications based on analyzes results obtained from the simulations and comparing with other transistors.

Key words:
MOSFET, the cut off frequency, the maximum oscillation frequency, noise figure, gain substantial, power added effective, third order intercept.

1. Introduction

Scale decreasing of semiconductors is a one of the most controversial aspects of the debates for the instruments designers and electronic experts. As at the date of transition to new technologies gradually replacing older technologies, electronic instruments size has also decreased.
With the advancement of technology and science and the production of supercomputers, satellites space, modern equipment telecommunications, electronic circuits in the frequency band UHF from several hundred MHz to 30GHz and above, wireless and broadband bandwidth of 2GHz to 200GHz etc. and to consequently, the need to process high frequencies in less time, reduce manufacturing costs, reduce power consumption and reduced dimensions used instruments keeps us decided that we use new technology called nano transistors.
Results of geometry reduce CMOS[1] technology are very interesting to improve radiofrequency efficiency in the flat MOSFET[2] body type SOI. Due to improved performance in Radio frequency MOSFET small sizes, currently integrating circuits of 2 or 5 GHz radiofrequency and baseband in frequency signal CMOS technology with possible combination in throughput. In addition the research, the applications range from pure CMOS processes can be implemented millimeter waves [1], [2].

The aim of this study demonstrate the suitability of logic CMOS with 65 nanometers for applications is the radiofrequency Despite the problems raised. Be especially careful, features of radiofrequency, such as ft[3], fmax[4], NFmin[5], PAE[6], P1dB[7], gm/gds[8], IM3[9] and the IP3[10] CMOS technology, 65 nm and 150 nm technologies mixed signal in throughput are compared.
To solve this problem, we use technology called Multi Fingers Gate MOSFET or BSIM4[11] model. A sample of N-type from this technology, shown in Figure 1. To check the characters such as threshold voltage, sub-threshold slope, DIBL[12] in this, we will use transconductance allowing mobility of electrons. This can be characters Changes in exchange for length, width and number of fingers gate be analyzed. 65nm and its single gate length (W) in the range between 4mμ to 40mμ the width of the gate 160mμ for comparing performance used in throughput. Multilingual N-type MOSFET technology also compared with 150nm. Gate length 180nm, gate width 160mμ between 1mμ to 20mμ with a total reviews elderly.

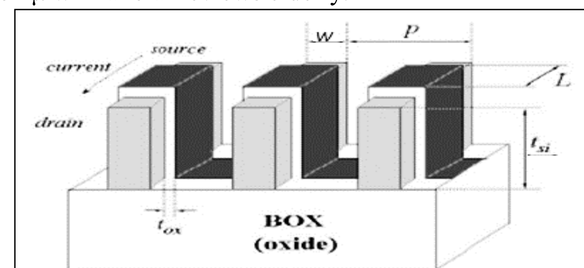

Fig.1: Multi fingers gate MOSFET model BSIM4.

MOSFET N type with different lengths technology dimensions shown in Table 2 for 65nm and in Table 3 for 150nm technologeis. Gate fingers optimization is very important to achieve the best performance in RF applications. Figure 2 shows a simplified equivalent circuit of small signal MOSFET examined in this section shows. The equivalent circuit parameters include noise factor (γ_0)

[1]-Complementary Metal Oxide Semiconductor.
[2] - Metal Oxide Semiconductor Field Effect Transistor.
[3]- Cut-Off Frequency
[4]- maximum oscillation frequency
[5]- Lowest Noise Figure.
[6]- Power Added Efficiency.
[7]- Comparable Point 1dB.
[8]- Inherent Gain.
[9]- Third Order Distortion Intermodulation.
[10]- Third order Intersection Point.
[11]- Berkeley Short Channel IGFET Model.
[12] - Drain Induced Barrier Lowering.

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also extracted. Drain and source of strength results in Table 3 and the lowest values Ids and gm also shown.

Table1: parameters for the 65 nm and 150 nm technologies

Technology	*Vth(v)*	*Vdd(v)*	*Lg(nm)*	*Tox(nm)*
150Nm	0.3	1.5	180	3
65 Nm	0.28	1.2	60	2.2

Table 2: different length dimensions in the 65 nm Technology

Finger length(mμ)	0.4	0.8	1	1.6	2	3.2	4
Number of fingers (NF)	160	80	64	40	32	20	16

Table 3: different length dimensions in the 150 nm Technology

Finger length(mμ)	1	1.2	2	5	8	10	20
Number of fingers (NF)	160	128	80	32	20	16	8

2. Simulations and Analysis of Results

For simulation of the new MOSFET technology called BSIM4 multilingual and simulation Comparison of different parameters and results from the two types of channel length of 65nm and 150nm MOSFET technology with each other, will be used.

3. Drain current-voltage characteristic values

Figure 2 shows the simulation results of characteristics drain current versus drain-source and gate-source voltage in the 65 nm and Figure 3 shows the simulation results of 150 nm Technologies in the same bias points.

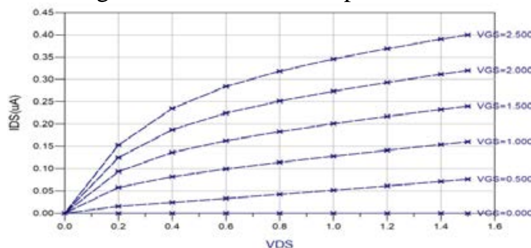

Fig. 2: drain current versus drain-source and gate-source voltage characteristics in the 65 nm technology

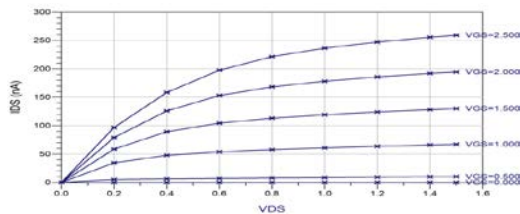

Fig. 3: drain current versus drain-source and gate-source voltage characteristics in the 150 nm technology

The features of both technologies result is an output from a reduction in channel length dimensions in the same bias condition, the achieved drain current from 65nm technology is a 0.4uA where from the 150nm technology is a 260nA. The effect of this be seen as an increase in other parameters.

4. Cutoff frequency, and maximum oscillation frequency

Cut off frequency (ft) is defined as the frequency where the current gain flow is equal to 1, while the maximum oscillation frequency (fmax) is defined as the frequency where power gain be equal to 1. Cut off frequency and maximum oscillation frequency and can be calculated as follows equations:

$$f_t = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \approx \frac{1}{2\pi} \cdot \frac{V_{sat}}{L_g} \quad (1)$$

$$f_{max} = \frac{f_t}{2\sqrt{g_{ds}(C_{gs}+C_{gd})+2\pi f_t R_g C_{gd}}} \quad (2)$$

The features of both technologies result is an output from a reduction in channel length dimensions in the same bias condition, the drain current achieved from 65nm technology is a 4mA where from the technology 150nm is a 0.27mA. The effect of this be seen as an increase in other parameters. In this regard gm represents the transconductance, Cgs and Cgd represents the gate-source and gate- drain capacitance an important loss. Gds is output conductivity coefficient, Rg and Rs represents the gate and source resistances, Vsat is a factor of saturation velocity. Equations 1 and 2 shows that the cut off frequency by reducing as the gate length dimensions reduce, and maximum oscillation frequency increases not only depend heavily on gm and gds, but is also dependent to the noise effect. Figure 4 shows the cut off frequency achieved in the unit current gain of 65 nm and Figure 5 shows the cut off frequency achieved in the unit current gain of 150 nm technologies.

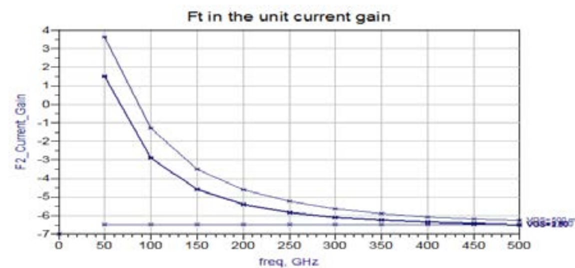

Fig. 4: cut off frequency achieved of 65 nm technology

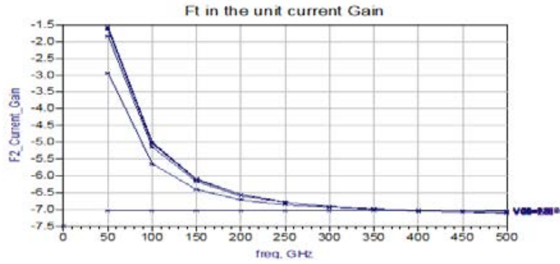

Fig. 5: cut off frequency achieved of 150 nm technology

They are the results of any resulting technology by reducing the size of the channel length, cut-off frequency of 70 GHz from 65 nm technology obtained and the cut-off frequency of 45 GHz obtained from 150nm technology achieved in unit current gain.
Figure 6 shows the maximum frequency of oscillation in unit power gain from 65nm and figure 7 shows the maximum frequency of oscillation in unit power gain from 150nm comparing the features in the both of technologies. Find obtained oscillation frequency obtained from the 65nm is a 270 GHz and 230 GHz in the 150 nm technology in unit power gain.

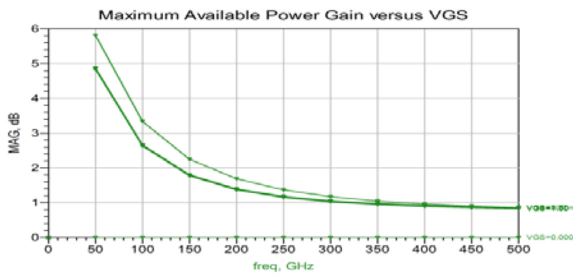

Fig. 6: maximum frequency of oscillation in 65nm technology

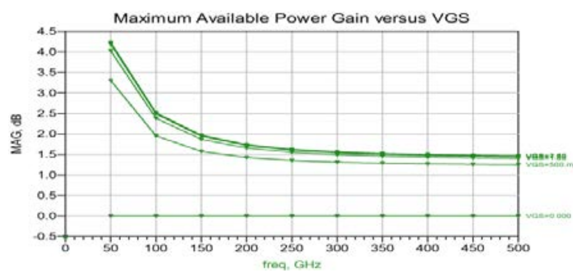

Fig. 7: maximum frequency of oscillation in 150nm technology

5. The Maximum Gain Available: MGA

Figure 8 shows the maximum gain available of 65 nm and Figure 9 shows the maximum gain available of 150 nm technologies. We obtained the maximum gain equal 17.2 dB from 65nm technology and 6.12 dB from 150 nm technologies in the same bias condition.

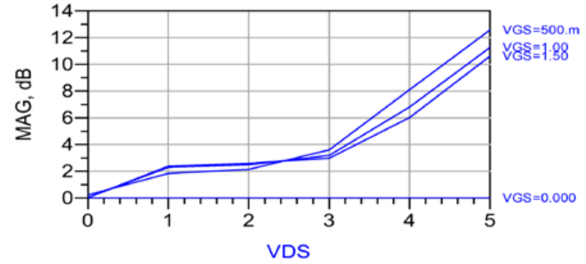

Fig. 8: maximum gain available of 65 nm technology

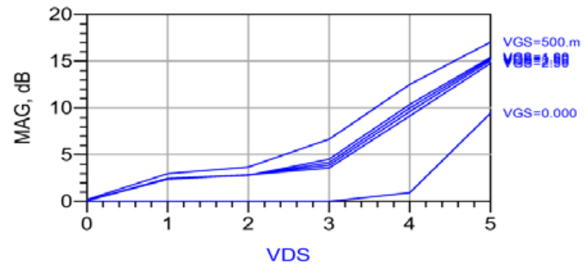

Fig. 9: maximum gain available of 150 nm technology

6. Noise figure: NFmin

Noise figure is a ratio of signal to noise in the ratio of signal to noise ratio in input network to output in high frequency circuits. The thermal noise is the main source of noise in CMOS for high frequency applications. To demonstrate the thermal noise of the lowest noise figure (NFmin, Fmin) is shown by the following equations.

$$F_{min}=1+2\frac{f}{f_t}\sqrt{\gamma_{gm}g_{m(R_g+R_s)}} \quad (3)$$

$$R_n=\frac{\gamma_{gm}}{g_m} \quad (4)$$

$$NF_{min}=10\log 10\, F_{min}\ [dB] \quad (5)$$

In this regard, the equivalent noise resistance Rn and gmγ factor is dumped into streams called drain noise and noise parameters related to an important loss. $\overline{I_d^2}$ in the frequency broadband shows with equation (6). [4]

$$\overline{I_d^2}=4KT\gamma_{gm}g_m\,\Delta f \rightarrow 4KT\gamma_{gd0}g_{d0}\Delta f \quad (6)$$

In this regard gd0 conductivity in channels, Vds= 0, γgm and γgd0 have added noise factors referred to gm and an important loss gd0. Theoretically γ value in the long channel is gm = γgd0 =2.3 in the saturation region. However, the value of γ in the short-channel modulation and greater than 2.3 and gm ≠ γgd0. [4], [5], [6], [7]

The equation 5 prove that the NFmin extremely depends on γgm and noise elements. Figures 10 shows the noise figure measuring in 65nm and Figures 11 shows the noise figure measuring in 150nm technologies. The values measured in the biased points Vds=5v,Vgs=1.5v against 1 GHz frequency, and the results of simulations shown That are reduced in size piece lowest noise figure and reduce the saturation. By reducing the gate fingers gate resistance (Rg) also decreases. However, with the increasing number of gate fingers, gate-drain capacitance (Cgd) also increases.

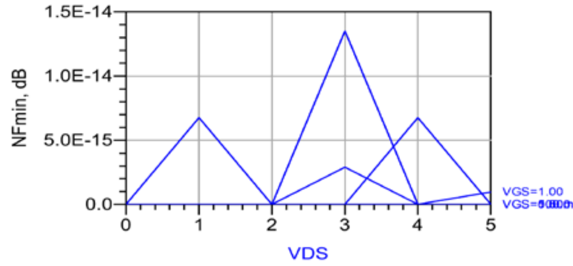

Fig. 10: noise figure measuring in 65nm technology

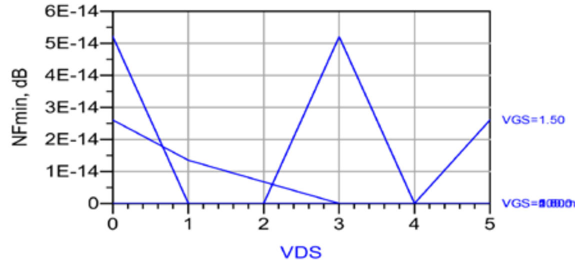

Fig. 11: noise figure measuring in 150nm technology

7. Inherent Gain: gm/gds

Inherent gain is the division of transconductance (gm) on the output conductance (gds). As shown in Equation (7), in saturation velocity, gm by inverting gate oxide thickness decreases, whereas the gds increase as Vds/L due to increase drain induced barrier (DIBL) according to the equation (8) increases. In addition to the Inherent gain L/Tox linked to equation (9).

$$g_m \propto W \frac{V_{sat}}{t_{ox}} \tag{7}$$

$$g_{ds} \propto \frac{V_{ds}}{L} \tag{8}$$

$$\frac{g_m}{g_{ds}} \propto W \frac{V_{sat}}{V_{ds}} \cdot \frac{L}{t_{ox}} \tag{9}$$

Till the thick gate oxide can't be reduced as gate length, inherent gain will be reduced with scaling progress. [8]

8. Large signal and features of distortion

Large signal and distortion features of are used to define the nonlinear analog circuit properties. Large signal and distortion features are calculated by the Load-Pull system and can be measured.

9. Power Added Efficiency and GA[13]

Power Added Efficiency can be calculated by the below equations:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{10}$$

$$PAE0\left(1 - \frac{1}{G_a}\right) \tag{11}$$

In this equations, Pdc is a dc gain and Ga is a Associated Gain. In the low frequency of 1 / Ga equal to zero and the result is a PAE0 of PAE. PAE0 50% yield on the A class and 79% from B class performance. By using large signal cut off frequency, Associated Gain equal to:

$$G_a = \left(\frac{f_{c,ls}}{f}\right)^2 \tag{12}$$

$$F_{c\,,\,ls} \propto f_{max} \tag{13}$$

Large signal cut off frequency approximately equal 30% of the maximum frequency of oscillation in HEMT technology and the amount of large signal cut off frequency in CMOS technology equal to 50% of maximum oscillation frequency obtained. [9], [10]

10. Third Order intersection Point: IP3

Third Order intersection Point explain the properties of non-linear junction piece is made to measure. Third Order intersection Point also be referred to the input-output IIP3 and OIP3. Third order modulation distortion IM3=62.3dB, OIP3=12.8dB of 65nm technology and IM3=8.53dB, OIP3=4.13dB of 150nm technology achieved and represents a nonlinearity of the instrument. To reduce distortion, IP3 should be in high possible amount and IM3 in the least possible amount.

11. Conclusion

In the context we compared the characteristics of the application and features in high radio frequency, and in each case based on the evidence and the research results were presented, we find that the semiconductor metal oxide

[13]- Associated Gain.

components according to the following terms as superior technology to increase performance in high frequency circuits were selected.
1- Scaling capability.
2- Zero power losses in the logical circuits.
Among the instruments scaling advantages compared to other made following:
1- Reduced capacity in the junction capacities.
2- Increase speed in the digital circuits.
3- Reduce power losses, delays and increasing the density of circuits for digital systems.
4- Reduce supply voltage.
As is scaling dimensions has a benefits, due to the effects of it for the detailed design is also very important and vital piece suits respectively. Among these works:
1- Electrical fields increase due to lack of proper scaling supply voltage.
2- Impossibility of reducing the internal potential of the piece.
3- Problems in reducing the size between source-drain junctions.
4- Reduced mobility due to great influence on the substrate.

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