NANOMOSFETs scaling challenges and novel approaches to solve them

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Abstract
This paper describes a comprehensive, simulation based Scaling challenges of MOSFETs including Power and performance management, Polysilicon depletion effect, Quantum effects, Gate tunneling, Threshold voltage roll-off and DIBL and Hot-carrier degradation. After that, then we propose some Technology boosters to decrease a device design, performance characterization, and the impact of statistical variability such as a Stress engineering, Performance enhancements due to strain, High permittivity gate dielectrics, High-k/metal gate and Metal gate on nanometer bulk MOSFETs. For the simulations and show the results, we used the Tcad simulation software.
Key Words:
MOSFET, DIBL, SCE, Quantum effects, Stress engineering.

1. Introduction

The scaling of the MOSFET devices has continued from its first introduction in integrated circuits four decades ago. This has resulted in doubling the component density on a single chip by proportionally scaling of the transistor dimensions over a period of time. This reduces the cost per function and delivers more functions at the same time, which is the essence of the famous Moore's law [1]. At the same time the scaling leads to improved performance while controlling the power consumption by reducing the supply voltage and carefully tuning the design. Schematically shown in Figure 1, a MOSFET consists of two back-to-back connected p-n junctions. The gate voltage applied across metal-oxide semiconductor (MOS) capacitor creates an inversion channel connecting the source and the drain, and controls the carrier density in it. From an operational point of view, the MOSFET has two critical structural parameters, namely gate length and gate dielectric thickness. MOSFET scaling affects both lateral and vertical device dimensions. While the reduction of the lateral dimensions increases the transistor density in a chip, the reduction of the oxide thickness is needed to ensure good electrostatic integrity.

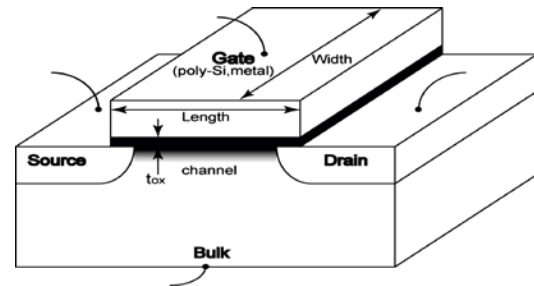

Fig. 1 Schematic view of a surface channel MOSFET.

2. Scaling challenges of MOSFETs

2.1 Power and performance management

A major challenge for further device scaling is the control of the circuit power consumption within acceptable limits. In CMOS circuits, the total consumed power can be split into mainly active switching power Pactive and standby leakage power Ppassive [2][3]. Pactive is the active switching power, proportional to the number of switching circuits Nactive, switching frequency f, load capacitance per circuit Cload, and supply voltage.

$$P_{active} = N_{active} C_{load} V_{dd}^2 f \quad (1)$$

Ppassive is the standby leakage power, proportional to the number of passive, non-switching circuits Npassive, supply voltage, and off-state leakage current.

$$P_{passive} = N_{passive} V_{dd}\, I_o \exp\left(-\frac{V_{th}}{S}\right) \quad (2)$$

Where I_o is a drain current at threshold voltage, and S is the device sub-threshold slope. The best value of S is limited to 60 mV/dec at room temperature T = 300K, and depends on the so-called body effect coefficient m.

$$s = \ln 10 \frac{KT}{q} m \rightarrow \ln 10 \frac{KT}{q}\left(1 + \frac{\varepsilon si/w_{dm}}{C_{ox}}\right) \quad (3)$$

Where K is the Boltzmann constant, εsi is the silicon permittivity, Wdm is the width and Cox is the gate oxide capacitance per unit area. Since the down-scaling of the device dimensions increases circuit integration density, Nactive typically increases as a result. f is in general

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inversely proportional to the transistor switching delay, and hence increases with scaling, but this is compensated by the reduction of Cload, by the factor of dimension scaling, as seen from Table 1.

Table 1: Scaling principles for MOSFET device and circuit parameters.

Scaled parameters	Constant field scaling	Generalized scaling
Dimensions (L, W, tox, xj)	1/K	1/K
Voltage (V)	1/K	α/K
Doping concentration (Na, Nd)	K	αK
Electric field (E)	1	α
Depletion-layer width (Wd)	1/K	1/K
Capacitance (C=εA/ tox)	1/K	1/K
Inversion charge density (Qinv)	1	α
Carrier velocity (v)	1	α
Current, drift (I)	1/K	α^2/K
Delay time/circuit (τ~ CV/I)	1/K	1/ αK
Power dissipation/circuit (P ~ VI)	$1/K^2$	α^3/K^2
Power-delay product/circuit (Pτ)	$1/K^3$	α^2/K^3
Circuit density (∝1/A)	K^2	K^2
Power density (P/A)	1	α^3

2.2 Poly silicon depletion effect

While the channel doping concentration increases with scaling to maintain electrostatic integrity, the poly silicon doping concentration remains limited to 1019~1020cm-3 due to doping solid solubility limits. We can see the effect of the temperature to the doping concentration and depth increases in figure 2. With This, in combination with the extreme scaling of the gate oxide thickness, results in the degradation of the gate capacitance and trans conductance [4][5].This degradation is due to the increase of the effective oxide thickness, resulting from the poly silicon depletion layer when the device is operated at inversion.

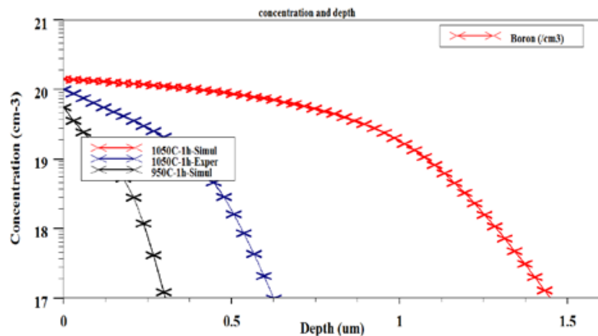

Fig. 2 The effect of the temperature in three levels, to the doping concentration and depth.

An analytical expression for the threshold voltage shift poly ΔVth due to the poly silicon depletion effect can be obtained from the Poisson equation, by including the poly silicon region [6].

$$\Delta V_{th}^{poly} = 2\psi_B \frac{N_{sub}}{N_p} \quad (4)$$

Here ψ_B is the difference between intrinsic and extrinsic Fermi levels in the substrate, and N_{sub} and N_p are the doping concentrations in the substrate and poly silicon, respectively. As stated earlier, an increase of substrate doping, or a decrease of poly silicon doping, both lead to an increase in threshold voltage.

2.3 Quantum effects

The increasingly strong surface electric field near the silicon/oxide interface creates a potential well, as the energy bands bend to form an inversion channel. This leads to quantum confinement of the inversion carriers, giving rise to discrete sub-bands for motion in the direction perpendicular to the interface and shifting the peak of the inversion charge centroid away from the interface (although retaining free continuum motion in the plane parallel to the interface) [7]. Most of the MOSFET models used in SPICE are based on the quasi-static assumption (QSA), in which an instantaneous charging of the inversion layer is assumed. Hence, circuit simulations will fail to accurately predict the performance of high-speed circuits. The channel of a MOSFET is analogous to a bias-dependent distributed RC network. In QSA, the distributed gate-channel capacitance is instead lumped into discrete capacitances between the gate and source and drain nodes, ignoring the finite charging time arising from the RC product associated with the channel resistance and the gate-channel capacitance Figure3.

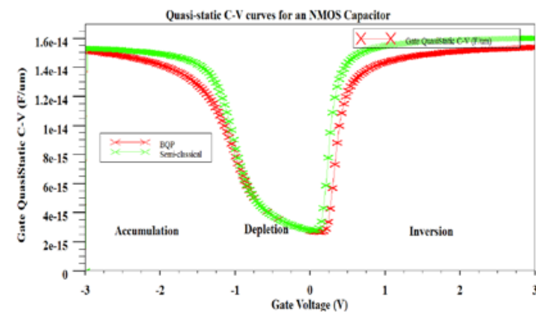

Fig. 3 Quasi-static C-V curves of an NMOS Capacitor from accumulation through inversion showing effects of quantisation such as reduced capacitance and threshold voltage shift.

The quantum mechanical confinement increases the effective oxide thickness, decreasing the inversion charge density at a given bias and in combination with the ground state shift, increases the threshold voltage [8]. Comprehensive 1D and 2D Schrödinger-Poisson solutions demonstrate the impact of quantum confinement on sub-

threshold slope [9], DIBL1, and SCE2 [10]. In Si, the peak of the inversion carrier concentration is located around 1.2nm away from interface [11]. as a result, the effective oxide thickness under inversion bias conditions can be expressed as a equation 5 [8].

$$t_{ox}^{QM} = t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \Delta Z \quad (5)$$

Where ΔZ is the distance of the inversion charge centroid away from interface. Accordingly, the correction to the threshold voltage due to quantum confinement effects can be written in the equation 6 [8].

$$\Delta V_{th}^{QM} = qN_{sub} \left(\frac{\Delta Z}{2\varepsilon_{si}} + \frac{t_{ox}}{\varepsilon_{ox}} \right) \Delta Z \quad (6)$$

In scaled devices with ultrathin-gate oxide, significant performance degradation is attributed to the quantum confinement effects, because of the increasing weight of Δz in the total effective oxide thickness.

2.4 Gate tunnelling

Gate tunnelling current has become a major contributor to static power dissipation, making it comparable to the dynamic power dissipation for sub-65 nm technology generations with pure SiO2 or SiON dielectric [12]. While several mechanisms of gate leakage exist, the most important one in contemporary technology is direct tunnelling, where carriers tunnel through the entire width of the potential barrier formed by the gate dielectric [13]. Direct tunnelling is exponentially sensitive to the physical thickness of the gate dielectric, and for sub-2 nm SiO2 dominates by orders of magnitude the leakage due to Fowler-Nordheim tunnelling or trap assisted tunnelling [14][15].

2.5 Threshold voltage roll-off and DIBL

The SCE relate to the loss of electrostatic control of the gate over the charge in the channel of the transistor. They are associated with the enhanced electrostatic influence of the drain, as the channel length shrinks. This influence is due to the relative enlargement of the depletion layer of the source/drain p-n junction, with respect to the channel length. One measurable manifestation of SCE is the threshold voltage roll-off, It's consists of a rapid reduction in Vth as the gate length is reduced, while maintaining the same vertical doping profile. This is due to the reduction of the lateral potential barrier with gate length scaling.

The Vth roll-off is more dramatic when the drain bias is high. This is expected, since an increase in drain voltage leads to further penetration of the drain-induced field into the channel of the transistor, reducing the lateral potential barrier that is typically controlled by the gate. This effect is termed. Vth lowering due to DIBL can be qualitatively explained by a semi-empirical 'charge sharing' model [16]. For an n-channel MOSFET the correction leads to the following expression for the threshold voltage.

$$V_{th} = V_{fb} = 2\psi_B - \frac{Q'_{dm}}{C_{ox}} \quad (7)$$

$$Q'_{dm} = -qN_a^- \left(\frac{L+L'}{2L} \right) Wdm \quad (8)$$

2.6 Hot-carrier degradation

The Hot-carrier degradation affects reliability and causes long-term instability [17][18], manifested by a threshold voltage increase and drive current reduction. Hot carriers generated by the high electric field near the drain are injected into the oxide with enough energy to create defect states (traps) in the oxide near the silicon/oxide interface [19].

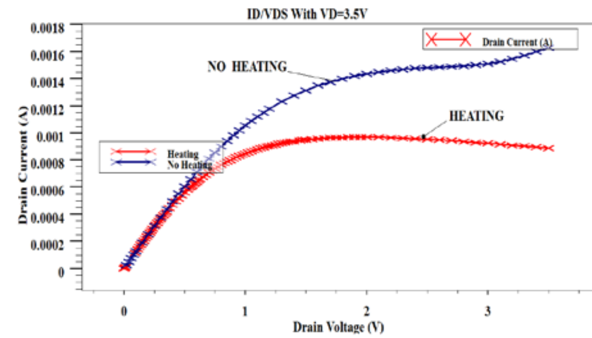

Fig. 4 The effects of hot carriers in the drain current in comparing with no heating.

It is found that only hot electrons having energy of 0.6eV larger than the Si-SiO2 conduction band discontinuity can cause SiO2 degradation in n-channel MOSFETs. The degradation is attributed to the breaking of the SiH bond at the interface. Figure 4 [18][20].

2.7 Statistical variability

In contemporary MOSFETs with sub-50 nm channel length, the number of dopants in the channel depletion is of the order of a hundred, and the number of interface traps is of order of ten. The exact number and location of the discrete dopants and traps fluctuate from device to device. In addition, resist-defined gate line edge roughness is unavoidable. The gate material granularity and the oxide thickness fluctuation of 1 interatomic layer of the Si

1- Drain Induced Barrier Lowering
2- short-channel effects

crystal lattice, also contribute to the microscopic differences in devices with identical macroscopic parameters.

3. Generalized scaling principle

Constant-field scaling principles had been an elemental strategy in designs of MOSFET devices and circuits, and worked as a successful guide for the design down to 1-μm gate length MOSFET. However, the difficulties in reduction of threshold voltage and junction built-in potential exposed the limited flexibility of the constant-field scaling scenario in the design of quarter-micron MOSFET technology. As a result Baccarani et al. proposed a generalized set of scaling rules in 1984, allowing for further device miniaturization under the above mentioned constraints [21]. The fundamental novelty in the generalized scaling rules is to relax the scaling pace of voltage. Assuming that scaled dimensions of MOSFETs are $r' = {}^{r}/_{k}\ (k > 1)$, and introducing an additional scaling factor α >1, the applied potential in the scaled device is $\varphi' = (\alpha/k)\varphi$. Accordingly the scaled device electric field is $-\nabla r'\varphi' = \alpha(-\nabla r\varphi)$. Applying to the Poisson's equations 9.

$$-\nabla r'.(-\varepsilon - \nabla r'\varphi') = \rho' = \alpha k\rho \qquad (9)$$

In the equations 8, ▽ is the gradient operator on dimensional position r , r', φ and φ' is electrostatic potential, ρ and ρ' is space charge density for sub-threshold region respectively for original and scaled devices. The maintenance of constant field requires$-\nabla r'\varphi' = -\nabla r\varphi$. This results in $\varphi' = {}^{\varphi}/_{k}$ and $\rho' = k\rho$ in the light of $\nabla_{r'} = k\nabla_{r}$. This could be achieved by scaling down supply voltage Vdd by the factor k, and by increasing substrate doping Nsub (Na for p-type or Nd for n-type) by the same factor k. It means the channel impurity concentration has to increase by a factor ακ. The rules of constant-field scaling for other device parameters listed in Table 1[25]. The current will be reduced by a factor k according to equation 1. Therefore the power consumption per circuit will reduced by a factor $1/K^2$. It enables the constant of power consumption on a chip.

3.1 Technology boosters

The scaling challenges of recent MOSFET technologies, described in the previous sections, demand the introduction of technology inventions and new materials. Remarkable advancements have already been achieved in channel and gate stack engineering. These innovative technology boosters bring about so-called equivalent scaling where the performance improvement and the aggressive pitch reduction continue to deliver the previously established performance trends, while the actual scaling of certain dimensions or electrical parameters (e.g. Vdd and Vth) has stalled.

3.2 Stress engineering

The effect of mechanical stress in semiconductor devices is not a new phenomenon. During MOSFET fabrication, thermal processes are common. Thermal cycling generates mechanical stresses between materials with different thermal expansion coefficients. In addition, silicon oxidation may cause compressive stress due to volumetric expansion while it consumes silicon. Therefore, shallow trench isolation around active regions can produce significant compressive stress by sidewall oxidation. As the area of a MOSFET gets smaller, the STI-induced stress in the active region becomes significant. The compressive stress from STI can lead to rapidly increased junction leakage [22] and, depending on layout conditions, can degrade the nMOSFET drive current [23]. Intentional use of mechanical stress to enhance the MOSFET performance started at the 90 nm CMOS technology. However, initial trials involved in-plane biaxial tensile stress in standard (001) wafers with a heterogeneous structure composed of epitaxial Si layer grown on a relaxed SiGe virtual substrate. Due to the larger lattice constant of the relaxed SiGe alloy, the silicon layer is stretched in both directions parallel to interface, leading to tensile strained silicon. We can show the stresses inside the stress module in figure 5, calculate stresses before and after etch in figure 6.

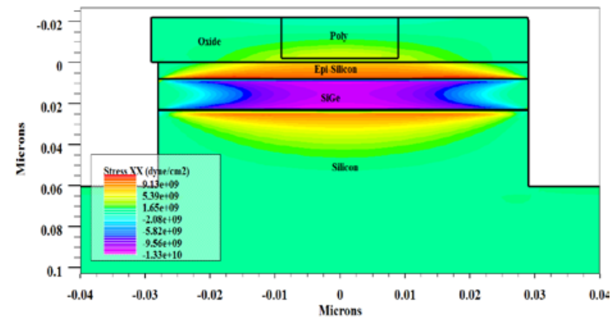

Fig. 5.stresses inside the stress module

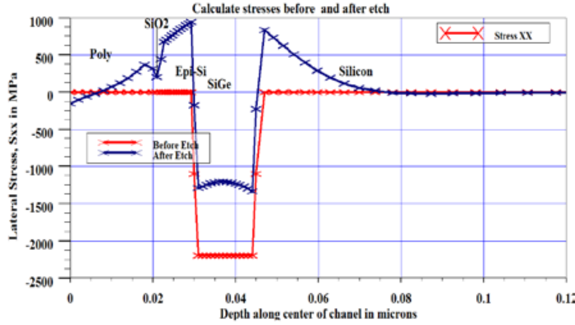

Fig. 6 Calculate stresses before and after etch in

3.3 Performance enhancements due to strain

The biaxial tensile strain splits silicon's six-fold degenerate electron conduction band minima into two-fold Δ2 and four-fold Δ4 minima, and the split energy (in electron volts) due to strain is proportional to the Ge fraction x in Si1-xGex [24].

$$\Delta E_{strain} = 0.67x \quad (10)$$

Since the minima of the Δ4 valleys are barely affected, the minima of the Δ2 valleys are reduced by ΔEstrain. When the substrate is inverted, ΔEstrain add to the quantisation induced splitting between the Δ2 and Δ4 sub bands, making it energetically unfavourable for carriers to populate the Δ4 valleys. Hence all the inversion charge populates the Δ2 sub bands that have smaller effective mass in the transport direction along the channel, compared to the transport mass for Δ4 carriers Additionally, the increased energy split between the Δ2 and Δ4 valleys reduces intra-valley scattering, thus further enhancing mobility[25][26]. The application of uniaxial strain along the channel has an impact on the electronic structure of the Si channel in a similar way, and therefore enhances electron mobility through the same mechanism as biaxial strain. Theoretical calculation shows that uniaxial strain offers more advantages over biaxial strain such as less band gap narrowing [27]. In the case of holes, compressive stress splits the degenerated valence sub bands, increasing the hole population in the sub band with smaller transport effective mass [26].

3.4 High permittivity gate dielectrics

The replacement of SiO2 by a high-k dielectric stack must satisfy a series of material constraints and process integration conditions. Although there are many potential high-k materials, based on their permittivity, a strict selection rules out many candidates. First of all, from a gate leakage perspective, a suitable conduction band offset is necessary to provide a sufficient barrier. For example, tantalum oxide has an adequately high permittivity of around 25, but the ~0.36eV conduction band barrier is not sufficient to provide any overall advantage over SiO2 [28]. A few high-k dielectrics in Table 2 [28][29].

Table 2: Some essential parameters for selected high-k materials and SiO2.

Material	Bandgap (eV)	Conduction band offset (eV)	Leakage current reduction (ref SiO2)	Thermal stability, Tmax (°C)
SiO2	**9**	**3.15**		
Al2O3	**8.8**	**2.8**	$10^2 – 10^3$	**~1000**
ZrO2	**5.7-5.8**	**1.4-1.5**	$10^4 – 10^5$	**~900**
HfO2	**4.5-6**	**1.5**	$10^4 – 10^5$	**~430-600**
ZrSiO4	**~6**	**1.5**		

3.5 High-k/metal gate

High-k/metal gates were introduced into mass production in 2007 by Intel in the 45 nm CMOS technology generation [30][31]. This is the first time that traditional oxides or oxyd nitrides have been replaced in gate stacks, to enable continuous scaling of the EOT.

3.6 Metal gate

Initially, poly-Si/high-k combination gate stack was considered as a route to improving gate leakage. However theoretical studies and experimental data show a mobility degradation compared to the use of metal gates [32][33]. Table 3 lists the WF[3] of some commonly studied metals for MOSFETs [34]. Depending on the gate dielectric, the work function varies due to differing band alignments. Depending on the gate dielectric, the work function varies due to differing band alignments.

Table 3: Experimental vacuum (effective) work functions of selected metals on various.

Metal/dielectric	Work function (eV)
Al/Al2O3	**3.9**
Al/SiO2	**4.14**
Al/ZrO2	**4.25**
W/SiO2	**4.6-4.7**
Mo/SiO2	**5.05**
Mo/HfO2	**4.95**
Pt/SiO2	**5.59**
Pt/HfO2	**5.23**

3- work functions

Pt/ZrO2	**5.05**
Ni/Al2O3	**4.5**
Ni/ZrO2	**4.75**
TiN/SiO2	**4.2-4.9**
TiN/HfO2	**4.33-4.58 (effective)**
TiN/HfO2	**3.6-5.1 (effective)**

4. Results

In this paper first presented a comprehensive overview of the scaling of key parameters of bulk MOSFETs. It described the scaling rules, constant-field scaling and generalized scaling, and it explored the new scaling features beyond the CMOS technology and the ITRS projections of design and performance over the next generations of devices. Secondly, the scaling challenges facing CMOS were described in detail, including: optical patterning difficulties, the trade-off between power dissipation and performance, the vertical and lateral scaling challenges such as gate direct tunnelling and short-channel effects, reliability and statistical variability. Finally, the technology boosters, such as stress engineering, Performance enhancements due to strain, High permittivity gate dielectrics and high-k/metal gates, all employed to enable continued scaling, were presented.

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