VCO Overload and Frequency Excursions: A non-linear Phenomenon in 2nd order Mixed Signal PLLs

Ehsan Ali†, Nasreen Nizamani†, Abdul Sattar Saand††, Abdul Rafay Khatri†, Ghulam Mustafa Bhutto††

†Department of Electronic Engineering, QUEST, Nawabshah, Pakistan
††Department of Electrical Engineering, QUEST, Nawabshah, Pakistan

Summary
The Charge Pump Phase Locked Loop (CP-PLL) are widelys used component in modern day highly integrated electronic systems involved in wireless communication and smart system applications to perform several functions like frequency synhesis, clock recovery, and clock generation. The CP-PLL is switching device becuase of the triggering nature of the digital phase detector. Mostly a second order CP-PLL is utilized in comsumer electronics applications. The voltage controlled oscillator (VCO) generates signal with frequency excursion due to a non-linear effect, called jump frequencies arising due to the filter impedance. These jump frequencies may lead to overload the VCO. This paper highlights the overload situation of the two different architecture of mixed-signal PLLs. The simulations are performed using fast and efficient Event Driven (ED) model. The effect of jump frequencies on both architectures of the CP-PLL is analyzed.

Key words:
Phase locked loop, VCO, Overload, non-linear system, frequency jumps.

1. Introduction

As we are running through the era of internet of things (IOT) mobile and wireless communications are becoming more and more important. Because the systems working in these applications needs to be heterogeneous and time and energy efficient. Mostly mixed-signal systems like analog to digital converters (ADC), digital to analog converters (DAC), switched capacitor filters and CP-PLL are used [1]-[4]. The CP-PLLs (mostly known as digital PLLs) have gained an important role in modern wireless communication and instrumentation system from several applications like clock generation, frequency synthesis, and clock recovery for several reasons, like easy to design and integrate, and are less costly [5]-[6]. Mostly the CP-PLL as shown in Fig.1 is preferred to achieve a robust operation and prudent designs. The mixed-signal architecture of the CP-PLL is given by an analog and a digital part which produces pulse width modulated behavior. Thus, it is highly complicated to apply the concepts of general feedback theory to characterize and analyze the dynamic behavior of the sampled system [6]-[8]. The CP-PLL is consist of several component forming the loop.

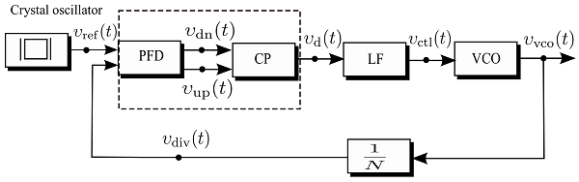

Fig. 1 The mixed-signal PLL representation [11].

A phase and frequency detector (PFD) circuit performing as state machine (as shown in Fig. 2) is used to detect the difference (error) signal. The charge-pump circuit transform this error signal into a suitable form of electrical signal and fed to the loop filter (LF). The LF is used to damp high frequency signals and establish a quasi-dc voltage driving the voltage controlled oscillator (VCO). The VCO generates a signal having frequency proportional to the applied voltage. A frequency divider circuit is implemented in the feedback loop to perform frequency synthesis. A tri-state PFD which is an edge triggered device is preferred in the design of mixed-signal PLLs. due to its wide phase tracking range ($\pm 2\pi$) [3],[8]. Generally the PLL operating with a charge-pump circuits are divided into two categories; the current switched charge-pumps (CSCP) and the voltage switched charge-pump (VSCP). The CSCP can be designed using constant current sources usually providing ideally constant pump current {+Ip,0,-Ip} during each transition cycle of PFD (as depicted in Fig.2). However, it is highly challenging to design a constant. The performance of the conventional CMOS based CSCP circuit suffers from several non-ideal effects like delayed and slew rated current pulses, related to the physical implementations, because the CSCP is used in conjunction with digital PFD circuit. Since these digital circuits are formed from flip-flops so their switching timing accumulates commutation delays [12]. Another issue related to the CSCP is the mismatch between up and down current sources. These problems are directly related to the CMOS implementations of a CSCP [13]. Thus, a VSCP is

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preferred to be implemented in most of the PLL design (like 4046 family) [14]-[15]. However, the VSCP produces an asymmetrical behavior [9]. There are different non-linear effect inside the architecture of mixed-signal PLLs, like non-linear characteristics and frequency jumps in the VCO signal. These frequency jumps are produced due to the passive filters impedance resulting in frequency excursions and that can lead to overload the VCO [8]. To predict the exact switching behavior, different modeling approaches are used, like circuit level simulations and behavioral models [6]-[7]. These methods are very precise but offers different technological bottlenecks, like long simulation time due to high sampling rate, the large amount of produced data, which is difficult to interpret due to the combination of numerous non-linear & non-ideal effects. Mostly, the linear (continuous-time and discrete-time) models are involved to provide starting point of the design and analysis of the dynamic behavior. However, since linear modeling approach is based on early linearization and it is only valid in a small region of locked behavior, they are not sufficient to characterize the frequency excursion and non-linear phenomenon [16]. Behavioral model using Event Driven method are introduced in [17]-[23] are more efficient and fast in computation, since these models are based discrete-time phase equations, so it more easier to study the non-linear characteristics of switched PLL cycle by cycle.

2. Theoretical Consideration of Frequency Excursions and Overload

The output frequency of VCO is dependent on the control voltage (υctrl(t)) established by the LF circuit. When the phase error is detected, a correction signal is pumped to the LF to generate a quasi-dc signal to accelerate or decelerate the VCO. The control voltage is established by charging or discharge the capacitor of LF. The filter impedance is used to stabilize the operation of the CP-PLL. During each cycle of PFD signal, pump current (±IP) is driven into LF impedance responds with instantaneous voltage step of $\Delta\upsilon_{\mathbf{ctrl}}\left(t_{\mathbf{n}}^{+}\right)=\Delta\upsilon_{\mathbf{ctrl}}=I_{\mathbf{p}}R_1$ as shown in Fig.5. At the end of pumping interval, the current switches OFF and a voltage step of equal magnitude in an opposite direction occurs. The VCO produce the signal with frequency following these steps, as demonstrated in Tab1.

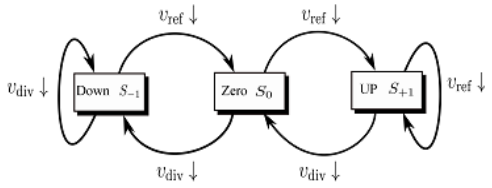

Fig. 2 The state machine representation of the tri-state PFD circuit

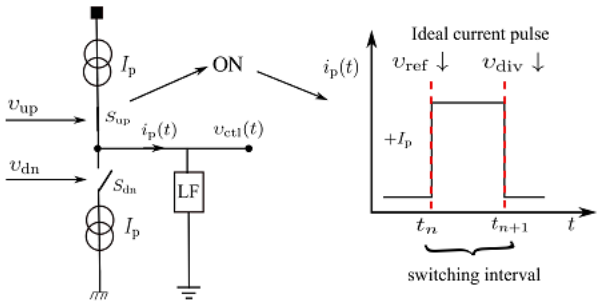

Fig. 3 The current switched charge-pump and its ideal current pulse CP-PLL[11].

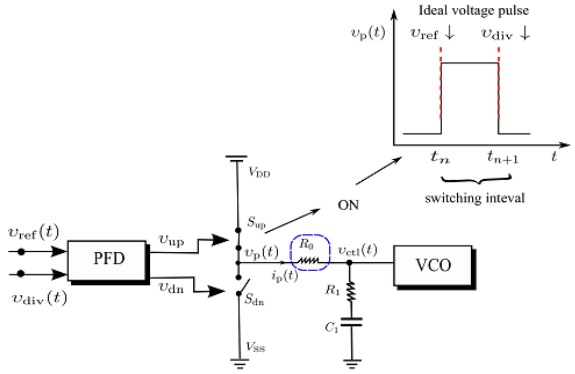

Fig. 4 The voltage switched charge-pump and its ideal voltage pulse[11].

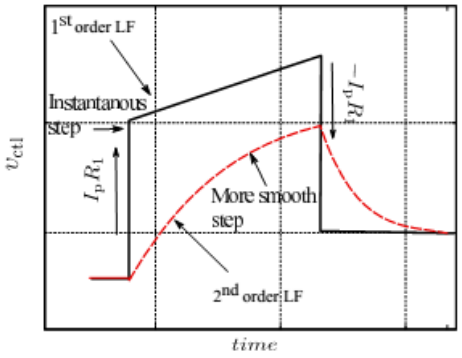

Fig. 5 The voltage jump in first order LF and smooth response by appending capacitor C2 [17].

Thus, there will be frequency excursions of Δωvco = KvcoIpR1 (radian/s) for each pumping cycle. These voltage step $\upsilon_{\mathbf{ctrl}}\left(t_{\mathbf{n}}^{+}\right)$ are constant in magnitude when a CSCP is implemented. To overcome this problem a capacitor is appended to the first order LF to reduce the effect of these voltage jumps. However these voltage steps are not constant when a VSCP is implemented due to its asymmetrical gain [9]-[10]. Since the pump current through a VSCP is established by:

$$i_{\mathrm{p}}(t)=\frac{\upsilon_{\mathrm{p}}(t)-\upsilon_{\mathrm{ctrl}}(t)}{R_0+R_1} \tag{1}$$

Thus, the voltage step can be represented as

$$\Delta\upsilon_{\mathbf{ctrl}}=\pm i_{\mathbf{p}}(t)R_1=\frac{\upsilon_{\mathbf{P}}(t)-\upsilon_{\mathbf{ctrl}}(t)}{R_0+R_1}\times R_1 \tag{2}$$

where $\upsilon_{\mathrm{p}}(t)$ represents {VDD, $\upsilon_{\mathrm{ctrl}}(t)$, VSS} during UP, NULL and DOWN states. The frequency excursions is a non-linear phenomenon exist in the 2nd order mixed-signal PLLs due to LF impedance. If the VCO has a linear characteristic (fvco(t) = Kvυctrl + fv) and the target frequency is relatively near zero (low target frequency and a very high VCO gain) it can happen that the undershoot of the system leads to a negative VCO frequency, this situation occurs especially in CSCP-PLL. To prevent that, the overload limit derived in [8] can be used which defines the boundary when the VCO frequency gets negative. As the VCO follows the voltage step across the load of the LF, a serious consequence of the ripples is the tendency to drive the VCO to produce a meaningless frequency, this overload situation occurs due to pump current [8]. If the magnitude of the jump frequencies exceeds its finite tuning range, then the VCO is overloaded at its input:

$$\upsilon_{\mathrm{ctrl(target)}}(t)=\frac{N\bullet\omega_{\mathrm{ref}}}{K_{\mathrm{v},\omega}}-I_{\mathrm{p}}R_1>0 \tag{3}$$

leads to the overload limit defined in [18]. This restriction must be taken into account on Gardner's stability representation since it becomes dominant for $x=\omega_{\mathrm{ref}}\tau_1>\pi$. The Gardner's stability limit [8] has been investigated in [24] using the Event Driven method, establishes that, the limit is not conservative using for both CSCP-PLL and VSCP-PLL. The principle of Event Driven method is explained in the next sections.

3. Event Driven Modeling Approach

The principle of ED technique is based on the calculating the phase of reference and divider signals at commutation instant as shown in Fig.6. Using this concept, it is enough to calculate all the parameters involved in predicting the switching behavior of the system at triggering point only. Therefore, to calculate the this concept, it is enough to calculate all the parameters involved in predicting the switching behavior of the system at triggering point only. Thus, to calculate the rising or falling event $t_{\mathrm{n+1}}^{\mathrm{ref}}$ occurring from the reference signal is calculated as:

Table.1: Possible state transitions and associated voltage steps in CSCP-PLL.

PFD at t_n^-	Event at t_n	PFD at t_n^+	$\upsilon_{\mathrm{ctl}}(t_n^+)=$
S_0	$\upsilon_{\mathrm{ref}}\downarrow$	S_{+1}	$\upsilon_{\mathrm{ctl}}(t_n^-)+I_{\mathrm{p}}R_1$
S_{+1}	$\upsilon_{\mathrm{ref}}\downarrow$	S_{+1}	$\upsilon_{\mathrm{ctl}}(t_n^-)$
S_{+1}	$\upsilon_{\mathrm{div}}\downarrow$	S_0	$\upsilon_{\mathrm{ctl}}(t_n^-)-I_{\mathrm{p}}R_1$
S_0	$\upsilon_{\mathrm{div}}\downarrow$	S_{-1}	$\upsilon_{\mathrm{ctl}}(t_n^-)-I_{\mathrm{p}}R_1$
S_{-1}	$\upsilon_{\mathrm{div}}\downarrow$	S_{-1}	$\upsilon_{\mathrm{ctl}}(t_n^-)$
S_{-1}	$\upsilon_{\mathrm{ref}}\downarrow$	S_0	$\upsilon_{\mathrm{ctl}}(t_n^-)+I_{\mathrm{p}}R_1$

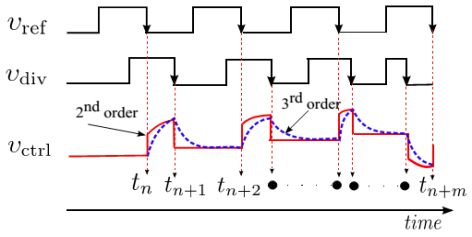

Fig.6: The concept of Event Driven methodology.

$$\varphi_{\mathbf{ref}}(t_{\mathrm{n+1}}^{\mathbf{ref}})=\varphi_{\mathbf{ref}}(t_{\mathbf{n}})+\int_{t_{\mathbf{n}}}^{t_{\mathbf{n+1}}}\omega_{\mathbf{ref}}(\tau)d\tau=2\pi \tag{4}$$

where $\omega_{\mathbf{ref}}(t)$ represents the angular frequency of reference signal. Since the reference frequency is constant for this case, it is easy to determine the time instant of falling event from reference signal as:

$$t_{\mathbf{n+1}}^{\mathbf{ref}}=t_{\mathbf{n}}+\frac{\left(1-\frac{\varphi_{\mathbf{ref}}(t_{\mathbf{n}})}{2\pi}\right)}{f_{\mathbf{ref}}} \tag{5}$$

To determine the time instant of falling event $t_{\mathrm{n+1}}^{\mathrm{div}}$ from the divider signal, the following phase equation has to be solved:

$$\varphi_{\mathrm{div}}\left(t_{\mathrm{n+1}}^{\mathrm{div}}\right)=\varphi_{\mathrm{div}}\left(t_{\mathrm{n}}\right)+\int_{t_{\mathrm{n}}}^{t_{\mathrm{n+1}}^{\mathrm{div}}}\omega_{\mathrm{div}}\left(\upsilon_{\mathrm{ctrl}}(\tau)\right)\,d\tau=2\pi \tag{6}$$

where $\omega_{\mathrm{div}}(t)$ represents the angular frequency of the divider signal. The useful event which is forcing the system dynamics is than further calculated as:

$$t_{\mathbf{n+1}}=\min(t_{\mathbf{n+1}}^{\mathbf{ref}},t_{\mathbf{n+1}}^{\mathbf{div}}) \tag{7}$$

Between two triggering events, the state dynamic changes continuously and υ_{ctrl}, is key parameter to be known at each switching state, and can be represented using state space as:

$$\begin{aligned}x(t)&=\mathbf{a}x(t)+\mathbf{b}\upsilon_{\mathbf{p}}(t)\\ \upsilon_{\mathbf{ctrl}}(t)&=\mathbf{c}^{\mathrm{T}}x(t)+\mathbf{d}\upsilon_{\mathbf{p}}(t)\end{aligned} \tag{8}$$

The control voltage equation is represented as:

$$\upsilon_{\mathbf{ctrl}}(t)=\mathbf{c}^{\mathrm{T}}\left[\Phi(t-t_{\mathbf{n}})x(t_{\mathbf{n}})\int_{t_{\mathbf{n}}}^{t}\Phi(t-\tau)\mathbf{b}\,\upsilon_{\mathbf{p}}(t)d\tau\right]+\mathbf{d}\upsilon_{\mathbf{p}}(t) \tag{9}$$

and the phase equation of the divider signal is represented as:

$$\varphi_{\mathbf{div}}(t_{\mathbf{n}}+1)=\varphi_{\mathbf{div}}(t_{\mathbf{n}})+\frac{2\pi}{N}\times$$
$$\int_{t_{\mathbf{n}}}^{t_{\mathbf{n}}+1}\left[K_{v}\left\{\mathbf{c}^{\mathbf{T}}\begin{bmatrix}\Phi(t-t_{\mathbf{n}})x(t_{\mathbf{n}})\\ \int_{t_{\mathbf{n}}}^{t}\Phi(t-\tau)\mathbf{b}\,\upsilon_{\mathbf{p}}(t)d\tau\end{bmatrix}+\mathbf{d}\upsilon_{\mathbf{p}}(t)\right\}+f_{\mathbf{v},\phi}\right] \quad (10)$$

then to find out the time instant of falling edge from divider signal numerical solving is required.

After deriving all the parameters, ED-algorithm presented in [22] is used to simulate the transient behavior of the CP-PLL. In the next section simulation result are discussed.

4. Simulation results

As already mentioned the Event Drive Method of modeling and simulations is more suitable to analyze the mixed-signal nature of the CP-PLL. By applying ED algorithm, the transient response of CSCP-PLL is simulated as shown in Fig.7, by setting the VCO frequency near to zero, it can be seen that, the voltage step are overloading the VCO. Since the size of voltage step is larger, so frequency excersions are overloading the VCO. Furthermore, it can bee seen that, the voltage jump are symmetrical and equal in magnitude for up and down cycles. This is a serious issue concerned with CSCP-PLL However, on the otherhand it can be seen that, due to asymmetrical pump current, a larger voltage jump in the up cycles is observed in transient response of VSCP-PLL. This is due to the fact that, when PLL is locking to a frequency near to zero. The difference between the supply of VSCP and LF capacitor is very high (see (2)), so the current flowing in the up cycle is larger than the current in the down cycle. Therefore, voltage steps in the down cycles are are vanished, Hence, no overloading effect occurs when using a VSCP-PLL. This is an advantage of using the VSCP instead of CSCP.

5. Conclusion

In this paper, it has been shown that, the Event Driven method is very efficient in analyzing the non-linear switching behavior of the mixed-signal PLLs. Furthermore, it has been shown that, overload occurs using the CSCP-PLL, since the voltage steps are driving the VCO to produce meaningless signal. To prevent this situation, it is necessary that PLL may locked far away from overload conditions described in [8]. On the other hand, no overloading effect is observed in VSCP-PLL due to the fact that the current gain of the system is varying around it locking point. By applying the Event Driven Method, it is more easier to predict the non-linear characteristics of the mixed-signal PLLs.

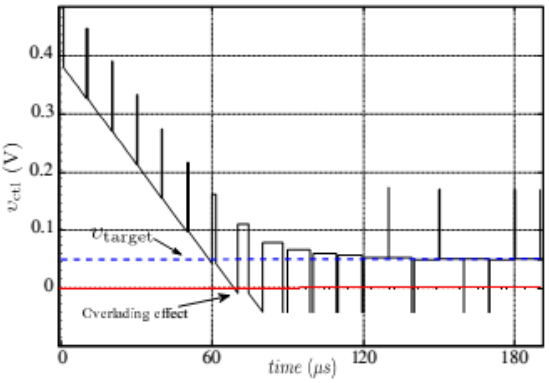

Fig.7: Overloading phenomenon in CSCP-PLLs

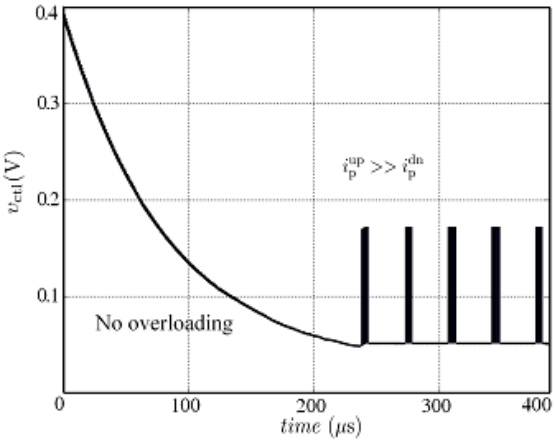

Fig.8: Asymmetrical behavior of VSCP-PLL protects overloading phenomenon.

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