Reusing Vehicular Control Networks as Test Access Mechanism for Automotive Semiconductor Chips

Muhammad Adil Ansari[1], Mohsin Shaikh[1], Ahmed Ali[1], Saleem Ahmed[2] & Muhammad Tarique Bhatti[1]
[1]*Quaid-e-Awam University College of Engineering, Science and Technology*
[2]*Dawood University of Engineering & Technology*

Abstract
Today, air and road vehicles accommodate several electronic control units (ECUs) to ensure safety, reliability and comfort. Such ECUs are connected through vehicular control networks (VCNs). Typically, integrated circuits are tested for structural defects, which could occur during fabrication. However, the adverse environment in vehicles may develop defects within a chip, which may lead to catastrophe. The work in hand presents test access mechanism for in-vehicle ICs through VCNs and the on-chip test circuitry; moreover, the proposed test access mechanism complies with the VCNs' protocols. In this paper, two well-known VCNs are considered, i.e., controller area network (CAN) and FlexRay.

Keywords:
Controller area network, FlexRay, test access mechanism, scan test design, vehicular control networks.

1. Introduction

Vehicles' occupants and environmental governing authorities are demanding for reliability, safety, comfort and reduced fuel consumption. Such demand has increased the accumulation of electronic systems in a vehicle; thus, the communication complexity among the in-vehicle electronic control units (ECUs) is increased. These ECUs are connected through vehicle control networks (VCN). An ECU can be comprised of host processor, communication controller (CC), differential bus transceiver, memory blocks, standard interfaces and different IP blocks. The host processor is coupled with different sensors and actuators. Among several VCNs, controller area network (CAN) [1] and FlexRay [2] are widely adopted networks in recent vehicles.

Besides, the technological scaling of semiconductor devices into deep submicron is decreasing the tolerance margin of the process variations and posing serious threat on the reliability of integrated circuits [3]. For critical real-time applications, the reliability of its component is extremely important to be ensured [4]. Therefore, the maintenance of automotive electronic system is also important as the mechanical maintenance of a vehicle in order to ensure safety, reliability and comfort. An early detection of the degradation of the system components helps to take appropriate action before it manifests as a failure, which may result in a catastrophe.

Traditional system-level test approaches for automotive chips have focused on functional test to detect defects or the reasons of irregular operations [5] [6]. Such functional tests usually require huge amount of test data and test time as compared with the structural test, to guarantee test quality [7], [8], [9]. A number of reliable test and diagnosis techniques such as scan test, scan-based logic built-in self-test (BIST), memory BIST, analog BIST, are commercially available during manufacturing [10], [11]. However, the test interfaces to those design-for-testability (DFT) circuitry are sometimes disconnected due to either limited number of connecting pads or security concerns.

The VCNs support network level functional testing of each network node; however, they do not explicitly support the structural testing of on-node semiconductor chips. For instance, ISO 26262 [12] standardizes the functional safety of electrical and/or electronic system in vehicle, however, the structural test of vehicular chips is not included.

The access to the on-chip test infrastructure is important to test the chip when it is a part of a system. However, generally, the access to the DFT circuitry is disconnected after post fabrication test because of the limited number of I/O pins or security concerns. Therefore, it is difficult to have access to the structural defects while the ICs are embedded into a system.

On-board diagnostic (OBD) systems are widely used for automotive applications and they have progressively improved in capability and standardization. OBD systems allow its users the access to the status of various parameters of vehicle sub-systems via the installed sensors. They continually monitor the status of various parameters and inform the driver via lights on the dashboard. Then, by using commercially available tools, the technician can retrieve the desired diagnostic information during service and repair of the vehicle. The applications of OBD systems have been extended from engine-level to the chassis, body

Dr. Muhammad Adil Ansari (maa1784@gmail.com) is the corresponding author and he is an Assistant Professor in the department of Electronic Engineering, Quaid-e-Awam University College of Engineering, Science & Technology, Pakistan.

Manuscript received December 5, 2017
Manuscript revised December 20, 2017

and accessory devices. Since today's automobile is no more a mechanical system, OBD systems may not be sufficient to maintain the reliability of automobiles. Thus, the diagnosis has to be extended to the semiconductor chip-level.

Diagnosis for the semiconductor chips figures out not only the physical weak points, which causes early-life failure, but also aging-induced defects of the semiconductor chips, which incurs severe system failure during lifecycle. Since the chip-level diagnosis uses the legacy infrastructure for structural testing, it has to be accessible during the diagnosis.

Such access is enabled through this work. This paper presents test access mechanism for offline low abstraction level maintenance of vehicular semiconductor chips through CAN and FlexRay networks, while complying with the corresponding network protocols. Such mechanism ensures safety, reliability and comfort for vehicle occupants. Moreover, it can also be utilized for medical equipment, industrial automation, etc.

The remaining paper is organized as follows. The succeeding section discusses semiconductor test techniques. Section 'Introduction' presents the fundamentals of the two VCNs. The proposed test access mechanism is presented in Section 'Test Access Through VCNs'. This paper is concluded in Section 'Conclusion'.

2. Semiconductor Testing

After fabrication of electronic systems, two types of tests are performed: functional test and structural test. The functional test of a circuit tests for meeting the functional specifications, assuming it is fabricated correctly. However, the structural test examines the faults produced during fabrication of a circuit or due to its aging. Through structural test, the availability, functionality and connectivity of each gate is tested. For structural testing, scan test technique [13] is the most widely used design for testability (DFT) technique [14].

To enable structural testing, controllability and/or observability are achieved for each possible node of the circuit. In scan testing, storage elements (latch, flip-flop) are replaced with scan cells, refer Figure 1(a), to achieve controllability and observability. The scan cells constitute a shift register during test mode and storage element during functional mode, refer Figure 1(b). During test mode, the test equipment applies the test stimuli data, which is serially shifted in through scan chain and applied to the corresponding combinational circuitry. The response against the applied test stimulus is captured in parallel by the scan cells and it is serially shifted out of the circuit through scan chain. The captured response is then compared with the expected response, which is stored at the test equipment. If both responses are same, the device is defect free, otherwise defective. The test controller is responsible of transporting the test data through test circuitry.

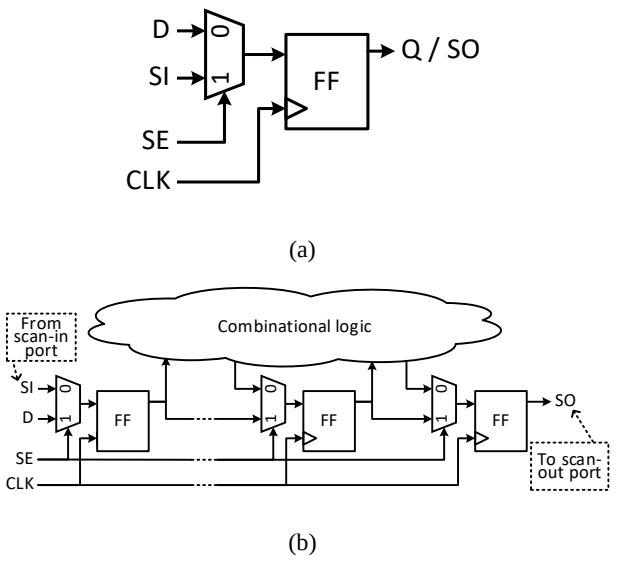


Figure 1 Scan design (a) scan cell and (b) scan chain with a combinational logic cloud [14].

3. Vehicular Control Networks

3.1 Controller Area Network

Controller area network is a robust asynchronous serial communication bus, which has effective features such as assurance to conflict free message delivery, high immunity to electromagnetic field interference and ability to self-diagnose and repair the data error [1]. CAN was initially developed for automotive industry to replace the complex communication among several in-vehicle ECUs. However, due to its effective features it is adopted by robotics, automotive industry and medical equipment.

CAN bus uses event-triggered protocol in which a node broadcasts messages over the network and the target node receives the message based on the message ID. The CAN controller of all network nodes perform acceptance test on the identifier fields of the incoming messages. If the message identifier passes the acceptance test at a node, the message is stored in the receive register, otherwise discarded.

There are four types of CAN frames: data frames, remote frames, error frames and overload frames [1]. Data frames transport information between source node and destination node. There are two data frame formats based of the identifier field; standard frames and extended frames. In standard CAN frame, there is an 11-bit identifier, whereas

in extended CAN frame there is a 29-bit identifier field those provide 2^{11} and 2^{29} unique identifiers for a network, respectively.

CAN is a message oriented protocol, in which the data messages are transmitted on the network without any explicit node address. Specific kind of message is tagged with a unique identifier before it is broadcasted on the network. The contents of a message can be any specific parameter value such as engine temperature, RPM, throttle etc. Each message has a unique identifier through the network, which is also used for arbitration and prioritization. The lower valued identifier has the higher priority.

CAN protocol resolves the bus access collisions among multiple messages through a non-destructive bit wise arbitration, based on a preprogrammed priority of each message in the identifier field of a message The CAN transceiver receives the bus value even if it transmits, in order to sense the logic level of bus. The CAN bus is implemented with wired-AND logic that means if a node transmits logic 1 on the CAN bus and another node transmits logic 0 then the received bit will be logic 0. For example, if a node transmits logic 1 (the MSB of the message identifier) and senses logic 0 then it means that another node attempts to transmit a frame with relatively higher priority. Consequently, the loosing node switches into receive mode and try attempting frame transmission later.

3.2 FlexRay

FlexRay follows time-triggered protocol, i.e., TDMA (Time Division Multiple Access). A node communicates during allocated time slot in a communication cycle. Figure 2 shows the frame structure of FlexRay communication protocol. The FlexRay communication is carried figure out in 64 recursive communication cycles and each communication cycle is composed of (1) static segment (TDMA-based), (2) dynamic segment (FTDMA-based), (3) symbol window and (4) NIT (Network Idle Time). Each static slot is assigned to exactly one node or no node but multiple slots can be assigned to a single node. The dynamic segment is an optional communication period and its slots' length is dynamic, which is composed of minislots. The dynamic slots may dynamically be assigned to the nodes. The symbol window is an optional communication period, which is used to transmit the symbols i.e., wakeup symbol, collision avoidance symbol and media access test symbol. The network idle time is used for clock synchronization among FlexRay nodes.

In FlexRay protocol, the time is represented as microticks, macroticks and cycles, refer Figure 2. The microtick is a basic time unit of a communication node, which is derived from the oscillator of the node and it may vary among nodes. However, the macrotick is a basic unit of global time, which

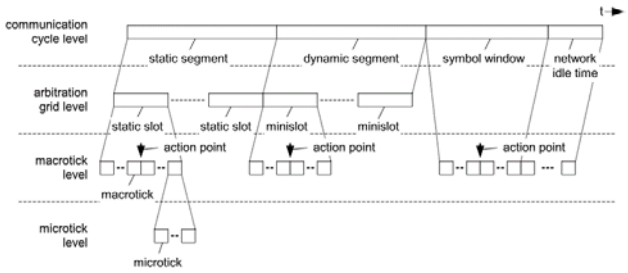
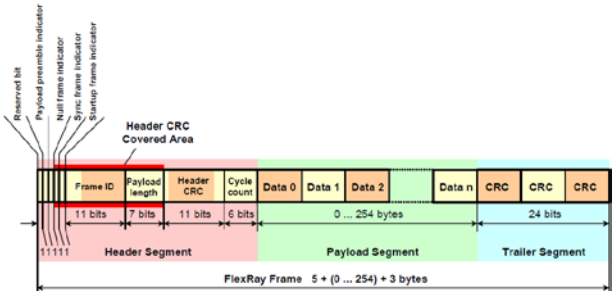


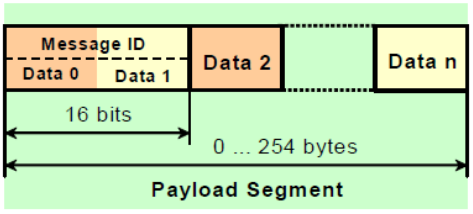
Figure 2 Timing hierarchy within the communication cycle [2]

is composed of integer number of microticks. A communication cycle or a cycle in FlexRay protocol is composed of integer number of macroticks.

The FlexRay frame consists of three segments: the header segment, the payload segment and the trailer segment, as shown in Figure 3. The details of frame structure can be referred from [2]. The null frame indicator (NFI) bit in the header segment indicates whether or not the frame is a null frame (contains no useful data). If NFI-bit is 'HIGH', the payload of the frame contains some data, otherwise the all payload bytes are zero.



(a)



(b)

Figure 3 (a) FlexRay frame format (b) payload segment of frames transmitted in the dynamic segment

4. Test Access Through VCNs

Figure 4 illustrates the basic concept of the proposed test access mechanism. The test equipment is connected to the VCN, which connects certain nodes or ECUs. In order to test semiconductor chips embedded on an ECU, we propose to switch the target ECU into test mode from functional mode. Subsequently, the test equipment sends test stimuli data to the targeted node and receives test response data from the same node. The exchange of test data between the

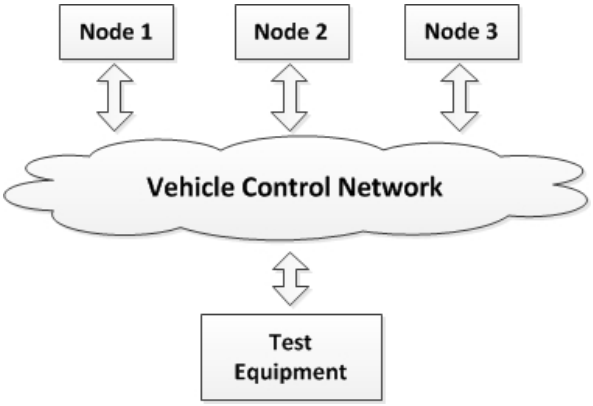


Figure 4 Concept of the proposed test access mechanism

targeted node and the test equipment is performed through the corresponding VCN while complying with the corresponding network protocol.

The process of switching a node between test and functional modes is dependent on the protocol of VCN. Thus, the test access through CAN and FlexRay are discussed in the following subsections.

4.1 Through FlexRay Network

This subsection presents the proposed test access method through FlexRay protocol. Here, NFI bit is used to differentiate test data frame from functional data frame. The test data is transmitted with NFI bit set to 'LOW' at the transmitter side. In other words, if a frame is received by a node having NFI bit '0' and non-zero data in its payload segments, it will be taken as a test data frame. The format of the test data frame is shown in Figure 5. The first byte in the payload segment of a test data frame indicates the address of the targeted chip on the targeted node and the remaining bytes contain the test data.

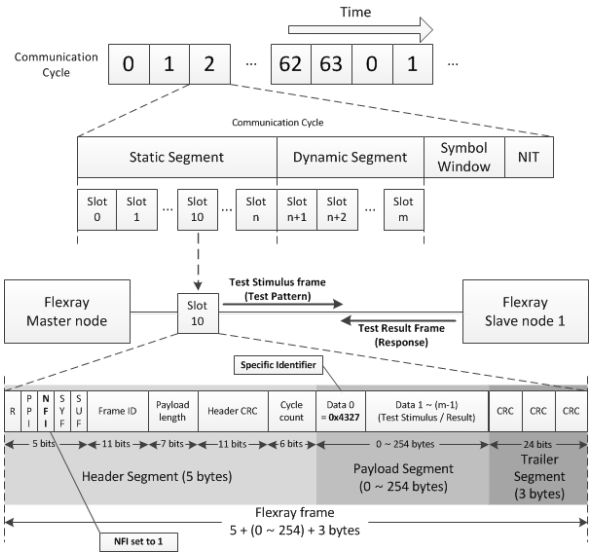


Figure 5 FlexRay frame's structure for carrying test data.

In order to test a chip on a node, the test equipment transmits test data frames to the targeted node during the corresponding time slot. At the node end, the test controller routes the test data to the targeted IC.

The test response from a chip is transmitted by the corresponding node during allocated time slot to the test equipment via the response frames, which are regular data frames. The response data is then compared with the expected response by the test equipment.

The test data frame is illustrated in Figure 5. The NFI-bit is (1) 'LOW' with test stimuli data in the payload segment and (2) 'HIGH' with test response data in the payload segment.

4.2 Through CAN Network

In this subsection, CAN- based test access mechanism is presented. In order to switch a CAN node into test mode, test dedicated IDs are used for each IC. Once a node receives a message with test dedicated ID, which corresponds to a particular IC, it switches into test mode. The number of message IDs for a CAN network is quite large, i.e., 2^{11} or 2^{29} and generally, up to 100 nodes are connected through a CAN network in vehicle [15]. Thus, there are many unused message IDs that can be used to identify test data frames. For n ICs, we need 2n message IDs for test data transportation through CAN network, i.e., n IDs for test stimuli messages for n ICs and n IDs for test response messages.

During test mode, the on-node test controller performs test operation on the targeted IC. Similarly, the test response, collected by the test controller, is transmitted to the test equipment, which compares the observed response with the expected response.

Figure 6 illustrates an example CAN network with five nodes including the test equipment. The black line shows the network connections. First, the test equipment broadcasts a CAN frame with message ID_{21} (indicated as red lines), which carries test stimuli data for a chip of node 4. Therefore, only node 4 receives this message and the corresponding test controller performs the test operation on the targeted IC. The test response against the applied stimulus is then broadcasted by node 4 for the test equipment with the message ID_{42}, as indicated through blue line. Thus, only test equipment accepts the response message.

In this way, the test data is shared between the test equipment and the node of targeted IC.

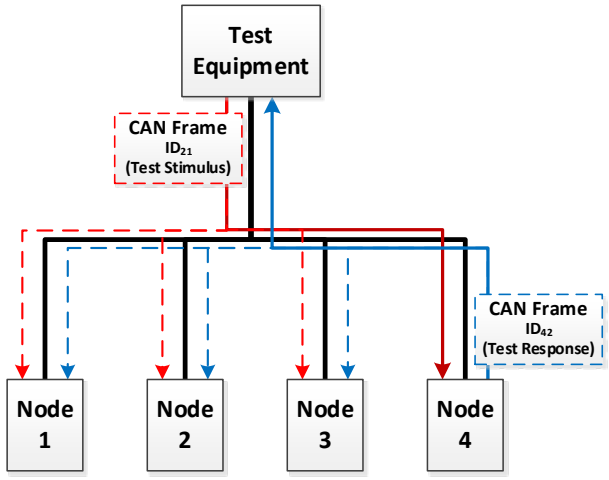


Figure 6 Example illustration of the test data sharing between test equipment and Node 4 through CAN network.

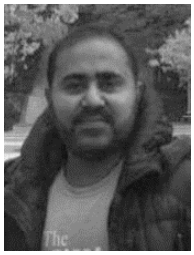
5. Conclusion

In this paper, the test data transportation between an in-vehicle integrated circuit (IC) and the test equipment is enabled through two vehicular control networks (VCNs); controller area network (CAN) and FlexRay. Such feature helps performing regular maintenance activity on each chip of the nodes connected to a VCN to improve the reliability. The transportation is performed while complying with the two network protocols; thus, no overhead will be experienced during functional operations.

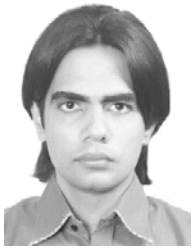
References

[1] R. B. Gmbh, "CAN Specification," 1991.
[2] F. Consortium, "FlexRay Communications System: Protocol Specification Version 2.1," 2005.
[3] J. Jung, M. A. Ansari, D. Kim, H. Yi, and S. Park, "On Diagnosing the Aging Level of Automotive Semiconductor Devices," IEEE Trans. Circuits Syst. II Express Briefs, vol. 64, no. 7, pp. 822–826, 2017.
[4] S. Seo, J. Kim, and S. M. Kim, "A Design of Fail-safe Gateway-embedded System for In-vehicle Networks," Int. J. Appl. Eng. Res., vol. 12, no. 6, pp. 921–927, 2017.
[5] K. Choi, J. Luo, K. R. Pattipati, S. M. Namburu, L. Qiao, and S. Chigusa, "Data Reduction Techniques for Intelligent Fault Diagnosis in Automotive Systems," in Proc. IEEE Autotestcon, 2006, pp. 66–72.
[6] Y. Zhang, G. W. Gantt, M. J. Rychlinski, R. M. Edwards, J. J. Correia, and C. E. Wolf, "Connected Vehicle Diagnostics and Prognostics, Concept, and Initial Practice," IEEE Trans. Reliab., vol. 58, no. 2, pp. 286–294, 2009.
[7] J. Zeng, M. Abadir, G. Vandling, L. Wang, S. Kolhatkar, and J. Abraham, "On Correlating Structural Tests with Functional Tests for Speed Binning of High Performance Design," in Proc. International Test Conference, 2004, pp. 31–37.
[8] A. Krstic, J.-J. Liou, K.-T. Cheng, and L.-C. Wang, "On Structural vs. Functional Testing for Delay Faults," in Proc. Fourth International Symposium on Quality Electronic Design, 2003, pp. 438–441.
[9] P. Maxwell, I. Hartanto, and L. Bentz, "Comparing Functional and Structural Tests," in Proc. International Test Conference, 2000, pp. 400–407.
[10] "DesignWare STAR Hierarchical System," Synopsys. [Online]. Available: https://www.synopsys.com/dw/doc.php/ds/es/STAR-Hierarchical-System_DS.pdf.
[11] "Need a Silicon Test Solution with Built-In Flexibility?," Mentor Graphics. [Online]. Available: http://s3.mentor.com/public_documents/datasheet/products/silicon-yield/products/tessent.pdf.
[12] G. Leen and D. Heffernan, "TTCAN : A New Time-Triggered Controller Area Nnetwork," Microprocess. Microsyst., vol. 26, pp. 77–94, 2002.
[13] B. Geuskens and K. Rose, "Implementing a CMOS Boundary-Scan Architecture Tutorial," in Proc. Seventh Annual IEEE International ASIC Conference and Exhibit, 1994, pp. 392–399.
[14] L.-T. Wang, C.-W. Wu, and X. Wen, VLSI Test Principles and Architectures: Design for Testability. 2006.
[15] T. Herpel and R. German, "A Simulation Approach for the Design of Safety-Relevant Automotive Multi-ECU Systems," Proc. IEEE Int. Conf. Syst. Syst. Eng., pp. 25–32, 2009.

Dr. Muhammad Adil Ansari received BE degree in Electronic Engineering from Mehran UET, Pakistan, in 2006. He received PhD and MS degrees in Computer Science & Engineering from Hanyang University, South Korea, in 2016 and 2010, respectively. He worked as operations engineer with Pakistan Telecom. Company Ltd., from 2006 to 2008 and he served as a lecturer in COMSATS Institute, Pakistan from 2010 to 2011. He is an assistant professor in Quaid-e-Awam University, Pakistan, since 2011. His research interests include design-for-testability of digital stacked and non-stacked integrated circuits.

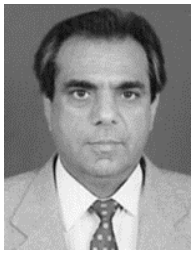


Dr. Mohsin Shiakh received BE degree in Software Engineering from Mehran University of Engineering and Technology, Pakistan, in 2006, MS degree from Hanyang University, South Korea, in 2010, and PhD degree from Chung-Ang University, South Korea, in 2017. He has served as software engineer and faculty member in different organizations. He is a faculty member of Quaid-e-Awam University, Pakistan, since 2012. His research interest includes software engineering, software quality assurance, re-engineering legacy application and software analysis.



Dr. Ahmed Ali received BE degree in Electronic Engineering from Mehran University of Engineering and Technology, Pakistan, in 2010 and PhD degree in Nano Engineering from Hanyang University, South Korea, in 2017. He is a faculty member of Quaid-e-Awam University, Pakistan, since 2012. His research area includes photonics based smart nano sensors development, electric field responsive nanostructures design, graphene based stimuli responsive platforms.

Dr. Saleem Ahmed received BE degree in Computer System Engineering from Quaid-e-Awam University, Pakistan, in 2005 and PhD degree in Electronic Engineering from Chonbuk National University, South Korea, in 2015. He is an assistant professor at Computer System Engineering Department, Dawood University of Engineering and Technology, Pakistan. He has wide experience of industry, teaching and research. His research focuses on Iterative Detection & Decoding, MIMO systems, Massive MIMO and Hardware prototyping of wireless systems.



Dr. Muhammad Tarique Bhatti received BE degree in Mechanical Engineering from Mehran UET, Pakistan. He received PhD degree from Dublin City University, Ireland, in 1991. He is an assistant professor in the department of mechanical engineering since 2012. His research is focused to computer controlled robotics and vehicular control.