

# Offline Earliest Deadline first Scheduling based Technique for Optimization of Energy using STORM in Homogeneous Multi-core Systems

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## Abstract

The energy and power of the multicore system is controlled and measured by the hardware management system. Power densities are proportionally increasing due to increase in temperature of the multi-processor system on chip MPSoC. Due to shrinking of the chip size and increased number of transistor on chip high peak temperature directly affect the speed and life span of the multicore system. Migration of task that produces high thermal value to such cores that has less temperature is a common technique to avoid high thermal values in multi core system. The proposed offline Scheduling Algorithm technique migrate task load to the core that has less thermal values in response to a threshold temperature this technique also considers other thermal problems which affects the power, reliability and performance of multi-core system. For evaluating and attaining the Stability of the proposed research for migration of tasks can be verified by comparing it with the different task migration techniques that are familiarized previously. The proposed technique also considers both hot and cold tasks to forecast the accurate thermal values by considering the previous thermal history of the tasks. The scheduling mechanism only considering such cores that are in highest energy state due to execution of some task such as running state while those cores that are in sleep or deep sleep mode can be consider in a lowest energy state. The simulation results shows that the proposed technique reduces almost 6°C temperatures at 13% utilization and the energy utilization is 230.43 J which is 5.12 % improved as compare to the global EDF used previously. The proposed scheduling technique can control and measure the thermal effects and energy consumption on chip and utilize the processor in an efficient way when least number of tasks is in running state but has the ability to schedule multiple task to make a slower and energy efficient processor.

## Index Terms:

*Dynamic Voltage and Frequency Scaling, Dynamic Power Management, Dynamic Thermal Management, Dynamic Voltage Scaling, Energy Optimization*

## 1. Introduction

The development in the processing unit is capable to run heavy tasks but it can have some issues e.g. Dimension,

cost, power utilization, performance, reliability and processing speed are the major issues with the advancement in processor. The lack of concentration can affect the overall system performance. The temperature on the chip increases for which various mechanisms are used to reduce the thermal effects due to high heat and increase the performance of the system because high heat causes the chip to be damage [1]. A. Biondi and G. Buttazzo et al. (2018) proposed a thermal-aware online scheduling based technique is used for high-performance homogeneous systems using a thermal model that considers both spatial and temporal gradients and their correlation with temperature evolution. Increase the performance of the homogeneous system dynamic voltage and frequency scaling is used for the smooth execution of task [2]. S. Asyaban and M. Kargahi,. (2018) Introduces a technique that improve the performance and reliability of a multi-core processor by checking the impact of power consumption of multi-core processor and dynamically check the frequency and voltage. This approach is also used to predict the thermal variation on each core. The proposed method gives 54.3% improvement in results and 61% improvement in energy delay as compared to the conventional multi-processor [3]. D. Konar, K. Sharma, V. Sarogi et al. (2018) proposed a GPU dynamic voltage and frequency scaling that is very efficient for saving energy for various applications and also used evaluate the impact of GPU DVFS on application power consumption when an application is in running state and also consider the impact of application perform ace and energy conversation as compared to DVFS that is widely used in embedded devices like cell phones and various multipurpose electronic gadgets to improve performance because GPU-DVFS consider both the architecture and application of GPU [4]. A. Yadlapati and K. Hari et al. (2018) proposed a scheduling based best speed fit EDF technique that chooses the suitable processor when the task is allocated for execution and the proposed technique doesn't consider

the fastest core. The performance and reliability of the chip is more improved than that of the global earliest deadline first algorithm that considers the priority of the task while executing. Migration of task can occur at any time with different speed processors, and task were assign on the basis of deadlines those tasks that can have an early deadline can have higher priority [5]. S. Chakraborty and H. K. Kapoor et al. (2017) proposed a technique that turns off and on some on-chip last level cache (LLC) is used to reduce the heat that produces high leakage power. This technique is used to increase the performance and reliability of the system. The effect due to high temperature on chip causes various thermal issues due to high heat on chip the cooling cost also increases. When the temperature of the chip reduces to 4°C a simultaneous 52% maximum savings in cache leakage occurs [6]. T. Afroze describes a dynamic thermal management technique that is one of the most reliable techniques to reduce and stabilize temperature of the multi-core system. DTM technique gives high performance as well as efficient reliability of the system. In a multi-core system exponentially decrease in the temperature also reduces the power utilization. DTM technique is a way to efficient to manage thermal responses of a processing systems. There are many techniques that are combined to manage temperature and thermal responses including "Dynamic Voltage and Frequency Scaling (DVFS)", "Dynamic Power Management (DPM)" and "Dynamic Voltage Scaling (DVS)". These techniques are very useful but they cause some reliability and performance issues as well as they are mostly used to resolve on chip temperature and power problem. Dynamic voltage scaling is used to control the gradual increase in on chip power consumption by decreasing the power. Dynamic voltage scaling also reduces the temperature of the system which improves the performance and reliability of the system. Reducing errors by maintaining the systems voltage at run time can manage the gradual increase in on chip power consumption. Dynamic voltage scaling is commonly applied in the active state high power state while dynamic power management technique is functional to operate a multi core processor when the power is in lower state. When the chip is in idle mode by following the appropriate migration policies the overall performance and reliability of the system increases. If the policies are aggressive the temperature on chip is increasing and these policies causes high temperature cycle that reduces the overall system reliability [7]. Khalid Bati et al. (2013) proposed a dynamic thermal management technique for reducing the power of consumption of each core. This thermal aware mechanism for scheduling of various task by considering their ambient temperature for allocation of task to a scheduler and various frequency and voltage levels on the basis of utilization factor of a task. In this thermal aware scheduling technique the simulation was done on EDF

scheduling algorithm [8]. H. Sun, P. Stolf, proposed a thermal control technique that reduces thermal errors around 1.63°C and consider hotspot by accurately measuring the temperature of the core using a sensor placement mechanism and select the most appropriate point for sensor placement [9]. As high temperature affects the reliability of the processor and causes various thermal issues. Dynamic thermal management is a techniques used to control and mange the thermal problem. For monitoring of temperature DTM technique is further classified as sensor placement technique on a processor and estimation of peak temperature on cores techniques this technique is measure the temperature efficiently because of offline phase. This is a thermal aware technique and reduces almost 4.5°C. Temperature in comparison to thermal unaware technique DTM is also used to avoid a thermal problem in cooling liquid technique and temperature aware task scheduling technique as well that is used in embedded devices [10].

## 2. Literature Review

T. Simunic, K. Mihic proposed that the power usage in the chip can be efficiently managed by using "Power management" technique that reduces the power consumption because all the cores that are not in working condition can be turned off due to which the performance of the system increases by decreasing the overall chip temperature the power consumption is also decreased. Due to replication of a single core configuration when the transition becomes among the two states when the power is high and from that state to a state when power is low these transitions can disturb the processor performance [12]. Inchoun Yeo describes (DTM) technique that is one of the most reliable way to reduce and stabilize system's temperature and also helpful for the high performance as well as efficient reliability of the system. Due to exponentially decreased temperature the power utilization also reduces. DTM technique is a way to efficient to manage thermal responses of a processing systems now a days there are many techniques that are combined to manage temperature and thermal responses including "Dynamic Voltage and Frequency Scaling (DVFS)", "Dynamic Power Management (DPM)", "Dynamic Voltage Scaling (DVS)". These technique are very useful but they causes some reliability and performance issues. They are mostly used to resolve on chip temperature and power problem. Dynamic Voltage Scaling is used to control the gradual increase in on chip power consumption by decreasing the power. DVS also reduces the temperature of the system which improves the performance and reliability of the system by reducing errors by maintaining the systems voltage at run time it can manage the gradual increase in on chip power

consumption. Dynamic voltage scaling is commonly applied in the active state while (DPM) technique is functional to operate a multi core processor when the power is in lower state. When the chip is in Ideal mode by following an appropriate procedure by following the appropriate policies the overall performance and system's reliability increases as high temperature cycle can affect and decrease the overall system's reliability if the policies that are followed are aggressive [13]. Joohno Kong, Sung Woo introduces power management that can have a very important impact in decreasing the temperature on chip because lower power consumption can affects the power densities there are many problems that occurs due to increase in temperature and power density e.g. electro migration is process that gets disturbed due to increase in temperature significantly electro-migration is affected by increased temperature while by reducing the temperature dielectric breakdown process can be smoothly in working. On other hand for unmanaged thermal control thermal stabilization plays an important role to manage power [14]. Mehdi Kamal, discuss that that size of the chip is reduces certainly increasing the electronic element transistor on a chip. So the frequency and power densities are gradually increases that cause power consumption a most important issue.now a day's multicore systems are very efficient but due to increase in temperature it can have power and thermal issues. Temperature gradients can be affected and imbalanced due to high peak temperature,the cooling cost can be increased due to high temperature the affect the system's performance and reliability so the power management technique and thermal management techniques can be used to have more reliable and high performance system on chip. Fan thermal packaging can be used for the thermal and power management but this is not a cost effective method while temperature aware energy efficient scheduling techniques is more efficient then fan thermal packaging because it is more reliable and lower in cost. A propose techniques is as follow dynamic thermal management techniques" DTM is both software and hardware low cost technique that can have decrease power utilization more reliable and it can have less impact on the system's performance. The most recent techniques like DTM, DVFS, DPM and integrated DVS doesn't account thermal cycle effects and also temperature gradients this is going to increases the systems reliability and performance while fetch toggling technique is a hardware technique which can increase the chip temperature because these hardware techniques such a clock gating do not consider appropriate information [16]. There are many dissimilar applications that perform differently and they have different temperature on chip machinery depending on their processing requirements. There are some application needs more intense CPU processing that creates more heat on chip and temperature on chip is increased as compared to those applications that

doesn't need intense processing so the differentiation in temperature among the different chip components can be approximately 10°C.while there is a considerable difference in thermal characteristics of Individual core's in running mode in the chip can have different thermal characteristics for every individual core's because of the core's peak temperature [16]. Pratyush Kumar,Lothar Thiele introduces a power management techniques that can decrease the power consumption by turning off all the cores that are in idle state. A power management technique doesn't consider spatial gradients. Power management techniques can also reduces average power utilization and on chip temperature by keeping the idle cores turn off. Power management techniques can also enhance the performance and reliability and reduces gradually the hotspots that appear on the chip when the power consumption increase due to high power consumption the peak temperature on chip constantly increases. This technique doesn't consider Thermal cycles and temporal gradients which unfortunately affects the entire system reliability [17 18 19]. Embedded systems are those intelligent devices that are used due to the integration of software and hardware while software is working as a main graphical user interface that performs the smart system to perform specific jobs. Now a day's mostly embedded systems are operated on DC batteries. The design of embedded devices are facing few issues because the chip size is reduces so the chip can have certain challenges e.g. power consumption, reliability of the system, size and dimension of the embedded device, cost and performance. Processing unit needs to attain high performance by consuming less power is one of the most important design challenges in embedded systems. Moore's law states, 'in every eighteen months the electronic component transistors becomes double on chip and constantly increasing with time [20]. C. J. Lasance, describe that in a multi-core systems, a little difference in the temperature of the operating system from reduces almost 50% life span of embedded equipment because the difference in temperature can cool down the overall temperature on each core [21 22]. There are few deficiencies in previous studies like the effect of ambient temperature which leads temperature underestimation. Chips were designed without considering the ambient temperature. A study shows 1°C increase in ambient temperature causes to increase the CPU and GPU temperature roughly 1.05°C and 1.08°C respectively an accurate prediction model to predict the temperature of destination core [23].

### 3. Problem Statement

The main objective and focus of this research work is chip (reliability) that is the most important issues in multi core

embedded technologies. High temperature causes multiple performances and reliability issues. Task migration is the way to avoid high temperature and improve performance. However accurate prediction about the coolest core and the task which needs to migrate to control the chip temperature is the major design issue in task migration techniques. Our technique considers all types of tasks including hot and cold task to accurately predict the temperature of the core in running mode and also use precisely thermal history to precisely check the chip temperature for the selection of cold core. A task migration technique based on previous history by considering workload of running core to predict the future temperature and coolest cores. This technique improves the reliability by avoiding thermal issues.

#### 4. Experimental Technique

The major components include a task producer where user can create random task sets in XML file that contains different parameters. This XML input file is used as an input for the simulation tool. The simulation tool for real-time multiprocessor scheduling can simulate the input file according to the scheduling policy and developed the power profiles according to the set of parameters given in XML file. These Power profiles generated from STORM can be saved in a text output file. The XML file contains all the information of task sets. A temperature model can also analyze the thermal responses of different scheduling algorithms. A statistical testing mechanism is used to test many data sets. These data sets are already stored produce thermal profile when used with some hardware constraint in thermal model ATMI and a power model is used for each core comprises of static and dynamic power.

$$\text{Total power} = \text{dynamic power} + \text{static power} \quad (1)$$

$$\text{Dynamic power} = C \times F \times V \quad (2)$$

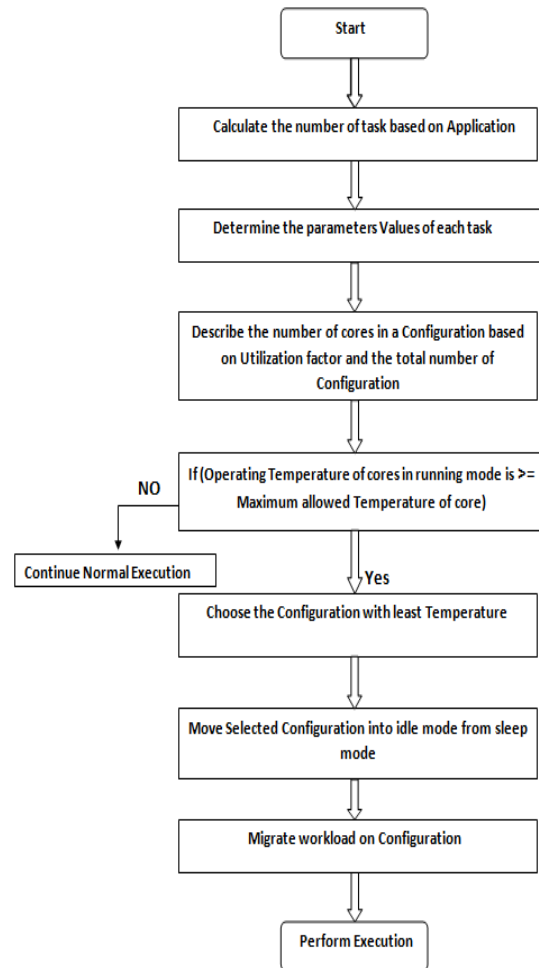
Therefore  $C$  is the switching capacitance.  $F$  is the frequency and  $V$  is the supply voltage

$$\text{Static power} = \text{Leakage current} \times V \quad (3)$$

##### A. Flow chart

We have proposed technique for quad core multiprocessing. In the processor in which the scheduler will first check the number of task jobs that are running in an application. Primarily the value of counter is zero for all 8-cores in a multiprocessing processor. The scheduler is able to determine the constraint and values of every individual task. So the counter for all the cores is initially zero. The configuration of core will be selected on the basis of least temperature and lower Power of

consumption among all other configurations once the core with least temperature is selected its counter in running mode is rapidly rising. In such case when the temperature of the core in running mode is less than the maximum allowable temperature then the scheduler will perform normal process of task execution. While in a situation when the core temperature in running mode is more than the thermal threshold value a temperature that is set maximum for the core in such situation select the configuration with least temperature and shift the selected configuration from idle mode to sleep mode and migrate all the tasks. The core is first shifted to idle mode from sleep mode to avoid delays and thermal threshold temperature value which is already set to reduce delays and migration cost. Once the workload will be migrated to the core that has least temperature the scheduler will start performing execution of job. In the proposed scheduler experiments are performed and set the ambient temperature at 26°C. The temperature of the core when it is in sleep mode is the current environmental temperature. When the value of current temperature is high then a configuration with least temperature is used and all the other cores are remain in sleep mode.



## B. XML File

A XML input sample file is shown below. The simulation duration for this XML input file is 1000 that guides the simulation tool for a functional execution in milli seconds. A 'SCHED' scheduler is define, name and id's are assign to all 4-core that contains individual tasks and relevant parameter information given by the user in <TASKS> entity. The activation time, period, priority, Worst case execution and deadline of the entire task are given in XML file.

```
WCET="1" priority="1"></TASK><TASK
```

TABLE 1: Configurations of cores

Frequency Mhz	Utilization Factor %	No of cores in running state	No of cores in sleep mode
100	0-9	1	3
100	9-18	2	2
100	18-24	3	1
100	24-34	4	0

## 5. Experimental Results

In this section we discuss our experimental results that illustrates the temperature variation between the curves of proposed EDF and Global EDF'. Proposed EDF considers reliability and performance parameter so only those cores are in running state that is in working condition. In the beginning exponentially temperature on chip rises and then arrive at a steady state level. At 13% utilization factor the global EDF has 5°C more temperature on chip as compare to our proposed approach. Proposed EDF based on core configurations and using quad-core processor. At Low workload for 13%UF only 2-processors are in running mode while remaining 2-processors are in sleep mode. Our technique consumes less power than that of Global EDF and reduces almost 5°C temperature on chip. X-axis depicts the time in milliseconds multiplied by  $10^4$  while y-axis represents the temperature in °C.

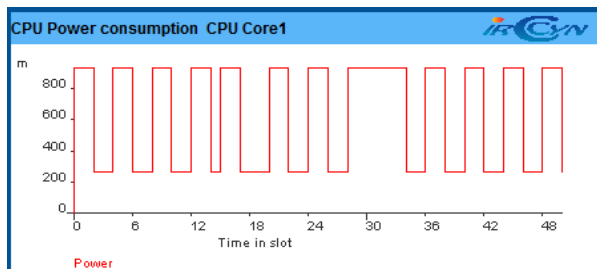


Fig. 1 CPU Core 1 load at 13% UF

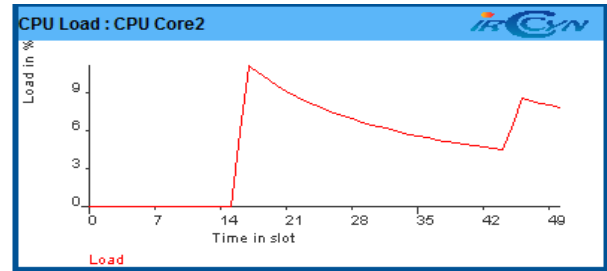


Fig. 2 CPU Core 2 load at 13% UF

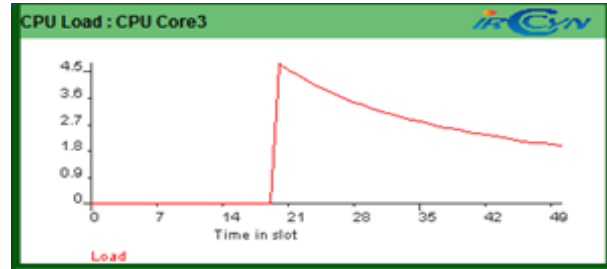


Fig. 3 CPU Core 3 load at 13% UF

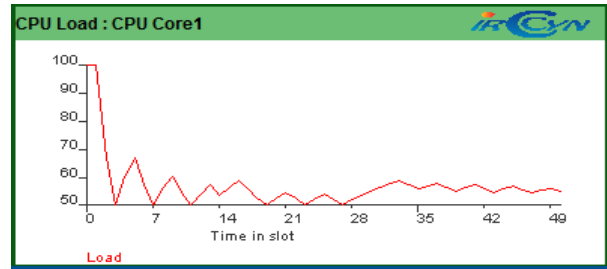


Fig. 4 Power Consumption CPU Core 1 at 13% UF

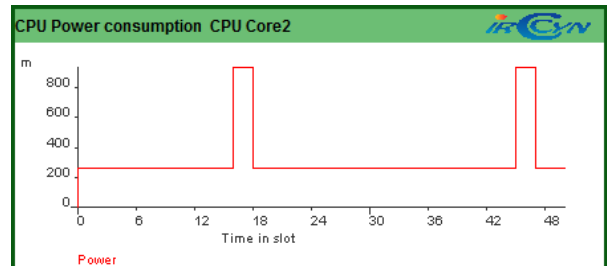


Fig. 5 Power Consumption CPU Core 2 at 13% UF

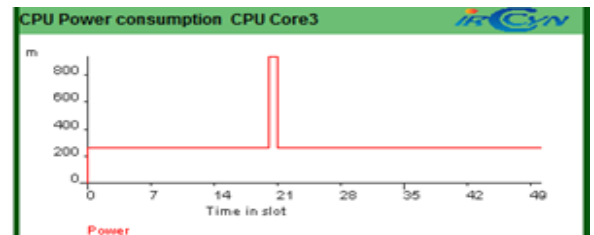


Fig. 6 Power Consumption CPU Core 3 at 13% UF

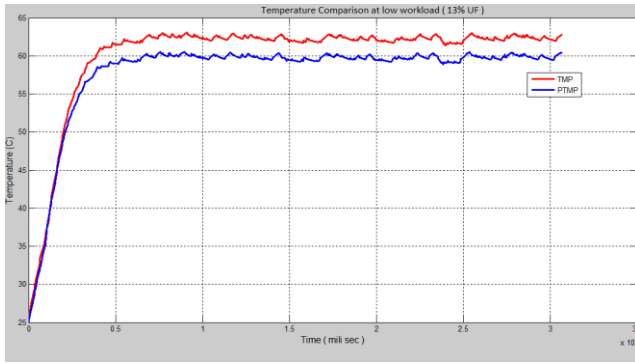


Fig. 7 Temperature's variation at Low workload on 26°C ambient temperature

## 6. Conclusion and Future Work

In this research work functional simulation on STORM and thermal model and proved its practicability in the context of MPSoC. A large amount of techniques now a day's doesn't consider the affect of environmental temperature which can be investigated in future work. Majority of the current algorithms defines only for homogeneous multi-core systems which can be extensive to heterogeneous multi-core systems.

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