Stability Analysis and Optimization of Simulated Annealing (SA) Algorithm Based PID Controller for DC-DC SEPIC Converter

Mirza Muntasir Nishat\textsuperscript{1}, Fahim Faisal\textsuperscript{2*}, Md Ashraful Hoque\textsuperscript{3*}, Anik Jawad Evan\textsuperscript{4*}, Md. Moshiour Rahaman\textsuperscript{5*}, Md. Sadman Sifat\textsuperscript{6*} and H. M. Fazle Rabbi\textsuperscript{7*}
{mirzamuntasir, faisalee, mahoque, anikjawadevan, moshiourrahaman, sadmansifat, hmfazlerabbi}@iut-dhaka.edu
\textsuperscript{1}Department of Electrical and Electronic Engineering
Islamic University of Technology (IUT)
Board Bazar, Gazipur -1704, Bangladesh

Abstract
This paper presents an investigative study on closed loop stability of SEPIC (Single-Ended Primary Inductor Converter) converter. Simulated Annealing algorithm based optimization technique is deployed to design an optimized controller for the SEPIC converter. Simulated Annealing (SA) algorithm is an algorithm based on the principles of thermodynamics where the analogy of cooling of metal and freezing into a minimum energy level is utilized and is widely used as an optimization technique in power electronics. State Space Average method is employed to model and obtain the transfer function of the converter based system. Hence, SA based PID controller is designed so that the stability of the converter can be evaluated and compared with conventional PID controller. Different performance parameters like percentage of overshoot, rise time, settling time and peak amplitude are taken into account to investigate the stability of the system by two fitness functions (IAE and ISE). MATLAB is used in order to carry out the simulations and hence, a comparative study is reported where the performances are evaluated.

Key words
Simulated Annealing Algorithm, PID Controller, SEPIC Converter, proportional-integral-derivative gains

1. Introduction
Ample amount of nonlinear optimization algorithms is maneuvered in different times by a lot of researchers to handle the nonlinearity of the complex systems [1-2]. Amongst them, simulated annealing algorithm appears to be one of the most flexible and versatile algorithms as it showcases the unique ability of not getting trapped in local minima [3-4]. Moreover, it does not rely on any restrictive properties of the model and can be easily tuned. Other optimization techniques have their own merits and demerits. For example, in neural network, the nets learn to approximate a function and possess adaptive characteristics in model changing environments [5]. However, traditional hill climb methods may fail to find out the global optimum value and can get stuck in a local minima or maxima [6]. However, simulated annealing algorithm searches for global optimum value of the system.

Among various nonlinear systems, power converters are the most common ones. Different power converters like Buck, Boost, Buck-Boost and SEPIC converters are associated with nonlinearity [7-8]. However, SEPIC converter depicts high nonlinear behavior and to investigate that phenomenon, controller is employed so that the closed loop response can be obtained in a satisfactory manner [9-11]. For this reason, PID controller is deployed in the system but determining the optimized values of the PID controller requires a lot of time through trial and error process [12-13]. Therefore, in this paper, SA is called into action so that the algorithm can take the charge of determining the optimized values of the PID controller for which there will be less overshoot at the initial stage, making the system suitable for battery charging and other low voltage applications.

In section 2, SEPIC converter is analyzed and mathematical modeling is done in order to obtain the transfer function of the system. Then design of the overall system is discussed in section 3. Hence, in section 4, all the simulation results are presented and overall comparative analysis is carried out. The conclusion is presented in section 5. All the simulations are done in MATLAB environment.

2. State Space Representation of Conventional SEPIC Converter
State Space Average method is a widely used technique to model different power converter circuits [14]. The mathematical model of conventional SEPIC converter is
presented for both ON and OFF condition of the switch (S). The corresponding figures and equations are depicted below:

\[ V_o = \frac{dV_s}{1-d} \]  

Hence, the internal state variables and the output variables are stated with a view to obtaining a time-domain solution. The state variables of SEPIC are considered as currents and voltages, respectively. When the converter is in continuous conduction mode, the operation can be illustrated for two cases:

(A) Switch (S) is ON and Diode (D) is OFF
(B) Switch (S) is OFF and Diode (D) is ON

\[ \frac{dI_{L1}}{dt} = \frac{1}{L_1} (r_{s1}I_{L1} + V_s) \]  

\[ \frac{dI_{L2}}{dt} = \frac{1}{L_2} \left[ -\left(r_{c1} + r_{L2}\right)I_{L2} + V_c \right] \]  

\[ \frac{dV_{c1}}{dt} = -\frac{1}{C_1} I_{L2} \]  

\[ \frac{dV_{c2}}{dt} = -\frac{1}{C_2} \left( R_o + r_{c2} \right) V_{c2} \]  

\[ \frac{dI_{L1}}{dt} = \frac{1}{L_1} \left[ -\left(r_{c1} + r_{L1} + r_{c2}r_a\right)I_{L1} - r_{c2}r_aI_{L2} - V_c - r_{c2}V_{c2} \right] \]  

\[ \frac{dI_{L2}}{dt} = \frac{1}{L_2} \left[ r_{c2}r_aI_{L1} - \left(r_{L2} + r_{c2}r_a\right)I_{L2} - r_{c2}V_{c2} \right] \]  

\[ \frac{dV_{c1}}{dt} = \frac{1}{C_1} I_{L1} \]  

\[ \frac{dV_{c2}}{dt} = \frac{1}{C_2} \left[ r_{c1}I_{L1} + r_{c2}I_{L2} - \frac{1}{R_o + r_{c2}} V_{c2} \right] \]  

where,  

\[ r_a = \frac{R_o}{r_{c2} + R_o} \]  

For \( r_{c1} = r_{c2} = 0, r_a = 1 \), putting the value in above equations the simplified forms are obtained and they are as follows:

(i) For S ON and D OFF:

\[ \frac{dI_{L1}}{dt} = \frac{1}{L_1} \left(-r_{s1}I_{L1} + V_s\right) \]  

For S OFF and D ON:

\[ \frac{dI_{L1}}{dt} = \frac{1}{L_1} \left[ -\left(r_{c1} + r_{L1} + r_{c2}r_a\right)I_{L1} - r_{c2}r_aI_{L2} - V_c - r_{c2}V_{c2} \right] \]  

\[ \frac{dI_{L2}}{dt} = \frac{1}{L_2} \left[ r_{c2}r_aI_{L1} - \left(r_{L2} + r_{c2}r_a\right)I_{L2} - r_{c2}V_{c2} \right] \]  

\[ \frac{dV_{c1}}{dt} = \frac{1}{C_1} I_{L1} \]  

\[ \frac{dV_{c2}}{dt} = \frac{1}{C_2} \left[ r_{c1}I_{L1} + r_{c2}I_{L2} - \frac{1}{R_o + r_{c2}} V_{c2} \right] \]  

So, the overall equation becomes,

\[ V_s dT + (-V_o)(1-d)T = 0 \]
It is inferred that the time domain parameters of the original order model by retaining the dominant poles. Thus, of the reduced order model remains the same as that of the \[\ \text{cond} \ \]

In order to reduce the computation time and complexity in the controller design, the fourth-order system is converted into the second-order system so that the transient behavior of the reduced order model remains the same as that of the original order model by retaining the dominant poles. Thus, it is inferred that the time domain parameters of the reduced order model are retained as that of the original fourth order model. There are various model order reduction methods available. Here, the moment matching technique has been applied to reduce the fourth-order system into the second-order system [17]. The technique is essentially the matching of time-moments of full order model’s response to those of the reduced order model. The transfer function for third order reduced model is given by the following equation:

\[
H_3(s) = \frac{a_{11} + a_{12}s + a_{13}s^3}{1 + a_{21}s + a_{22}s^2 + a_{23}s^3}
\]  

Here, the values of \(a_{11}\) to \(a_{33}\) are found by using the coefficients \(C_0, C_1, C_2, C_3, C_4, C_5\) which are given in the following equations:

\[
\begin{align*}
    a_{31} &= \begin{bmatrix} a_{11} & a_{12} \\ C_1 & C_2 \\ C_3 & C_4 \\ C_5 & \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ C_0 & 0 \\ 0 & 0 \\ 0 & \end{bmatrix} \\
    a_{22} &= \begin{bmatrix} 0 \end{bmatrix} + \begin{bmatrix} 0 & C_0 \\ 0 & C_1 \\ 0 & C_2 \\ 0 & C_3 \\ 0 & C_4 \\ 0 & C_5 \end{bmatrix} \\
    a_{23} &= \begin{bmatrix} 0 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & C_0 \\ 0 & C_1 \\ 0 & C_2 \\ 0 & C_3 \\ 0 & C_4 \\ 0 & C_5 \end{bmatrix}
\end{align*}
\]

After that, the general expression for the reduced second-order transfer function is given as:

\[
H_2(s) = \frac{a_{21} + a_{22}s}{1 + a_{21}s + a_{22}s^2}
\]

The values of \(a_{11}, a_{12}, a_{21}, a_{22}\) are found by using the coefficients \(C_0, C_1, C_2, C_3\) which are mentioned below:

\[
\begin{align*}
    a_{11} &= \begin{bmatrix} C_1 & C_0 \\ C_2 & C_1 \\ C_3 & C_2 \\ C_4 & C_3 \\ C_5 & C_4 \end{bmatrix} \\
    a_{12} &= \begin{bmatrix} 0 & C_0 \\ 0 & C_1 \\ 0 & C_2 \\ 0 & C_3 \\ 0 & C_4 \\ 0 & C_5 \end{bmatrix} \\
    a_{21} &= \begin{bmatrix} 0 \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & C_0 \\ 0 & C_1 \\ 0 & C_2 \\ 0 & C_3 \\ 0 & C_4 \\ 0 & C_5 \end{bmatrix} \\
    a_{22} &= \begin{bmatrix} 0 \end{bmatrix} + \begin{bmatrix} 0 & C_0 \\ 0 & C_1 \\ 0 & C_2 \\ 0 & C_3 \\ 0 & C_4 \\ 0 & C_5 \end{bmatrix}
\end{align*}
\]

Thus, the reduced model is obtained so that this transfer function can be utilized to inspect the stability of the DC-DC SEPIC converter.
3. Simulated Annealing Algorithm (SA)

3.1 Overview of SA

SA refers to an optimization technique, based on the principles of thermodynamics. Here, the analogy of cooling of metal and freezing into a minimum energy level is brought into action [18]. The main objective of this algorithm is to find the global optimum value of the system. Moreover, the simulated annealing algorithm is capable of dealing complex nonlinear systems and appears to be more versatile, robust and handy than other search algorithms. However, the algorithm is metaheuristic and computing time is high.

![Flow Chart of Simulated Annealing (SA) algorithm](image)

The algorithm starts by initializing a very high temperature and perturbing the placement through a defined move. After that the score is calculated and depending on the change in score the decision is taken whether it is to be accepted or rejected. Hence the value is updated and process is repeated until freezing point is reached. The flowchart of the algorithm is illustrated in Fig. 3.

3.2 Objective Function

In this paper, two performance indices are taken into account to minimize the errors which imply quantitative measure in order to portray the performance of the PID controller. The indices are defined as Integral of Absolute Magnitude of Error (IAE) and Integral of Squared Error (ISE) [19].

\[
IAE = \int_0^\infty |e(t)| dt \quad (25) \\
ISE = \int_0^\infty e(t)^2 dt \quad (26)
\]

3.3 Design of SAPID Controller in SEPIC Converter

PID controller parameters are attained with the help of Simulated Annealing (SA) algorithm. The fitness function will be evaluated and thus the optimized values of the controller will be obtained to inspect the stability of the system. The basic block diagram of SA-PID controller is displayed in Fig. 4.

![Basic Block Diagram of SA based PID Controller](image)

4. Simulation Results and Analysis

The parameters of the converter circuit shown in Table 1

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>( V_{in} )</td>
<td>10 V</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>( f_s )</td>
<td>100 KHz</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>( d )</td>
<td>0.5</td>
</tr>
<tr>
<td>Inductor</td>
<td>( L_1, L_2 )</td>
<td>100 ( \mu )F</td>
</tr>
<tr>
<td>Resistor</td>
<td>( r_{L1}, r_{L2} )</td>
<td>1 m( \Omega )</td>
</tr>
<tr>
<td></td>
<td>( r_{C2} )</td>
<td>3 m( \Omega )</td>
</tr>
<tr>
<td></td>
<td>( r_{C2} )</td>
<td>1 m( \Omega )</td>
</tr>
<tr>
<td>Capacitor</td>
<td>( C_1, C_2 )</td>
<td>800 ( \mu )F, 3 mF</td>
</tr>
<tr>
<td>Load Resistance</td>
<td>( R_o )</td>
<td>1 ( \Omega )</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>( V_o )</td>
<td>10 V</td>
</tr>
</tbody>
</table>
4.1 Open Loop Analysis

At first, open loop analysis is carried out to observe the system’s performance. In Fig. 5, it is shown that the steady state is achieved approximately at 0.03 sec. Moreover, it is observed that percentage of overshoot is 64%, peak amplitude is 1.63, rise time is 0.000902s and settling time is 0.0203s. Hence, it is evident that overshoot is really high in terms of open loop response which needs to be reduced as it is a major concern for different application of SEPIC converter.

![Fig. 5 Voltage amplitude Vs. Time for output of open loop response](image)

To enhance the performance of the converter, closed loop techniques are employed by many researchers in different time. Among various methods, PID controller is the most widely employed method and researchers implement this control technique to investigate and improve the performance of power converters.

4.2 Closed Loop with conventional PID

PID controller comprises of three terms named as Proportional, Integral and Derivative component which are tuned by empirical methods like Ziegler-Nicholas method [21], analytical methods and different optimization techniques. However, it is not easy to determine the exact values of these parameters as most of the classical methods demand explicit mathematical modeling of the processing plant and may not provide satisfactory results because of input-output disturbances or nonlinear behavior of the plant.

The mathematical representation of a conventional PID controller can be written. From this, the transfer function can also be generated.

\[
U(t) = k_i \int e(t) dt + k_p e(t) + k_d \frac{d}{dt} e(t) \quad (3.29)
\]

So, the transfer function of the PID controller is given below:

\[
\frac{U(s)}{E(s)} = k_p + \frac{k_i}{s} + s k_d = k_p \left( 1 + \frac{1}{T_i s} + s T_d \right)
\]

Typical PID controller structure is depicted in Fig 6.

![Fig. 6 Typical PID controller structure model](image)

Here, \(k_p\), \(k_i\) and \(k_d\) are designated as the proportional, integral and derivative constants of the PID controller respectively. However, the values of the \(k_p\), \(k_i\) and \(k_d\) need to be tuned to achieve better results. Conventional PID controller is employed in SEPIC converter and the step response is taken to inspect the stability of the system which is shown in Fig. 7.

In closed loop analysis, it is observed that the overshoot it is 11% which is much less than open loop analysis. Moreover, rise time and settling time have also improved and they are 0.000954s and 0.000639s respectively. In addition, peak amplitude has also decreased and it is 1.11 which leads to steady state error.

![Fig. 7 Step Response of Conventional PID Controller for SEPIC converter](image)
But this approach takes a lot of time as the parameters are obtained through manual tuning. Therefore, nonlinear optimization technique is implemented by many researchers in PID controller so that the optimized values of parameters can be attained with the help of algorithm development. Thus, better performance will be achieved without manual intervention.

4.3 SA based PID Controller

In Simulated Annealing algorithm, initial temperature is a major concern as it determines the solution space in order to search for optimal values of the controller. In this section, initial temperature is kept at 100. The optimized values of the PID controller and output of performance indices are shown accordingly. The parameters are listed in Table 2.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial Temperature</td>
<td>100</td>
</tr>
<tr>
<td>Temperature Update</td>
<td>Exponential Temperature Update</td>
</tr>
<tr>
<td>Reannealing Interval</td>
<td>100</td>
</tr>
<tr>
<td>Annealing Function</td>
<td>Fast Annealing</td>
</tr>
</tbody>
</table>

4.3.1 Simulation Results

In Table 3, the gain values ($k_P$, $k_I$ and $k_D$) of PID controller for SA- PID are presented.

<table>
<thead>
<tr>
<th>Gains</th>
<th>IAE</th>
<th>ISE</th>
</tr>
</thead>
<tbody>
<tr>
<td>$k_P$</td>
<td>23.815</td>
<td>39.705</td>
</tr>
<tr>
<td>$k_I$</td>
<td>1006.452</td>
<td>2012.13</td>
</tr>
<tr>
<td>$k_D$</td>
<td>0.02</td>
<td>0.02</td>
</tr>
</tbody>
</table>

Step responses for IAE and ISE are illustrated in Fig. 8, and Fig. 9. The overall comparative analysis of the step responses is illustrated in Fig. 10. At first, step response of IAE is manifested. Here, rise time is 0.000665 s, settling time is 0.000104 s, overshoot is 1.3% and peak amplitude is 1.01.

Secondly, step response of ISE is illustrated in case of SA-PID. For this, rise time is 0.000622 s, settling time is 0.000334 s, overshoot is 3.04% and peak amplitude is 1.03.

4.3.2 Comparative Analysis

Finally, comparative analysis of step responses for SA-PID with the conventional PID controller is observed and shown in Fig. 10. It is evident that SA based controller has shown better result for IAE with respect to the conventional PID controller in terms of overshoot. The performance parameters are tabulated for SA-PID which is presented in Table 4.
Table 4 Evaluation of Performance Parameters for SA-PID

<table>
<thead>
<tr>
<th>Performance Parameters</th>
<th>Conventional PID</th>
<th>SA-PID</th>
</tr>
</thead>
<tbody>
<tr>
<td>%OS</td>
<td>11</td>
<td>2.2</td>
</tr>
<tr>
<td>Tr</td>
<td>0.000954</td>
<td>0.000665</td>
</tr>
<tr>
<td>Ts</td>
<td>0.000639</td>
<td>0.000104</td>
</tr>
<tr>
<td>Peak Amplitude</td>
<td>1.11</td>
<td>1.01</td>
</tr>
</tbody>
</table>

5. Conclusion

In this paper, a stability analysis of closed loop SEPIC converter is presented based on an optimized design of SA based PID controller. It is observed that IAE depicts more optimized result in terms of overshoot (2.2%) than ISE where the overshoot is 3.04%. Though rise time of IAE (0.000665s) is slightly higher than that of ISE (0.000622s), settling time is less for IAE (0.000104s) with respect to ISE (0.000334s). Moreover, peak amplitude is less for IAE than ISE which leads to less steady state error. Therefore, SA based PID controller by using IAE is the most optimized approach for SEPIC converter.

References


