Simulation and Analysis of Non-isolated High Step-Up DC-DC Boost Converter for Renewable Energy Systems

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Abstract
This paper proposes a novel cascaded DC-DC boost converter aimed for PV applications. It consists of a conventional boost unit and a voltage multiplier network. The proposed configuration greatly enhances voltage gain while operating at low duty cycles. The extensive analysis is performed for the proposed converter in continuous current mode (CCM) and discontinuous current mode (DCM). Moreover, critical values of inductors are determined to investigate the boundary conditions between CCM and DCM. It was firmly concluded that while considering the lesser number of elements and semiconductor devices for the same input voltage, the proposed converter can yield comparatively high voltage gain than the conventional and recent boost dc-dc converters. Finally, the desired validation of the mathematical expressions is inspected via simulation results.

Key words:
Photovoltaic system; Voltage multiplier; High voltage gain

1. Introduction

Environmental outcomes of using fossil fuels and depletion of their reserves have made it obligatory to promote clean and sustainable energy sources. Environmental pollution turns into a terrible issue by the adoption of fossil fuels for energy production, which is emitting several billion tons of CO2 per year. To scale down the production of CO2, renewable energy sources such as photovoltaic (PV), wind turbine, waves, and geothermal are adopted in numerous industrial applications [1,2]. Renewable sources such as solar photovoltaic (PV) and wind are progressively being used in consequence of the environmental interest, and it is leading in the technology and rapidly declining manufacturing cost [3,4]. However, the intermittent nature of renewable sources and the unpredictability of the demand for load present a challenge for the broad promotion of these clean sources of energy [5,6]. The output of these renewable sources has remarkably low voltage value. Therefore, high step-up DC-DC converters are exceedingly desirable to operate a load that requires a high operating voltage. High step-up DC-DC converters can be used as an interface in such systems to improve the output voltage [7]. Such converters can be operated using two separate methods: PWM and frequency variations. The PWM-controlled DC-DC converters are categorized into two classes, non-isolated and isolated. In terms of simplicity and cost-effectiveness, conventional non-isolated step-up PWM converters such as boost, buck-boost, and Sepic, etc. have perceptible features [8,9]. Unfortunately, the gain from such converters is reduced due to circuit parameters and heavy-duty cycle operation in order to achieve high voltage gains, which in effect decreases the converter output to a high degree.

Different methods have been presented in the literature that utilizes different voltage boosting techniques such as multilevel, interleaved, or cascaded topologies, or using voltage multiplier cells (VMC)[10-13], or possibly combined with switched capacitors (SCs) and/or coupled inductors. A new hybrid DC-DC converter is presented in [14], different switched capacitors techniques and coupled inductors are merged with a conventional boost converter to achieve high voltage gain. The advantages of this technique are high voltage, low current and voltage stress on elements, and using a single switch; however, the converter has a large number of components, which results in increased cost, losses, and size of the converter. Converter presented in [15] can achieve high voltage gain at low duty cycles, and the structure can be extended to n stages, which further increases the voltage gain of the converter. The voltage stress on the components compared with output voltage is decreased; however, a number of switches are employed, which complicates the control tactics, and hence the cost as separate driving circuitry is required to drive the switches. A new structure by combining coupled inductor and voltage lift technique is presented in [16]. High voltage gain can be achieved by adjusting the turns ratio of the coupled inductor, and stress on semiconductors is low; however, the voltage gain is proportional to the turns ratio of the coupled inductor, which increases the size and causes EMI issues. A new topology of step-up dc-dc converter using voltage lift technique is proposed in [17]. Capacitor–inductor-capacitor (CLC) cells are developed to increase the voltage gain, and the converter can further be extended to N-lift topology to enhance the voltage gain. The converter employs a single switch and has low switching voltage; however, high voltage gain is achieved at the price of

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utilizing a large number of elements, which degrades converter efficiency and also increases the cost.

In this study, a new structure of a DC-DC boost converter is presented to achieve high voltage gain. The proposed solution optimally implements the cascade connection of a conventional boost and a voltage multiplier circuit. The proposed converter possesses the capability of achieving high voltage gain at a reasonably low duty cycle, which makes it more suitable for medium and high voltage applications. For instance, in DC microgrids, they can be used to interface various low power voltage sources like batteries, photovoltaic (PV) panels, and fuel cells into a universal DC bus (380V) Voltage. Proposed converter topology, operation principles, and characteristics waveforms are discussed in Section 2.

2. The proposed structure

The proposed converter circuit is elucidated in Fig 1. Which is comprised of three inductors, two switches, three capacitors, and four diodes? PWM technique is employed to control the switch operates at a switching frequency of 10 kHz. To simplify the analysis of the proposed converter, few presumptions are made. i) Steady-state operation of the converter is considered. ii) The voltage ripple for each capacitor is ignored due to sufficient capacitor value; therefore, the capacitor's voltage during on and off period is comparable iii) The current ripple for each inductor is ignored in CCM operation only. iv) The effect of parasitic elements is neglected.

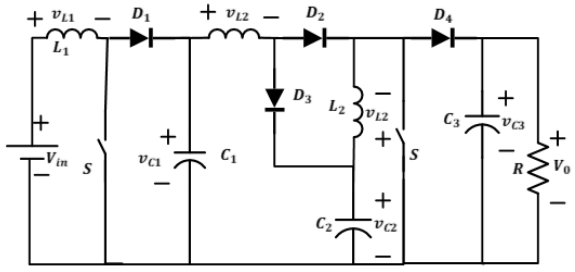

Fig. 1 Structure of the proposed converter

2.1 Proposed converter operation in CCM.

At a time when both the switches are on, diodes D_1, D_3 and D_4 are reverse biased and diode D_2 is forward biased (**Fig** 2). The supply voltage V_i is delivering energy to the inductor L_1. This energy is stored in the magnetic field of inductor L_1, and its current is linearly increased from its minimum value I_{LV1} to its final value I_{LP1} as illustrated in **Fig 3**. Since capacitor C_1 is detached from the supply voltage, the voltage of the capacitor C_1 is dropped to the lowest value V_{CV2} by liberating its stored energy to the inductor L_2 and hence current in the inductor L_2 is raised from the lowest value I_{LV2} to its highest value I_{LP2}. In the meanwhile, the capacitor C_2 is discharged through the inductor L_3 and its voltage is dropped from the peak value V_{CP2} to the lowest value V_{CV1}, while current in the inductor L_3 is boosted from its minimum value I_{LV3} to its maximum value I_{LP3}. Also, capacitor C_3 is providing energy to the load as D_4 is reverse biased. The voltage of the capacitor C_3 is dropped from the maximum value V_{CP3} to the lowest value V_{CV3}. The currents and voltages of all the four diodes during CCM are demonstrated in **Fig 4.**

In the next cycle when both the switches are off, diodes D_1, D_3 and D_4 are forward biased and diode D_2 is reverse biased. Inductor L_1 releases its stored energy to Capacitor C_1 and the voltage of the capacitor C_1 is reached to the maximum value V_{CP2} at time T_{off}, while current in the inductor is reduced to a minimum value of I_{LV1}. In the meanwhile, inductor L_2 donates the stored energy to the capacitor C_2 and voltage of C_2 is raised to a peak value V_{CP2} , while current in the inductor L_2 is dropped to I_{LV2}. Also, Inductor L_3 is discharged through a capacitor C_3 and load. Current in inductor L_3 is reduced to I_{LV3} and the voltage of the capacitor C_3 is raised to the maximum value V_{CP3}.

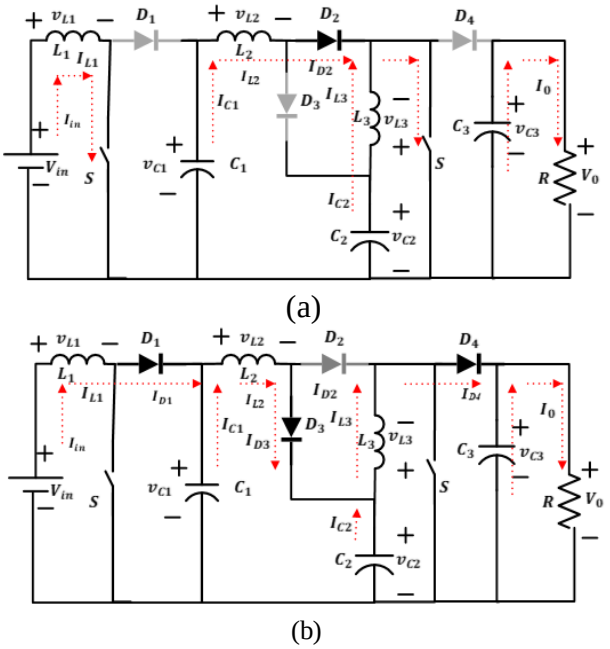

Fig. 2 Proposed converter (a) during the on-switching period; (b) during the off- switching period.

Voltage and current equations of inductors in CCM:

At time T_{on}, voltage and current relations of inductors L_1, L_2 and L_3 are obtained as:

$$\begin{cases} v_{L1,1} = V_i = L_1 \dfrac{di_{L1,1}}{dt} = \dfrac{\Delta i_{L1,1}}{T_{on}}; i_{L1,1} = \dfrac{V_i}{L_1} t + I_{LV1} \\ v_{L2,1} = L_2 \dfrac{di_{L2,1}}{dt} = v_{C1,1} = \dfrac{V_i}{(1-D)}; i_{L2,1} = \dfrac{v_{C1,1}}{L_2} t + I_{LV2} \\ v_{L3,1} = L_3 \dfrac{di_{L3,1}}{dt} = v_{C2,1}; i_{L3,1} = \dfrac{v_{C2,1}}{L_3} t + I_{LV3} \end{cases} \quad (1)$$

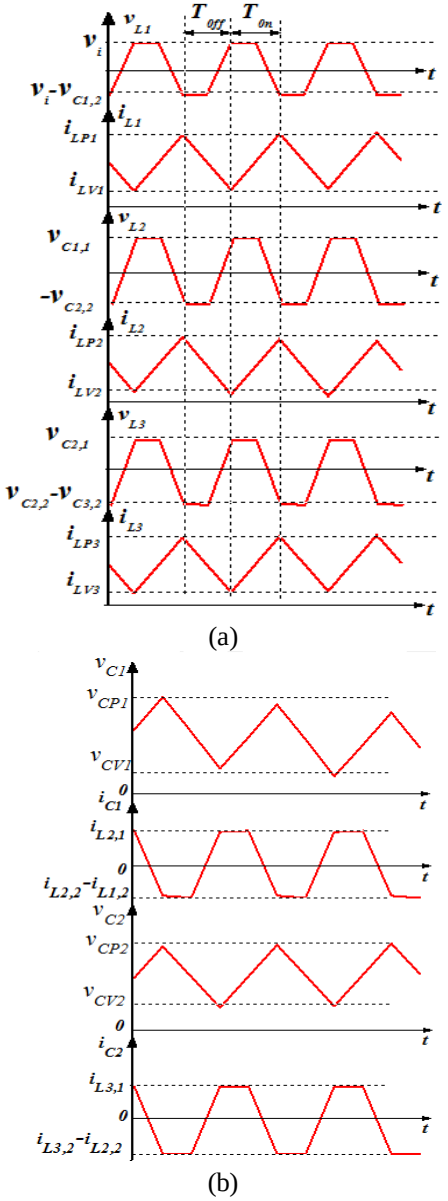

Fig. 3 The current and voltage waveforms in CCM for; (a) Inductors L1, L2, L3 (b) Capacitors C1, C2.

In the time interval of T_{off}, voltage and current relations of inductors L_1, L_2 and L_3 are acquired as:

$$\begin{cases} v_{L1,2} = V_i - v_{C1,2} = L_1 \dfrac{di_{L1,2}}{dt} = -\dfrac{\Delta i_{L1}}{T_{off}}; i_{L1,2} = -\dfrac{(V_i - v_{C1,2})}{L_1} t + I_{LP1} \\ v_{L2,2} = L_2 \dfrac{di_{L2,2}}{dt} = v_{C1,2} - v_{C2,2}; i_{L2,2} = -\dfrac{(v_{C1,2} - v_{C2,2})}{L_2} t + I_{LP2} \\ v_{L3,2} = L_3 \dfrac{di_{L3,2}}{dt} = v_{C2,2} - v_{C3,2}; i_{L3,2} = -\dfrac{(v_{C2,2} - v_{C3,2})}{L_3} t + I_{LP3} \end{cases} \quad (2)$$

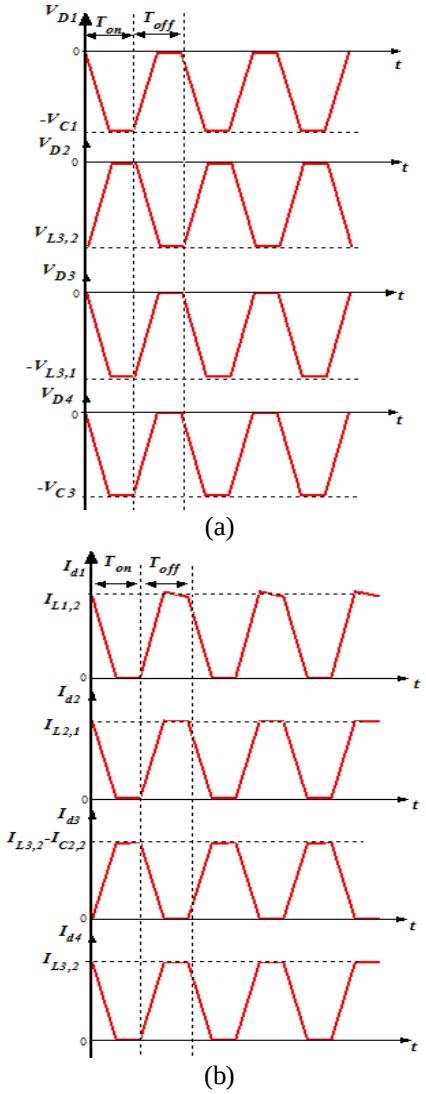

Fig. 4 The current and voltage waveforms in CCM for; Diodes D1, D2 D3, D4.

Voltage and current equations of capacitors in CCM:

By applying inductor volt-sec balance rule for inductors L_1, L_2 and L_3 and applying KCL (**Fig** 2(a) and (b)), Capacitors C_1, C_2, and C_3 voltages and currents can be earned as:

$$\begin{cases} v_{C1,1}=v_{C1,1}=v_{C1,2}=v_{C1}=\dfrac{V_i}{(1-D)};\ I_{C1,1}=I_{L2,1},I_{C1,2}=I_{L2,2}-I_{L1,2} \\ v_{C2,1}=v_{C2,2}=v_{C2}=\dfrac{V_i}{(1-D)^2};\ I_{C2,1}=I_{L3,1},I_{C2,2}=I_{L3,2}-I_{L2,2} \\ v_{C3,1}=v_{C3,2}=v_{C3}=\dfrac{V_i}{(1-D)^3};\ I_{C3,1}=-I_0,I_{C3,2}=I_0-I_{L3,2} \end{cases} \quad (3)$$

Voltage and current equations of Diodes in CCM:

At the time T_{on} and T_{off} , Diodes voltages and currents can be calculated as:

$$\begin{cases} V_{D1}=-V_{C1};I_{D1}=i_{L1,2};V_{D2}=V_{L3,2},I_{D2}=i_{L2,1} \\ V_{D3}=-V_{L3,1};I_{D3}=i_{L3,2}-i_{C2,2};V_{D4}=-V_{C3},I_{D4}=i_{L3,2} \end{cases} \quad (4)$$

Voltage gain and current ratio of the proposed converter in CCM:

Considering the converter without losses, voltage gain, and current ratio are deducted as:

$$\begin{cases} \dfrac{V_0}{V_i}=\dfrac{1}{(1-D)^3} \end{cases} \quad (5)$$

$$\begin{cases} \dfrac{I_0}{I_i}=(1-D)^3 \end{cases} \quad (6)$$

2.2 Proposed converter operation in DCM.

In this section, the proposed converter is analyzed extensively during DCM. Significant current and voltage relations are established, and graphs depicting these relations are also demonstrated. The converter has three modes of operation during DCM. The equivalent circuits during DCM operation are shown in **Fig** 2 and 5 (the grey color signifies off-state of diodes). The characteristics waveforms during DCM are shown in **Figs**.6 and 7.

Mode I.

During on-switching time (t_0, t_1), diodes D_1, D_3 and D_4 are reverse biased, and diode D_2 is forward biased, as illustrated in **Fig** 2 (a). Similar to CCM operation, Input voltage V_i supplies energy to the inductor L_1 and the current in inductor L_1 is increased to its maximum value I_{LP1}(**Fig** 7). Capacitor C_1 being cut off from source voltage, discharged through the inductor L_2 and its voltage is dropped to the lowest value V_{CV1} As a result, the inductor L_2 current is elevated from the lowest value I_{LV2} to highest value I_{LP2}. In the meanwhile, capacitor C_2 is discharged through the inductor L_3, mounting inductor's L_2 current to the maximum value I_{LP3}. The voltage of the capacitor C_2 is descended to the minimum value V_{CV2}. During this time interval, the capacitor C_3 is providing energy to the load and its voltage is dropped to the lowest value V_{CV3} (**Fig 8**).

Mode II.

During the off-switching period at a time (t_1, t_2) diode D_2 is reverse biased and diodes D_1, D_3 and D_4 re forward biased analogous to CCM. Inductor L_1 releases the stored energy to the capacitor C_1 and its current drops to zero at the end of time interval (t_1, t_2), while the voltage of the capacitor C_1 is reached to the maximum value V_{CP2}. The current in the inductor L_2 falls to zero at the end of time interval (t_1, t_2) by liberating its stored energy to the capacitor C_2, thus the voltage of the capacitor C_2 attained to the highest value V_{CP2}. During this time interval (t_1, t_2), inductor L_3 provides energy to the capacitor C_3 and load and thus the voltage of the capacitor C_3 is reached to a peak value V_{CP3}. Also, current in the inductor L_3 is reduced to zero at the end of the time interval (t_1, t_2).

Mode III.

During the time (t_2, t_3), all the four diodes are reverse biased, and the inductors current is zero, as shown in **Fig 5**. Voltage of capacitors C_1 and C_2 is retained to peak values V_{CP1} and V_{CP2}, respectively since capacitor's C_1 and C_2 current is zero during this time interval. Capacitor C_3 continues to supply energy to the load by releasing its stored energy. Voltage of capacitor C_3 is reduced to the minimum value V_{CV3} at the end of the time interval (t_2, t_3).

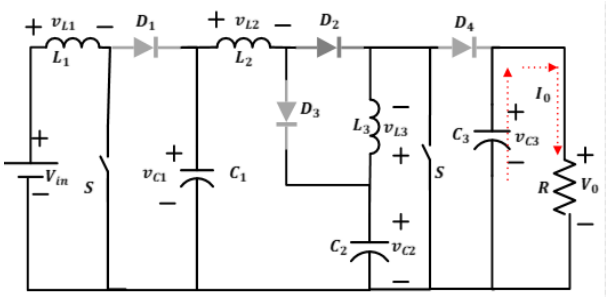

Fig. 5 Proposed converter during discontinuous inductor current (t2-t3)

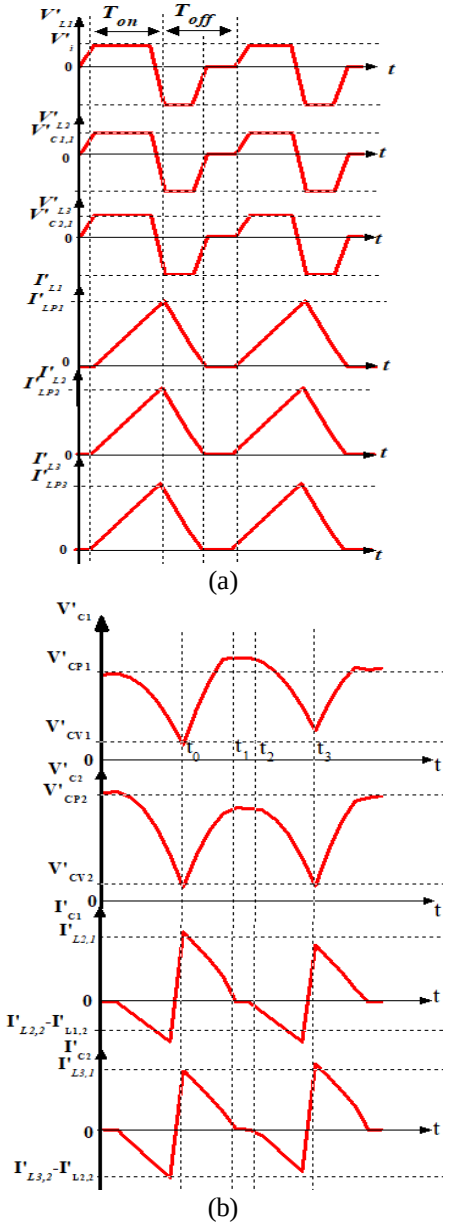

Fig. 6 The current and voltage waveforms in DCM for; (a) Inductors L1, L2, L3 (b) Capacitors C1, C2.

Voltage and current equations of inductors in DCM (at t DT *= and t =* $D'T$ ***).***

$$\begin{cases} v'_{L1,1} = V_i = L_1 \dfrac{di'_{L1,1}}{dt} = \dfrac{\Delta i'_{L1,1}}{T_{on}}; i_{L1,1} = \dfrac{V_i}{L_1} t + I_{LV1} \\ v'_{L2,1} = L_2 \dfrac{di'_{L2,1}}{dt} = v'_{C1,1} = \dfrac{V_i}{(1-D)}; i'_{L2,1} = \dfrac{v'_{C1,1}}{L_2} t + I_{LV2} \\ v'_{L3,1} = L_3 \dfrac{di'_{L3,1}}{dt} = v'_{C2,1}; i'_{L3,1} = \dfrac{v'_{C2,1}}{L_3} t + I_{LV3} \end{cases} \quad (7)$$

$$\begin{cases} v'_{L1,2} = V_i - v'_{C1,2} = L_1 \dfrac{di'_{L1,2}}{dt} = -\dfrac{\Delta i_{L1}}{T_{off}}; i'_{L1,2} = -\dfrac{\left(V_i - v'_{C1,2}\right)}{L_1} t + I_{LP1} \\ v'_{L2,2} = L_2 \dfrac{di'_{L2,2}}{dt} = v'_{C1,2} - v'_{C2,2}; i'_{L2,2} = -\dfrac{\left(v'_{C1,2} - v'_{C2,2}\right)}{L_2} t + I_{LP2} \\ v'_{L3,2} = L_3 \dfrac{di_{L3,2}}{dt} = v'_{C2,2} - v'_{C3,2}; i'_{L3,2} = -\dfrac{\left(v'_{C2,2} - v'_{C3,2}\right)}{L_3} t + I_{LP3} \end{cases} \quad (8)$$

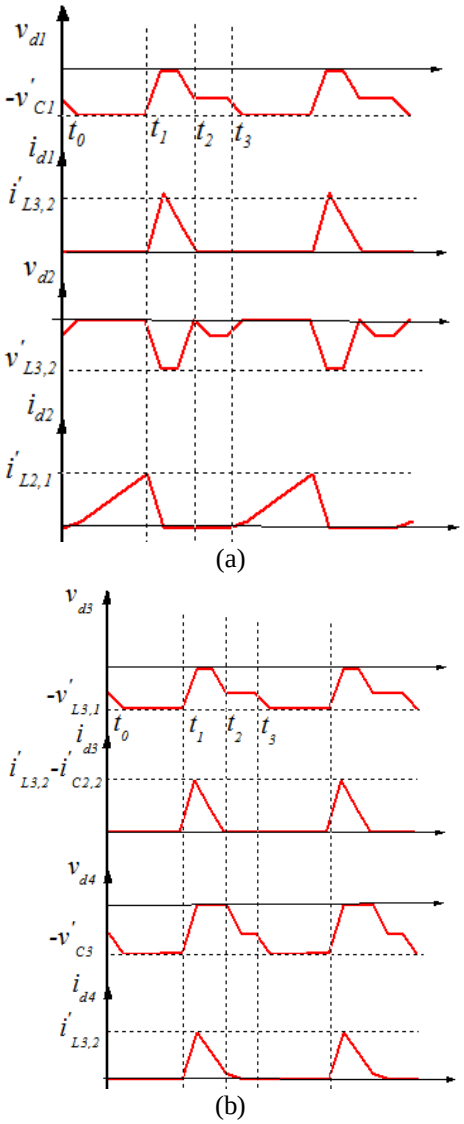

Fig. 7 The current and voltage waveforms in DCM for; (a) Diodes D1, D2 (b) Diodes D3, D4.

Voltage and current equations of capacitors in DCM (at $t\ DT$ *= and t =* $D'T$ ***).***

$$\begin{cases} v'_{C1,1}=v'_{C1,1}=v'_{C1,2}=v'_{C1}=\dfrac{V_i}{(1-D)};I'_{C1,1}=I'_{L2,1},I'_{C1,2}=I'_{L2,2}-I'_{L1,2} \\ v'_{C2,1}=v'_{C2,2}=v'_{C2}=\dfrac{V_i}{(1-D)^2};I'_{C2,1}=I'_{L3,1},I'_{C2,2}=I'_{L3,2}-I'_{L2,2} \\ v'_{C3,1}=v'_{C3,2}=v'_{C3}=\dfrac{V_i}{(1-D)^3};I'_{C3,1}=-I_0,I'_{C3,2}=I_0-I'_{L3,2} \end{cases} \quad (9)$$

Voltage and current equations of diodes in DCM (*at t = DT and t = $D'T$).*

$$\begin{cases} V'_{D1}=-V'_{C1},I'_{D1}=i'_{L1,2};V'_{D2}=V'_{L3,2},I'_{D2}=i'_{L2,1} \\ V'_{D3}=-V'_{L3,1},I'_{D3}=i'_{L3,2}-i'_{C2,2};V'_{D4}=-V'_{C3},I'_{D4}=i'_{L3,2} \end{cases} \quad (10)$$

Voltage gain in DCM is concluded as follow:

$$\begin{cases} \dfrac{V_0}{V_i}=\dfrac{\left(D+D'\right)^2+D^2+DD'}{D'^2} \\ \dfrac{V_0}{V_i}=\dfrac{\left(D+D'\right)^2+D^2+DD'}{D'^2} \end{cases} \quad (11)$$

Critical inductance:

The operation of the converter can be divided into two main groups, i.e., CCM and DCM, depending on the current value of the inductance. The margin between DCM and CCM operation can be determined founded on the critical inductance value of the inductances L_1 (L_{C1}), L_2 (L_{C2}), L_3 (L_{C3}). At critical mode, we have:

$$I_{LV1}+I_{LV2}+I_{LV3}=0 \quad (12)$$

And the critical inductances can be calculated as:

$$\begin{cases} L_{C1}=L_{C2}(1-D),L_{C2}=L_{C3}(1-D)^2,L_{C3}=\dfrac{V_i}{2I_0 f(1-D)} \end{cases} \quad (13)$$

The converter operates in CCM when $L_1 > L_{C1}$, $L_2 > L_{C2}$ and $L_3 > L_{C3}$ while operates in DCM when $L_1 < L_{C1}$, $L_2 < L_{C2}$ and $L_3 < L_{C3}$.

RMS calculation

For RMS calculation, a ripple in the inductor's current is ignored. RMS values of the inductors, diodes, capacitors, and switches are calculated as follow:

$$\begin{cases} I_{L1}=\dfrac{I_0}{(1-D)^3},I_{L2}=\dfrac{I_0}{(1-D)^2},I_{L3}=\dfrac{I_0}{(1-D)} \\ I_{D1,rms}=\dfrac{I_0}{(1-D)^3}\sqrt{(1-D)},I_{C1,rms}=\dfrac{I_0}{(1-D)^2}\sqrt{\dfrac{D\left[(1-D)+D(D-2)^2\right]}{(1-D)}} \\ I_{D2,rms}=\dfrac{I_0}{(1-D)^2}\sqrt{D},I_{C2,rms}=\dfrac{I_0}{(1-D)}\sqrt{\dfrac{D}{(1-D)}} \\ I_{D3,rms}=\dfrac{I_0}{(1-D)^2}\sqrt{(1-D)},I_{C3,rms}=I_0\sqrt{\dfrac{D}{(1-D)}} \\ I_{D4,rms}=\dfrac{I_0}{(1-D)}\sqrt{(1-D)},I_{s1,rms}=\dfrac{I_0}{(1-D)^3}\sqrt{D},I_{s2,rms}=\dfrac{I_0(2-D)}{(1-D)^2}\sqrt{D} \end{cases} \quad (14)$$

3. The comparison analysis between the proposed converter and other recent converters.

In this section, comparison analysis between the proposed converter and other boost converters cited in **Table 1** is made to verify the eminence of the proposed converter. The proposed converter is compared with the presented converters in terms of voltage gain and number of elements. Augmented and acceptable voltage gain is provided by the proposed converter with equal or fewer components than other presented converters. Based on the CCM operation, the curve of voltage gain variation with the duty cycle of the proposed converter and other converters is illustrated in **Fig 8**. **Table 1** also includes a comprehensive comparison in terms of enhanced voltage gain. The gain of the converter presented in [13] is proportional to the number of voltage multiplier cells. To achieve high voltage gain, the number of cells has to be increased and hence the number of elements (four elements per cell), which in result increases the size, cost, and power loss. Converters presented in [18-21] have more number of components than the proposed converter; moreover, the proposed converter has the additional advantage of augmented voltage gain in comparison with the above-mentioned converters. The converter in [22] has a single switch and an equal number of elements as that of the proposed converter, however, voltage gain is limited due to high duty cycle operation.

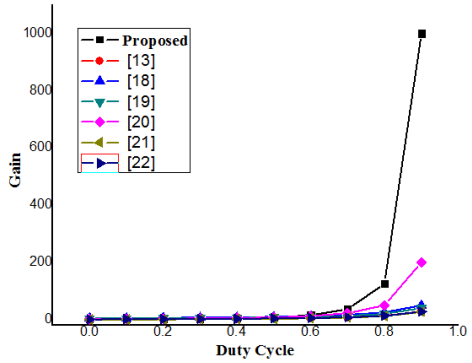

Fig. 8 Voltage gain comparison between the proposed converter and other recent converters.

Table 1: Voltage gain comparison between the proposed converter and other high gain converters.

	Proposed converter	Converter in [13]	Converter in [14]	Converter in [15]	Converter in[16]	Converter in [17]	Converter in[18]
Switches	02	01	02	02	01	01	01
Inductors	03	03	05	02	03	06	03
Capacitors	03	05	02	05	04	04	05
Diodes	04		05	04	05	03	03
Total count	12	12	14	13	13	14	12
Voltage gain	$\frac{1}{(1-D)^3}$	$\frac{1+n.D}{(1-D)}$ $n=2$ no. of stages	$\frac{-5}{(1-D)}$	$\frac{4}{(1-D)}$	$\frac{2}{(1-D)^2}$	$\frac{3D}{(1-D)}$	$\frac{1+2D}{(1-D)}$

Table 2: Converter specification

Parameters	CCM	DCM
R	200Ω	200Ω
L_1, L_2, L_3	8mH, 5mH, 6mH;	30µH, 130µH, 700µH
C_1,C_2, C_3	220uF, 80uF,220uF	220uF, 80uF,220uF
Diodes	MUR3060PT	MUR3060PT
Switch	IRF460Z	IRF460Z
Duty cycle	D = 50%	D = 50%
V_i, f	12V, 25kHz	12V, 10kHz

4. Simulation Results

In this section, Simulation results in PSIM 12.20 are provided to verify the theoretical analysis and validate the performance of the proposed DC-DC converter shown in Fig 1. Parameters used in the simulation are provided in **Table 2.**

Critical inductance

From equation (13), the critical inductance values $L_{C1,}$ $L_{C2,}$ and L_{C3} can be obtained as 666µH, 111µH, and 27.4µH, respectively, considering parameter values provided in **Table2**. With critical inductance values, the converter operates in critical mode and current in the inductors L_1, L_2, and L_3 reaches zero.

Simulation Results for CCM

The specifications of the components used for CCM operation are provided in **Table 3**. The simulation results are demonstrated in **Figs**. (9-10). The inductor L_1 voltage at time T_{on} reaches 12 V, as can be calculated from equation (1). At time T_{off}, inductor L_1voltage achieved to -11.8 V, which is also in accordance with equation (2). Also, at time T_{on}, inductor L_2 and L_3 voltages attained are 25 V and 50 V, respectively, which shows consistency with theoretical results in equation (1). At time T_{off}, the acquired voltages (-26 V and -51 V) illustrate the required consistency with the results obtained from equation (2). Similarly, voltages of capacitors C_1, C_2, and C_3 are approximately 23V, 49V, and 96V, which are desirably consistent with equation (3). Moreover, the voltages of all the four diodes achieved to -23.8V, -23.8V, -47.8V, and -96V, respectively, which dictates the required confirmation for equation (4). The acquired switch

current (2.4 A) is in accordance with equation (10). Furthermore, it is fairly evident from Fig 2(a)and (b) that the variation of inductors currents having peak values 3.9A, 1.9 A and 1.2 A, respectively are also consistent with theoretical expression given in equation (1) and finally all the diode and capacitor currents illustrated in **Figs**. **4** and **5** provide confirmation for equation (4).

Simulation Results for DCM

With the specifications given in **Table 6,** the converter operates in DCM. The simulation results in DCM are shown in **Figs**. 11 and 12. As shown in **Fig** 11, the voltage of the three inductors provides validation of equations 7 and 8. The voltage of the capacitors shown in Fig 17 is following equation (9). The voltage and current waveforms of the four diodes shown in **Fig** 12 reaffirm the theoretical analysis given in equation (10).

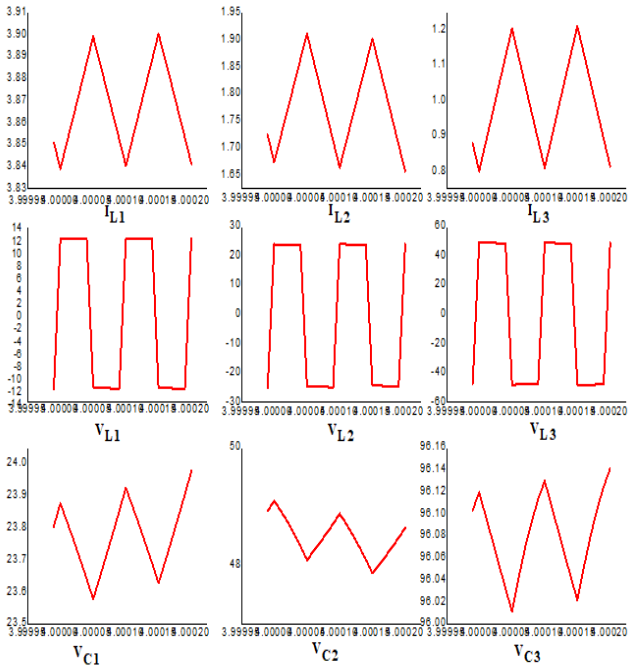

Fig. 9 Simulation waveforms in CCM for; Inductors L1, L2, L3, and capacitors C1, C2, C3.

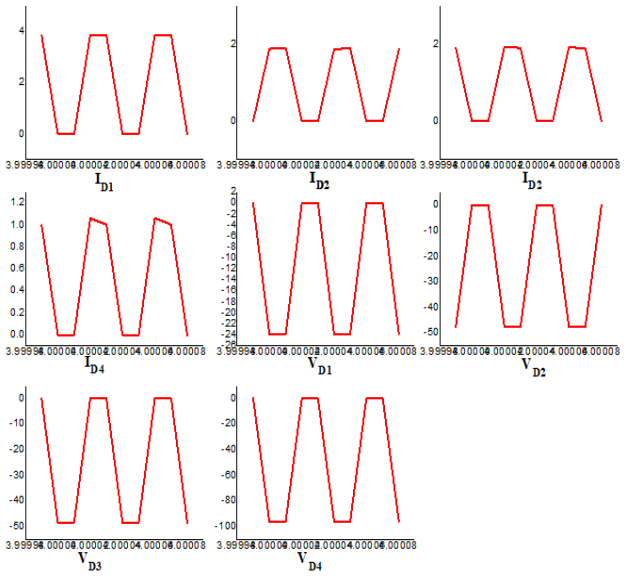

Fig. 10 Simulation waveforms in CCM for; Diodes D1, D2, D3, D4.

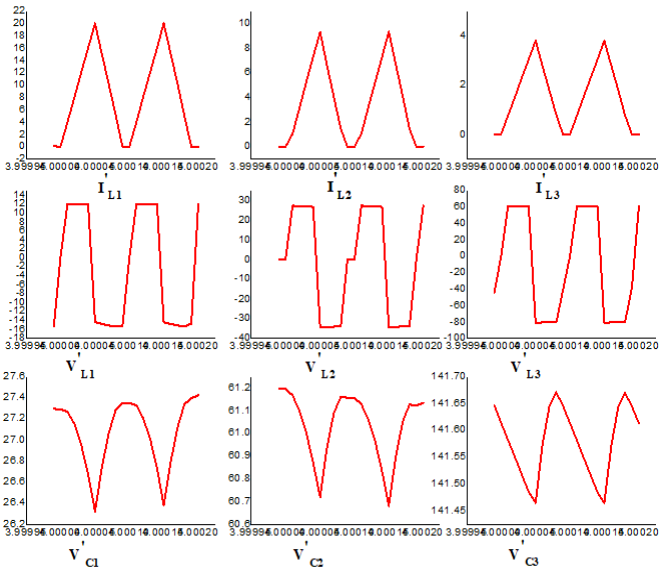

Fig. 11 Simulation waveforms in DCM for; Inductors L1, L2, L3, and capacitors C1, C2, C3.

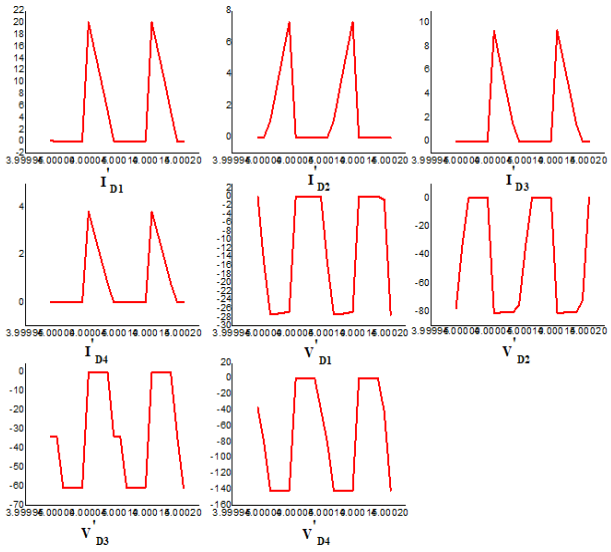

Fig. 12 Simulation waveforms in DCM for; Diodes D1, D2, D3, D4.

5. Conclusion

In this paper, a new structure of DC-DC boost converter based on cascade configuration was proposed. The converter employed two switches operating at the same duty cycle; therefore, additional driving circuitry was not required. The resulting gain equation signified that the proposed converter could achieve high voltage gain as compared to other conventional boost converters, which makes it more suitable for high step-up applications. Such as a photo-voltaic system, boosting up the low voltage of solar panels to the required dc bus voltage, and impart noteworthy role in augmenting the voltage in DC nano-grids. Theoretical concepts were fairly validated by simulation results. The output voltage obtained in CCM and DCM from simulation was 96 V and 121V, respectively considering Vi = 12V, f = 10kHz, D = 50% and D' = 50%. The switches current in CCM was found to be 2.7A and 2.1A, while the current in DCM was found to be 6A and 4A, respectively. The obtained simulation results have fairly approved the analysis of the presented converter.

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