Practical LDPC Coding System Design – An Overview

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Summary:

LDPC codes are gaining attention due to their excellent performance but still there are a lot of challenges in the hardware implementation. Due to high complexity, LDPC codes generally offer high processing delays which makes them impractical for many applications. Efforts have been made to keep a good tradeoff between the complexity and performance. Quasi cyclic LDPC codes have the advantage of both encoding and decoding over the conventional LDPC (non-structured) as they reduce the hardware complexity greatly. It has simplified the check and variable node interconnections. QC LDPC has limited decoding performance compared to unstructured random LDPC codes. Different architectures have been proposed to improve the throughput as well as reduce the complexity.

Key words:
QC LDPC, Sum Product Algorithm, Digital Communication, Error Correction Coding, LDPC Codes.

1. Introduction and Overview of LDPC

1.1 High Performance, High Complexity LDPC Codes: Theoretical Approach

LDPC codes [1] construction requires parameters such as row and column weights, rate, girth and code length. LDPC codes are classified into two types of constructions. The first one is random construction that offers flexibility in term of design and construction. This method has been used in LDPC codes construction as presented by Macky & Neal and S.Chung et al [].The LDPC codes has shown the capacity approaching [2-4, 5-7] high performance but at the cost of high complexity which makes it unsuitable for some practical applications and hardware implementation.

1.2 Better Performance, Low Complexity LDPC Codes: Practical Approach

LDPC parity check matrix can be obtained by cyclic shift [8] or circular permutation matrices [9] which facilitate the hardware implementation and still offer better performance. The following methods are adopted for getting the Parity Check matrix from circulants.

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1.2.1 Quasi Cyclic LDPC Code Design

The Quasi cyclic LDPC codes can be obtained by the following methods.

i. **Identity matrix:** The parity check matrix from Identity circulants. This is the usual and easy approach to construct the QC LDPC codes.

ii. **Q matrix:** An n×n circulant permutation matrix is called Q-matrix [10] if the number of 1's is only one in every column, every row and every diagonal of it.

iii. **D matrix:** An n×n circulant permutation matrix is called D-matrix if the number of 1's is only one in every column and every row of it [11]. The D-vector describing D-matrix is composed of arithmetic progression. The formula of general term of arithmetic progression is an =a1 + (n-1)b.

iv. **Progressive edge growth (PEG):** In the standard PEG algorithm [12], given the graph parameters, i.e., the number of symbol nodes, the number of check nodes, and the symbol-node-degree sequence, an edge-selection procedure is started such that the placement of a new edge on the graph has as small impact on the girth as possible.

v. **Modified PEG to get Q and D matrices:** In [13], here two new parameters have been added to PEG, i.e., the dimension of a circulant permutation matrix and permutation vector are introduced. Using this algorithm, the QC-LDPC codes based on D-matrix and Q-matrix, outperform the QC-LDPC code based on an identity matrix and PEG random LDPC code, which suggests that D-matrix and Q-matrix are more suitable to be used in QC-LDPC codes than identity matrix as it exhibits better performance and have hardware friendly structures for practical application. The idea of permutation vector is originally introduced. The main principle of this method is to optimize the placement of a new edge to maximize the local girth length under the permutation vector constraint.

vi. **Row Division method:** This method is to construct large girth QC LDPC [14, 15] codes and cut down the hardware implementation cost. The row groups are paired two times the row weight, which has the complexity as compared to the connection of individual columns and rows. The new codes offer more flexibility in term of girth, code rates and codeword length.

1.2.2 Quasi Cyclic LDPC Encoder Implementation

i. **Shift Register based Implementation:** QC–LDPC codes have encoding advantage over conventional LDPC codes and their encoding can be carried out by shift register [16] with complexity linearly proportional to the number of parity bits of the code. Additionally QC-LPDC codes require less amount of memory as compared to the general LDPC codes, since their parity check matrices consist of the circulant permutation matrices or the zero matrices.

ii. **RAM based Implementation:** RAM (instead of shift register) based QC-LDPC encoder [17] for hardware resource saving and high data throughput (in terms of data input to output). Less XOR & AND gates are required due to equal or more zeros compared to 1's. Secondly this eliminates the need for additional CLB logic for the parallel to serial circuit, and enhances the data throughput

1.2.3 LDPC Decoding Algorithms

i. **Sum Product Algorithm:** This is also well known as the belief propagation algorithm invented by Gallager and then re-invented by Mackay & Neal.The sum product algorithm [1, 18-20] has shown best performance with highest complexity.

ii. **Logarithmic Sum Product Algorithm:** The logarithmic sum-product algorithm [20] is an enhanced version of the sum-product algorithm, introducing LLR (Logarithmic Likelihood Ratio), which reduces most multiplication to addition.

iii. **Min Sum Algorithm:** To simply belief propagation (BP) algorithm, min-sum algorithm[21-23] is introduced to reduce the complexity of the check node operation. The min-sum algorithm is in effect a simplified version of the logarithmic sum-product algorithm. It trades off precision for speed by eliminating the need for addition in the message update process, resulting in a possible increase in the number of iterations. Several modification has been made to improve the performance and convergence as in references [24-27].

1.2.4 LDPC Architecture

i. **Parallel:** This Architecture [28] gives extremely low power dissipation and high throughput but is not area efficient.

ii. **Serial:** In [29], the serial approach has been adopted, stating that parallel approach leads to an extremely complex interconnect problem. One possibility to avoid the extremely complex interconnect problem is going for a sequential decoding machine that processes the input nodes in a linear order from the first bit-node to the last in every iteration. The results is that the complex interconnect can be solved in random access memory. This is called the serial approach. To reach the required throughput performance tens or more decoding machines can be used on one chip.

iii. **Semi-Parallel:** The semi-parallel decoding architecture [30] offers a better balance between throughput performance and hardware requirements, which is fairly advisable for QC- LDPC codes. This kind of architecture generally achieves a good trade-off between hardware complexity and decoding throughput.

iv. **Minimum Semi-Parallel:** This architecture [31] shows that there is a throughput/complexity gap between semi-parallel and serial decoders, which would be efficient and suitable for wireless applications. In order to exploit the gap between semi-parallel and serial decoders, a novel LDPC decoding architecture with a flexible inter-circulant time-sharing scheme of processing units is proposed in this paper. The architecture is advisable and competent for efficiency-demanding applications, such as wireless and mobile systems and portable devices. Practical implementation is one of the major issues of LDPC codes.

2. LDPC Coding System Design

2.1 LDPC Decoder Architecture

Different approaches are made to implement the LDPC codes in hardware looking at requirements of the market. Some researchers emphasized the high throughput but overlooked the complexity while others proposed the very low area, energy efficient but with inefficient low throughput. The following block diagram in Fig. 1 best defines the architectural and throughput along with complexity trade off [31]. Parallel architecture gives extremely high power dissipation and high throughput and need large hardware area due to complex interconnection. On the other side serial architecture offers very low power dissipation, require less hardware. QC LDPC makes the tradeoff between serial and parallel architecture.

2.2 Semi Parallel Architecture

Semi parallel architecture [32-35] are often designed for structured codes. Structured codes have the inherit advantage that could be used to reduce hardware implementation. The structure of a code affects the interconnection network between variable and check nodes. Quasi cyclic LDPC codes are the type of structured codes that have less hardware complexity and cost of both the encoder and decoder. The cyclic shifting of the identity sub-matrices of the QC LDPC parity check matrix, simplifies routing and addressing of messages within processing nodes. Decoder architecture mainly differ in processing node inter-connection, communication scheduling and node implementations.

Semi parallel decoding architecture employs a time sharing scheme of processing units to reduce hardware complexity. To demonstrate the parallelism between the block of the QC LDPC, the parity check matrix is shown as an example. In this example, the parity check matrix is divided into two horizontal layers and three vertical layers. There is a serial processing inside each block and a parallel processing between blocks. In Fig. 1, the serial factor of the parity check matrix is which is the size of the circulant. This type of architecture is called semi-parallel.

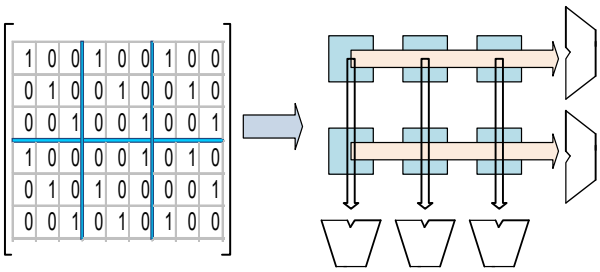

Fig. 1 QC LDPC Parity check matrix and its semi-parallel processing hardware.

When the serial factor becomes equal to M (or N) then it is totally serial architecture and if it becomes equal to 1, then the architecture is fully parallel. The complexity can be reduced further if the gap between serial and semi-parallel architecture is efficiently utilized.

2.3 Hardware Realization of LDPC Decoder

Layered decoder is one of the practical decoder used for fast convergence and is also memory efficient. The flow for the layered decoder is show in the Fig. 2. V2C is the message from variable to check node, C2V is check to variable node message passing and Est. code is the estimated code word.

There is some other more efficient technique in which both row and column offsets are not required, only one shift matrix and the shifting information [36] is required. The offset matrix in Fig. 1 can be written as the offset entries for each of the circulant matrices.

$$offsets = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 2 & 1 \end{bmatrix} \Leftrightarrow H = \begin{bmatrix} I_0 & I_0 & I_0 \\ I_0 & I_2 & I_1 \end{bmatrix} \quad (1)$$

Now the Fig. 2 can also be shown with this offset control matrix in the Fig. 3.

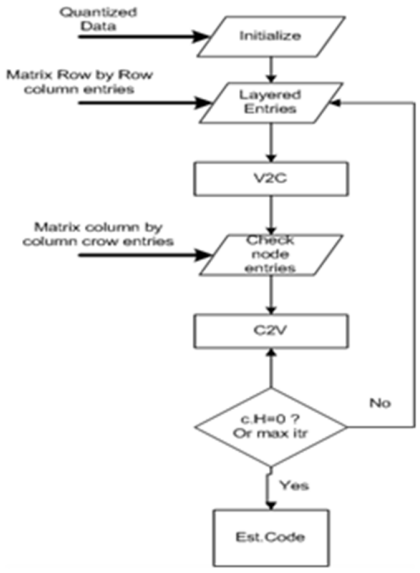

Fig. 2 Data flow of a typical layered decoder.

2.4. Clipping and Quantization

The Finite word length of the soft information [37], as one of the major factors, affects size of the memory, the complexity of computation logic, routing complexity, and the decoding performance of an LDPC code. It also decides the size of memory to store the intrinsic and extrinsic messages and determines the overall implementation area in the partially parallel (semi-parallel) LDPC decoder. Therefore, the reduction of the finite word length without significant performance loss can decrease the hardware size which includes the computation logic and memory banks.
For a binary BPSK modulated data, transmission over AWGN corrupts this data and then the data is no more integer and shaped as floating point. The received values are clipped symmetrically [38] at a certain threshold and then uniformly quantized in the range. There are quantization

intervals, symmetric with respect to the origin and each represented by quantization bits. Integer numbers to be assigned and at bit nodes, an outgoing message is clipped to if it exceeds the threshold. Table 1 shows the comparison for quantization values.

Table 1: Comparison of uniform and non-uniform quantization for LDPC decoder

Decimal values (After AWGN)	(6:3) Uniform Quantization	5-bits Non-uniform Quantization	(5:3) Uniform Quantization	4-bits Non-uniform quantization
± 0.000	s00000	s0000	s0000	s000
± 0.125	s00001	s0001	s0001	s001
± 0.250	s00010	s0010	s0010	s010
± 0.375	s00011	s0011	s0011	s011
± 0.500	s00100	s0100	s0100	
± 0.625	s00101	s0101	s0101	s100
± 0.750	s00110	s0110	s0110	
± 0.875	s00111		s0111	s101
± 1.000	s01000	s0111	s1000	
± 1.125	s01001		s1001	
± 1.250	s01010	s1000	s1010	
± 1.375	s01011		s1011	
± 1.500	s01100	s1001	s1100	s101
± 1.625	s01101		s1101	
± 1.750	s01110	s1010	s1110	s111
± 1.875	s01111			
± 2.000	s10000	s1011	s1111	
± 2.125	s10001			
± 2.250	s10010			
± 2.375	s10011			
± 2.500	s10100	s1100		
± 2.625	s10101			
± 2.750	s10110			
± 2.875	s10111			
± 3.000	s11000	s1101		
± 3.125	s11001			
± 3.250	s11010			
± 3.375	s11011			
± 3.500	s11100	s1110		
± 3.625	s11101			
± 3.750	s11110	s1111		
± 3.875	s11111			

A good tradeoff between hardware complexity and decoding performance is given with 6-bits quantization scheme for both intrinsic and extrinsic messages, which are uniformly quantized with 1 sign bit, 2 integer bits and 3 fractional bits.

This fixed size quantization of 6-bits shows good performance. Some papers have suggested some adaptive quantization [39] techniques for either intrinsic or extrinsic messages. In an LDPC decoder both intrinsic (channel values) and extrinsic information (C2V messages) has to be stored. If we can use less number of quantization bits, the storage complexity will be significantly reduced. In fact, using less quantization bits can greatly simplify the hardware implementation but will degrade the error performance of LDPC decoder. Adaptive quantization can be used to get better BER performance.

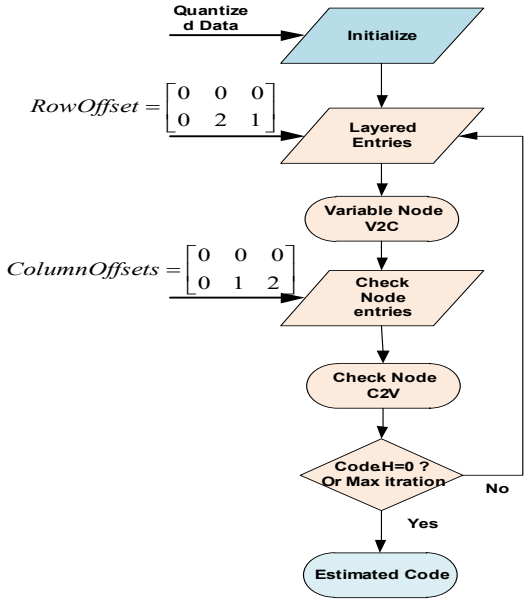

Fig. 3 Layered Decoder with Offsets entries

2.5 Variable and Check Node Hardware Units

At each iteration, the check update node unit (CNU) is computing the sign and the absolute min values. It finds the smallest two inputs and the index of the smallest one. CNU function is to find the first minimum, 2nd minimum and the index of the 1st minimum for each row process. The hardware for the CNU process is shown in the Fig. 4 & 4a. After finding that values, these are stored for later use in variable node update unit (VNU) as in Fig. 5. In VNU the input messages are firstly transferred to two complement format and then do the add operation. Finally they are transferred back to sign and magnitude format and is scaled.

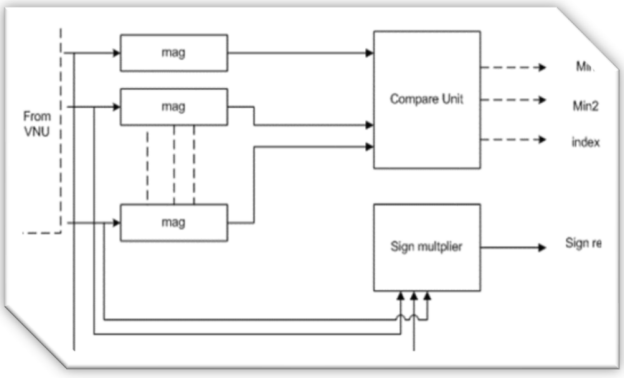

Fig. 4 CNU Architecture to find the minimum values and the signs

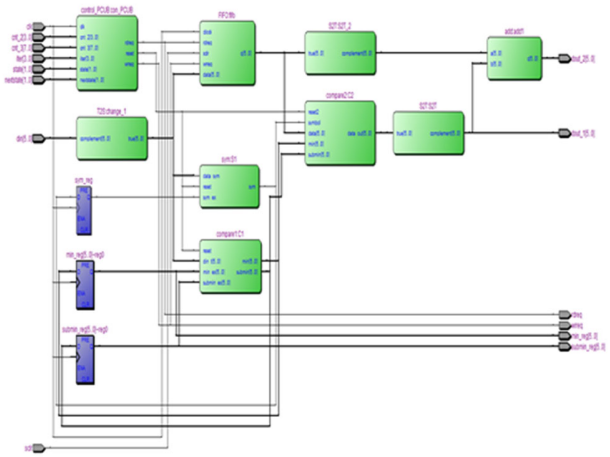

Fig. 4a. Verilog RTL view of CNU

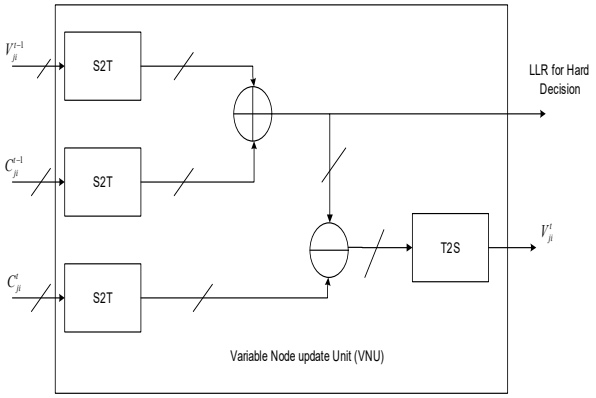

Fig. 5 VNU detail for updating the variable message and data out for hard decision

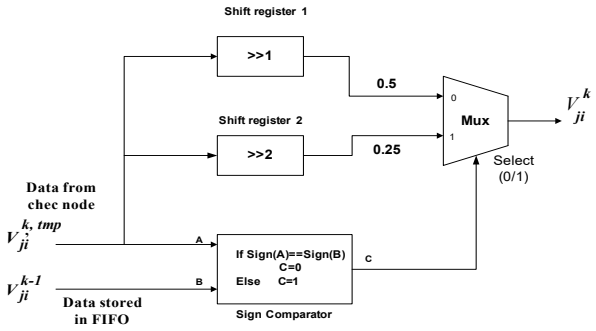

Fig. 6 Hardware implementation for normalized values based on sign comparator

3. Case Study

In this section, an overview of QC LDPC Codes' implementation has been discussed. The section introduces some concepts which can be implemented on hardware. A new method [40, 41] is suggested here for LDPC decoder on FPGA and other hardware. In Fig. 6, a new hardware to scale and update the variable message is shown. The scaling factor multiplication complexity is the same as used in already existing hardware LDPC decoders. It uses two different scaling factors which give better approximation in decoding. The increase in hardware complexity is the sign comparator , FIFO and multiplexer. This circuitry does not add time latency as sign comparator implemented as exclusive OR gate and multiplexer delay is not that significant. The scaling factor chosen are according to the message overestimation and hardware implementation.

We see that the signs are compared as XOR gate and the scaling factors are basically implemented as data bus shifting. The only problem is with FIFO as it is required to temporarily store the message and then utilized for comparison. FIFO need to be synchronized properly as the date to VNU comes from CNU is fast. Some alternate solutions can be found to store the date temporarily if FIFO seems not a good solution. One module is required for each row block of a QC LDPC parity check matrix used in decoding. Fig. 7 gives the sign comparator while Fig. 8 shows FIFO in connection with data for sign comparison and then scaled accordingly.

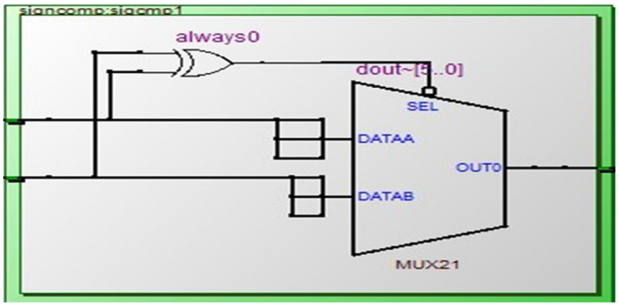

Fig. 7 RTL Verilog view of sign comparator

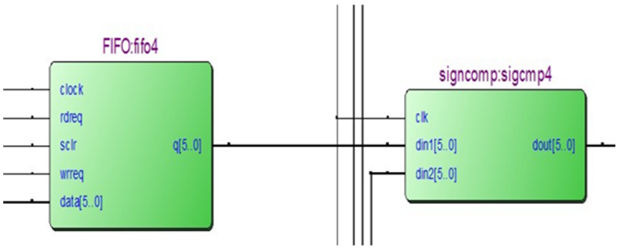

Fig. 8 FIFO for temporarily storing data for sign comparison

4. Analysis and Future Direction

Due to the near Shannon limit performance, LDPC has got popularity among the coding theory researchers. The main drawback of the LDPC code is the hardware complexity and long processing delay. The tradeoff between hardware complexity and processing delay has been achieved but still some further improvement is needed for implementing the algorithms more efficiently. While there has been much research on LDPC decoders and their VLSI implementations, many difficulties to achieve requirements remain such as lower error floors, reduced interconnect complexities, smaller die areas, lower power dissipation [42], and design re-configurability to support multiple code lengths and code rates [43].

The motivation behind this paper is today's demand for low-cost, low complexity but reliable and high throughput solutions in the digital communication technology. The invention of the re-configurable hardware (FPGA) has triggered the fast prototyping and hardware realization for complex solutions. Together with re-configurable hardware, simulation tools (e.g. Verilog, Matlab, and C++) give the accurate performance evaluation for the algorithms with realistic channel models like AWGN, fading channels etc.

Ever since the rediscovery of LDPC codes; Code design & construction [44], efficient encoding and decoding, performance analysis, and applications of these powerful error-correction codes in digital communication [45] and storage systems have always been the focal points of research.

5. Conclusion

Wireless communication and data storages require error correction codes for reliable information flow. In this paper, the design of encoder and decoder for LDPC codes has been presented to give an overview of implementation. Different current architectures and some new directions are given to efficiently implement the low complexity LDPC decoder for an improved performance. This paper aims to give an overview of the LDPC codes to researcher in academia and to those working in industry.

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